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REVIEW ARTICLE
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REVIEW: DESIGN OF DIRECT FORM TRANSPOSED FIR INTERPOLATOR

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Abstract: This paper presents the designing of direct form transposed FIR interpolator on the basis of MAC algorithm. There are various configurations or structures for realization of any FIR filter System. For wireless and audio applications the use of efficient digital filter is increasing because of speed of conversion and less hardware requirement. Interpolator is useful for smoothing signals such as sinusoids or baseband I/Q waveforms. Interpolation is the estimation of the unknown, or the lost, samples of a signal using a weighted average of a number of known samples at the neighborhood points. For this purpose, interpolation filter is used to produce new samples of the waveform accurately without reducing signal quality. A number of design methodologies have been used and work done on interpolator has been reviewed.

Keywords: DSP, Interpolator, MAC, FIR

INTRODUCTION

Digital signal processing (DSP) refers to the technique of representing digital signal to improve accuracy and reliability of digital communication. Digital filters play very important roles in DSP systems. Systems that use different sampling rates at different stages are called the multi rate systems. The multi rate techniques are used to convert the given sampling rate to the desired sampling rate, and to provide different sampling rates through the system without destroying the signal components of interest. There are a number of applications where sampling rate must be changed and it is done with the help of interpolators and decimators. Up sampler and down sampler are used to change the sampling rate of digital signal in multi rate DSP systems. But this rate conversion leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors.

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost. Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require multi rate digital signal processing (DSP) algorithms for several crucial operations in order to increase speed, reduce area and power consumption. Due to a growing demand for such complex DSP applications, high performance, low-cost implementations of DSP algorithms are receiving increased attention among researchers and design engineers. Multi rate digital filters and filter banks find application in communications, speech processing, image compression, antenna systems, analog voice privacy systems, and in the digital audio industry. During the last several years there has been substantial progress in multi rate system research. So in this paper a Direct form FIR transposed Structure is presented for wireless applications.

IMPULSE RESPONSE OF FIR FILTER

The impulse response of FIR filter is characterized by the following equation:

$$Y = \sum_{k=0}^{n} C_k x_k \quad (1)$$

Where $C_1, C_2, \ldots\ldots C_k$ are fixed coefficients and the $x_1, x_2 \ldots\ldots x_k$ are the input data words.
So, for digital implementation it will require *K* multiply-and-accumulate (MAC) operations.

INTERPOLATOR

Interpolation is the estimation of the unknown, or the lost, samples of a signal using a weighted average of a number of known samples at the neighborhood points. Interpolators are used in various forms in most signal processing and decision making systems. Up-sampling is the process of increasing the sampling rate of a signal. For instance, up-sampling raster images such as photographs means increasing the resolution of the image. The up-sampling factor (commonly denoted by L) is usually an integer or a rational fraction greater than unity [2]. This factor multiplies the sampling rate and develops an output sequence xu[n] with a sampling rate that is *L* times larger than that of the input sequence *x*[*n*]. The up sampler is shown in Figure 1. Up-sampling operation is implemented by inserting equidistant zero-valued samples between two consecutive samples of x[*n*]. The input and output relation of up sampler can be expressed as:

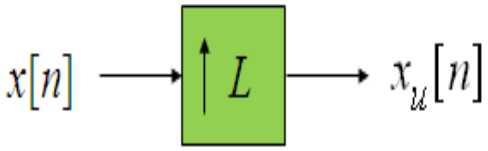

Figure.1.Up-sampler

$$X_u[n] = \begin{cases} x\left(\frac{n}{2}\right) & n = 0, \pm 2, \pm 4 \\ 0 & otherwise \end{cases} \quad (2)$$

The z transform of input output relation is given by:

$$X_u[Z] = \sum_{\substack{n=-\infty \\ n=even}}^{\infty} X_u \; n \; Z^{-n} \qquad (3)$$

$$= \sum_{m=-\infty}^{\infty} X(m) z^{-2m} \quad = X(Z^2) \qquad (4)$$

In a similar manner, we can show that for a *factor-of-L up-sampler*

$$X_{u(Z)} = X(Z^L) \qquad (5)$$

On the unit circle, for z $= e^{jw}$, the input-output relation is given by:

$$X_u(e^{jw}) = X(e^{jwL}) \qquad (6)$$

A factor-of-2 sampling rate expansion leads to a compression of X (e^{jw}) by a factor of 2 and a 2-fold repetition in the baseband [0, 2π].This process is called imaging as we get an additional "image" of the input spectrum. Similarly in the case of a factor-of-*L* sampling rate expansion, there will be L-1 additional images of the input spectrum in the baseband. Interpolator is used as low pass filter to remove the xu [n] images and in effect "fills in" the zero-valued samples in xu[n] with interpolated sample values.

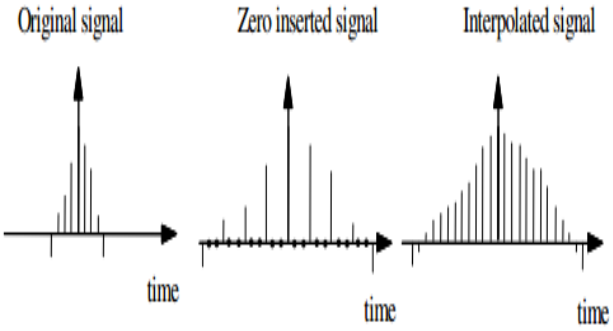

Figure.2 Upsampling

INTERPOLATION OF A SAMPLED SIGNAL

A common application of interpolation is the reconstruction of a continuous-time signal x(t) from a discrete-time signal x(m). The condition for the recovery of a continuous-time signal from its samples is given by the Nyquist sampling theorem. The Nyquist theorem states that a band-limited signal

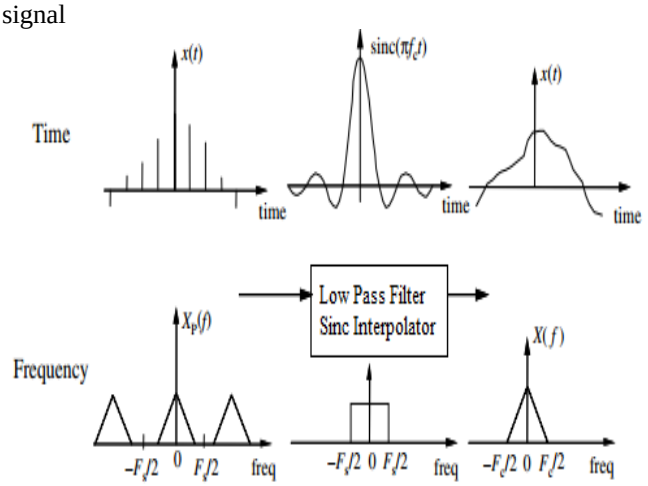

Figure.3 Reconstruction of continous time signal from its samples

Reconstruction of a continuous-time signal from its samples. With a highest frequency content of Fc(Hz), can be reconstructed from its samples if the sampling speed is greater than 2Fc samples per second. Consider a band-limited continuous-time signal x(t), sampled at a rate of Fs samples per second. The discrete-time signal x (m) may be expressed as in fig 3.

MAC ALGORITHEM

Digital finite impulse response (FIR) filters form the basis for numerous digital signal processing Applications. The basic operation needed to implement a FIR filter is the signed multiply-and-accumulate (MACS), which is traditionally performed using a hardware multiplier peripheral in any DSP device [4]. It computes the product of two numbers and add thad product to the accumulator(Register).

$$a \leftarrow a+(b*c) \qquad (7)$$

The output of Accumulator is fed back to one input of adder so that on each clock cycle,the output of multiplier is added to register.It can compute product more quickly than method of shifting and adding.

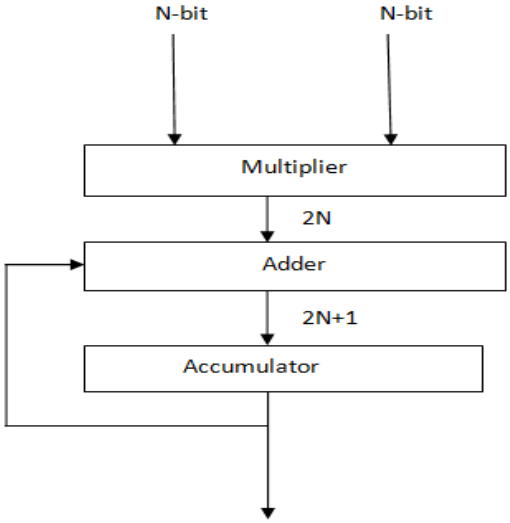

Figure-4.Basic Structure of MAC

Some of the MSP430 devices have an integrated hardware multiplier that can perform this MACS operation allowing these devices to run the FIR filter algorithm more efficiently than devices without a built-in

DIRECT FORM FIR TRANSPOSED STRUCTURE

Direct Form Transposed filters are becoming a very important component in the design of various filter structures due to the fact that it reduces the cost and complexity of the filter. Ideal band- limited interpolation will take a digital (sampled) signal and produced an interpolated signal that will be identical to the signal that would be obtained by sampling the underlying continuous-time signal at a higher rate. Ideal band-limited interpolation can be accomplished by means of up sampling and using an ideal low pass filter. A time-domain interpretation of the ideal interpolator, naturally leads to transposed implementations. Direct Form FIR transposed structure is given in figure 5.

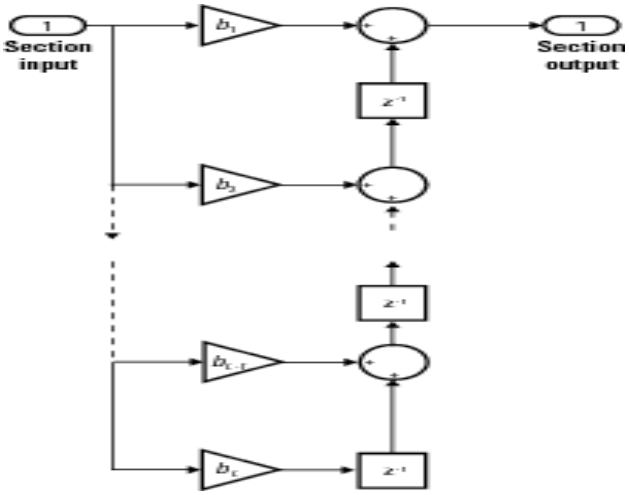

Figure 5 Direct –Form FIR Transposed Structure

Transposed structures are a way of doing sampling-rate conversion that leads to very efficient implementations. But more than that, it leads to very general viewpoints that are useful in building filter banks. In many applications we need to compensate for nonlinear distortions. Consequently, we have to apply nonlinear signal processing because linear methods do not provide acceptable results. Examples of such applications include equalization of digital communication channels, pre and post-linearization, e.g., for loudspeakers, microphones, or analog front-ends (AFE) of communication system.

ALGORITHMS USED PREVIOUSLY

There are a number of techniques which are used to design interpolator. A few of them has been reviewed and following interferences has been drawn.

Dalut Algorithem:

Interpolator is particularly useful for smoothing signals such as sinusoids or baseband I/Q waveforms. For these signals, interpolation filter is used to accurately produce new samples of the waveform without reducing signal quality. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost. In this paper a multiplier less technique is used which substitutes multiply-and-accumulate operations with look up table (LUT) accesses. Interpolator has been implemented using Partitioned distributed arithmetic look up table (DALUT) technique. This technique has been used to take an optimal advantage of embedded LUTs of the target FPGA. The proposed interpolator has been designed using half band transposedFIR structure with Matlab, simulated with Modelsim XE, synthesized with Xilinx Synthesis Tools (XST) and implemented on Spartan-3E based 3s500efg320-4 FPGA device. The proposed LUT based multiplier less approach has shown a maximum operating frequency of 61.6 MHz as compared to 52.1 MHz in case of MAC based multiplier approach by consuming considerably less resources to provide cost effective solution for wireless communication systems. This method is useful to enhance the system performance in terms of speed and area. [2].

PID (Proportional integral Derivative) control algorithm:

In this paper, an efficient design scheme for implementation of PID control algorithm in FPGA is presented. The algorithm is implemented using a Distributed Arithmetic (DA) based scheme where a Look-Up-Table (LUT) mechanism inside the FPGA is utilized. In this paper, a novel DA-based PID controller was presented, for FPGA implementation. By using the DA- based LUT scheme, the memory inside FPGA has been utilized to provide efficient design for PID controllers, resulting in reduction of FPGA design cost. In addition, due to the flexibility of the LUT in the FPGA, this FPGA-based PID controller can be easily extended It can be shown that DA based PID controller saves 80% hardware utilization and 40% savings in power consumption compared to the multiplier-based scheme. It also offers good closed loop performance while using less resources, resulting in cost reduction, high speed and low power consumption which are desirable in embedded control applications. Finally as a case study we discuss the DA based scheme to design a temperature control system. The design uses a modular approach, so that some modules can be reused in other applications. The complete digital control system is built using commercial FPGA‘s to demonstrate its efficiency. The same approach can be extended to design other embedded controllers using FPGA [6].

Variable Precision MAC algorithm:

The MAC Unit plays an important role in DSP applications. When implemented on FPGA, many MAC Units can be implemented on a single FPGA flexible to different design architectures. Hence the need of efficient MAC Units arises for filter applications. This paper discusses about variable precision based MAC Unit implemented on FPGA at algorithmic level. The proposed algorithm for FIR Filters is high performance and area efficient than the conventional MAC Unit. The delay for VP MAC Unit is reduced nearly by 60% than the conventional MAC Unit. The design of High Performance Digital Filtering algorithms with is a typical challenge for most of the designers. As it requires high sampling rate, implemented with less cost, which is flexible to adopt for different designs or structures and is fabricated for different technologies using same or similar process. The variable precision can be used for implementing MAC Unit. The MAC Unit forms a important unit or structure in the design of filters. Instead of using directly if multiple multipliers are used to implement the same then it is called as variable precision MAC. This paper discusses about the MAC Unit designed to implement FIR filters on FPGA based on variable precision [7].

MAC Algorithm:

This paper is implementing hardware design in Field Programmable Gate Arrays (FPGAs) is a formidable task. There is more than one way to implement the DSP design for FFT processor and digital FIR filter. Based on the design specification, careful choice of implementation method and tools can save a lot of time and work. There are toolboxes available to generate VHDL (Verilog) descriptions of the filters which reduce dramatically the time required to generate a solution. Time can be spent valuating different implementation alternatives. Proper choice of the computation algorithms can help the FPGA architecture to make it efficient in terms of speed and/or area. The creation and analysis of representative data can be a complex task. Most of the filter algorithms require multiplication and addition in real-time. The unit carrying out this function is

called MAC (multiply and accumulate). Depends on how good the MAC is, the better MAC the better performance can be obtained [8].

PROPOSED WORK

Till now most of the work on interpolator has been done on speed and area parameters. A number of techniques are being used to enhance the speed and reduce the area. But many researches has limitation in speed and area [3], because computational complexity greatly depends upon the design of filter that is being used. In order to minimize the existing problem there is a great requirement of such a model which should have higher speed and lesser area.so, main emphasis is given to propose a model of interpolator with MAC algorithm which will reduce the computational complexity and to increase the performance in terms of speed and area parameters. As in case of wireless applications there is a great necessity to optimize the speed factor as well as area factor.

SCOPES OF WORK

Nowadays in wireless and audio application the use of efficient digital filter is increasing because of the speed of conversion and the less hardware requirement. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost. In hardware DSP a signal can be scaled by a coefficient‘s processing. For wireless applications there is great necessity of such interpolator which will consume less area and more speed without delays. To avoid computational complexity we give preference to Direct Form FIR Transposed structure. This research may have the scopes in the areas of communication system, multimedia, image processing, digital signal processing

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