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Small-Signal Amplifier with JFETs in Triple Darlington Topology

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ABSTRACT: New circuit model of small-signal amplifier with three identical JFETs in Triple Darlington topology is proposed and qualitatively analyzed for the first time. Unlike CS-JFET amplifiers, the voltage gain of the proposed circuit is found considerably higher than unity. This amplifier successfully scales signal excursions swinging in 1-35mV range at 1KHz frequency. In wide-band performance range (7.59MHz bandwidth), the proposed amplifier simultaneously produces high voltage and current gains (18.039 and 150.729 respectively) with considerably low THD (0.22%). These properties offer a flexible application range to the proposed circuit as high-voltage-gain wide-band amplifier in 42Hz-7MHz frequency range. An additional biasing resistance R_A (ranging in 250Ω-100KΩ) is to be essentially used in the proposed circuit to maintain its voltage/current amplification property. This amplifier can also be tuned in specific range of audible frequency which explores its suitability to use in Radio and TV receiver stages. Small-signal AC analysis of the circuit, variations in voltage gain as a function of frequency and different biasing resistances, temperature dependency of performance parameters like voltage gain, bandwidth, current gain and total harmonic distortion of the amplifier are widely studied to observe a wide spectrum of qualitative performance.

KEYWORDS: Small-signal amplifiers, Triple Darlington amplifiers, Circuit Design and Simulation.

I. INTRODUCTION

Amplifying signals through Darlington pair and CS-JFET is an important phenomenon of electronics [1]-[5]. Application range of Darlington pair extends from small-signal to power amplifier circuits [3]-[6] whereas a CS-JFET amplifier is preferably used as impedance matching circuit in cascade stages of amplifiers [1]-[2]. Principally, both the circuits, Darlington pair and CS-JFET amplifier possess high input impedance, low output impedance and a voltage gain approximately equal to unity [1],[5]. However, current gain of CS-JFET is generally found higher [1]-[2] despite the fact that Darlington pair's current gain factor β_D is treated as identical to the product of current gains of the individual transistors ($\beta_D \approx \beta_1\beta_2$) [3]-[6]. When used in small-signal amplifiers, Darlington pairs (or Triple Darlington unit) exhibit problem of poor response at higher frequencies [3]-[9]. However, a CS-JFET holds fair frequency response in audible range [1].

With an intention of combining the desirable features of FETs and BJTs, Aina et al [10] in 1993 developed a JFET-BJT Darlington pair and received simultaneously high input impedance and current gain (high transconductance). This attempt motivated many workers, and therefore, a series of modifications in Darlington's composite unit or in respective amplifier circuits were suggested in next two decades [3]-[15]. These efforts include the use of devices other than BJTs [11],[14],[15], hybrid combination of devices in Darlington's topology [12],[13] and, moreover, use of additional biasing components in amplifier circuits [3]-[9], [11]-[14]. Experimentation with triple Darlington topology is also attempted in the sequence [7]-[9], [13]-[15] to achieve the higher voltage/current gain for small input signals.

Present investigation is focused around the use of three identical JFETs in Triple Darlington configuration [14]. This unit with appropriate biasing components is explored herein a new circuit model of small-signal amplifier suitable for the applications where high input impedance and output conductance is the desirable feature. Proposed circuit provides simultaneously high voltage and current gain with fair response at higher frequencies. Possible applications of the proposed design includes high-gain-low-THD-wideband-amplifiers, cascadable gain blocks for radio and TV receiver stages and high frequency power sources.

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II. DESCRIPTION OF CIRCUITS

Present work consists of a qualitative comparison between small-signal JFET Darlington pair amplifier (Fig.1) [11] and a new circuit model of small-signal amplifier using three identical JFETs in Triple Darlington topology (Fig.2).

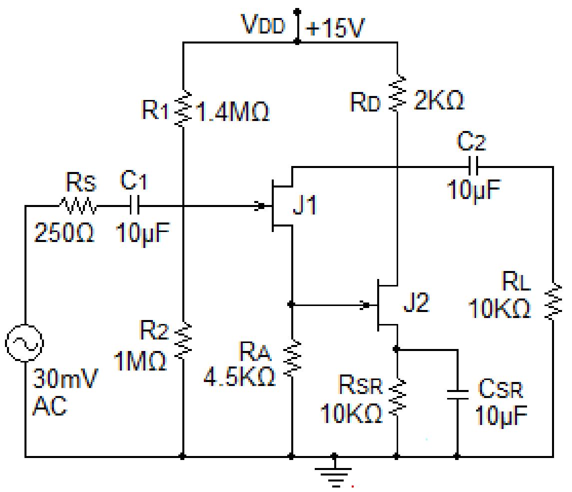

Fig.1. JFET Darlington pair amplifier
(Reference Amplifier)

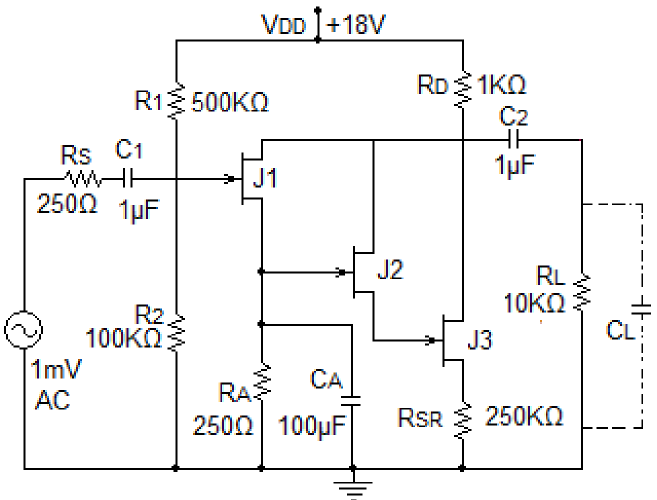

Fig.2. JFET Triple Darlington amplifier
(Proposed Amplifier)

Fig.1 amplifier [11] is treated herein 'Reference-amplifier' whereas 'Proposed-amplifier' of Fig.2 is obtained by including one more JFET in the design of Fig.1 and by introducing a bypass capacitor C_A across additional biasing resistance R_A [3], [6]-[9]. Both designs use potential divider biasing methodology [1], [3], [6]-[9]. Devices used are N-Channel JFETs (J2N4393 with threshold voltage V_{TH}=−1.422). Other biasing components and DC supply with their suitable values are shown in respective designs.

PSpice simulation [16] is performed to carry out present investigations. Both circuits are fed by 1V AC input signal source, from which, an AC signal of 30mV for reference amplifier (Fig.1) [11] and 1mV for proposed amplifier (Fig.2) at 1KHz frequency is drawn as input for the amplification purpose. However, respective amplifiers fairly amplify AC input signals in 30-80mV and 1-35mV range at 1KHz frequency.

III. RESULTS AND DISCUSSIONS

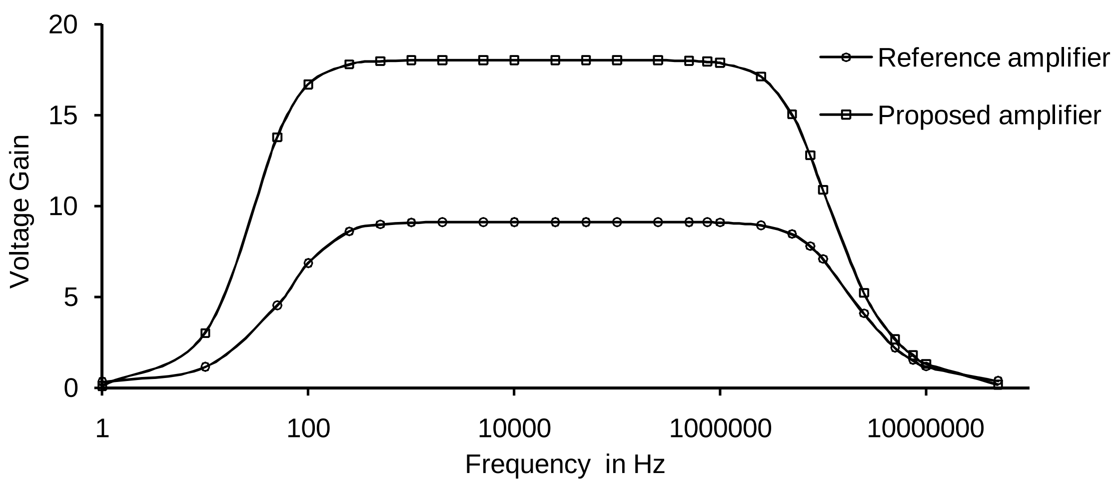

Fig.3. Voltage gain as a function of frequency

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Fig.3 depicts the variation of voltage gain as a function of frequency. Reference amplifier [11] produces 9.1084 maximum voltage gain A_{VG}, 530.909 maximum current gain A_{IG} and 12.365MHz bandwidth B_W. However proposed amplifier generates 18.039 maximum voltage gain A_{VG} (18.485mV peak output voltage V_{OP}), 150.729 maximum current gain A_{IG} (1.8484µA peak output current I_{OP}) and 7.59MHz bandwidth B_W (with lower-cut-off frequency f_L=42.542Hz and upper-cut-off frequency f_H=7.5906MHz).

Total Harmonic Distortion (THD) for the mentioned circuits are calculated for first few harmonic terms [1], [11], [13]-[14]. Calculations suggest that proposed amplifier possesses only 0.22% THD for first 10 harmonic terms whereas reference amplifier [11] holds 2.15% THD for 8 significant terms.

Variation of A_{VG}, A_{IG} and bandwidth B_W with temperature is also measured and listed in TABLE I. Bandwidth of both Fig.1 and Fig.2 amplifier slightly increases but voltage and current gains significantly decrease at rising temperature. This decrement in A_{IG} and A_{VG} is associated with 'negative temperature coefficient' property of drain current [1]. The drain current in JFET is mainly composed of majority carriers whose mobility decreases at elevated temperature due to enhanced collision rate between them and the remaining ions in the semiconductor channel [1]. This decreases the drain current and therefore the effective current and voltage gain of the JFET based system of Fig.2.

TABLE I. VARIATION IN A_{VG}, A_{IG} & B_W WITH TEMPERATURE

Temp (°C)	Reference Amplifier (Fig.1)			Proposed amplifier (Fig.2)		
	A_{VG}	A_{IG}	B_W (MHz)	A_{VG}	A_{IG}	B_W (MHz)
-30	10.37	604.55	11.95	20.75	173.39	7.01
-10	9.91	577.68	12.10	19.76	165.12	7.20
0	9.68	564.67	12.17	19.28	161.12	7.30
27	9.10	530.90	12.36	18.03	150.72	7.59
50	8.64	503.65	12.52	17.03	142.34	7.85
80	8.06	470.08	12.63	15.79	132.01	8.24

Decisively, the inclusion of third JFET and shifted position of the by-pass capacitor stimulates proposed circuit to appear with the intense performance in low temperature region. Proposed amplifier produces enhanced voltage gain, considerably low THD, reduced current gain and bandwidth than reference amplifier and receives a fair exemption from the 'poor frequency response problem' of small-signal Darlington pair (or Triple Darlington) amplifiers at higher frequencies [3],[11]. Small-signal AC equivalent circuit [1], [14] of proposed amplifier to determine the expression for A_{VG} is drawn in Fig.4.

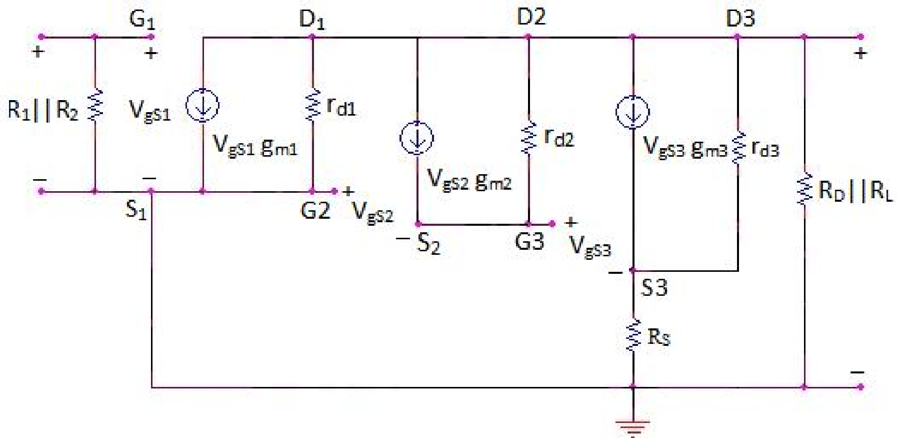

Fig.4. AC equivalent circuit of proposed amplifier

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Refer Fig.4. Proposed amplifier does not allow any significant current to flow from drain to source of J2 as $g_{m2}\rightarrow 0$ mho and $I_{D2}\approx 3.26\times10^{-12}$amp, thereby, producing a capacitive effect in the circuit. Presence of Gate-Source-Capacitance C_{GS} of 2.67pF and Gate-Drain-Capacitance C_{GD} of 2.98pF due to the typical placement of J2 in proposed circuit generates an intense capacitive effect. Thus, the combination C_{GS} and C_{GD} due to centrally located JFET J2 (Fig.2) causes an effective reduction in the bandwidth. Hence, during the analysis of equivalent circuit (Fig.4) for AC voltage gain, J2 of the proposed amplifier is virtually treated as absent. This opinion suggests following expression for the approximate value of A_{VG} of proposed amplifier-

$$A_{V(Prop)} \approx \frac{-g_{m1}\left[1+R_s\left(g_{m3}+\frac{1}{r_{d3}}\right)\right]}{\frac{1}{r_{d3}}+\left(\frac{1}{R_O}+\frac{1}{r_{d1}}\right)\left[1+R_s\left(g_{m3}+\frac{1}{r_{d3}}\right)\right]} \quad (1)$$

Analysis of Fig.4 shows that the equivalent output resistance of the proposed amplifier $R_O\approx R_L||R_D$ is lower (≈909.09Ω) than the equivalent input resistance $R_I\approx R_1||R_2$ (≈83.33KΩ). In continuation, AC voltage gain is estimated by equation and figured out to be -19.84 with r_{d3}=42.36Ω, g_{m1}=0.0218mho and g_{m3}=0.0000149mho for the suggested design of Fig.2. Negative sign in equation shows phase reversal of the output voltage waveform [1]. The value of A_{VG} obtained by equation (1) is approximately 1.7 point higher than the observed value. Conclusively, the theoretically computed value of A_{VG} (-19.84) based on equation and the observed value (-18.039) are clearly justifying the school-of-thought used to design Triple Darlington JFET amplifier of Fig.2.

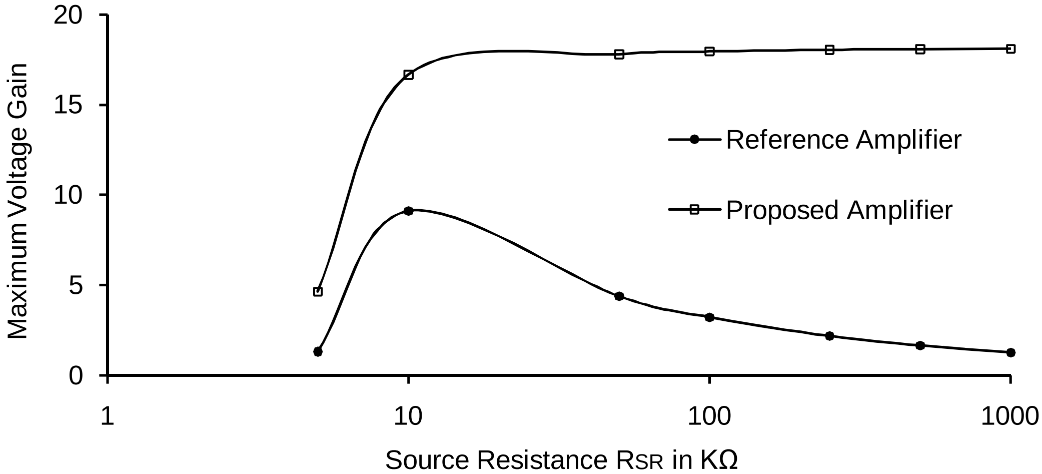

Fig.5. Variation of Maximum Voltage gain with R_{SR}

Variation of A_{VG} with source resistance R_{SR} is shown in Fig.5. A_{VG} of reference amplifier receives its maximum at 10KΩ, thereafter; it decreases at elevated values of R_{SR} [11]. However, for proposed amplifier, A_{VG} rapidly increases with R_{SR} up-to 10 KΩ, thereafter steadily reaches to its maximum at 250 KΩ of R_{SR}. In fact, at lower values of R_{SR} (<10KΩ), the third JFET (J3) appears in the circuit with positive V_{GS} which responsibly widens the channel and therefore enhances I_D and I_{RD}. This results in reduction of I_{RL} and therefore A_{VG}. However at higher values of R_{SR} (≥10KΩ) the third JFET (J3) also appears with negative V_{GS} which shrinks the effective channel width and forces I_D and I_{RD} to reduce. This enhances I_{RL} and therefore A_{VG}.

Performances of both the amplifiers highly depend on additional biasing resistance R_A [11], [13]-[14]. Variation of A_{VG} with R_A is shown in Fig.6. Reference amplifier with R_A=3KΩ crops A_{VG}=6.49 which further rises and reaches about saturation with A_{VG}=9.3052 at R_A=100KΩ. However proposed amplifier crops 18.039 A_{VG} at R_A=250Ω which exponentially decreases at higher values of R_A and reaches to 1.1812 at R_A=100KΩ. In proposed amplifier, as R_A rises to 100KΩ from 250Ω, the corresponding I_{RA} decreases and makes V_{GS} of J1 and J3 more negative. This forces J1 and J3 to appear in the circuit with narrower channel, thus increasing channel resistance and reducing I_D. Additionally, the constant status of R_{SR} (250KΩ), enhanced channel resistance and R_A altogether forces I_{RL} to trim-down to a considerable limit, hence causes reduction in A_{VG}. In addition, if R_A is removed from the proposed circuit and bypass capacitor is introduced across R_{SR}, A_{IG} of the amplifier reaches to a non-significant value 0.003 whereas A_{VG} reaches below unity to a value 0.111. Hence, the presence of additional biasing resistance R_A in proposed amplifier

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configuration is essential to establish 'Triple Darlington JFET unit' suitable for amplification of small-signals [11], [14].

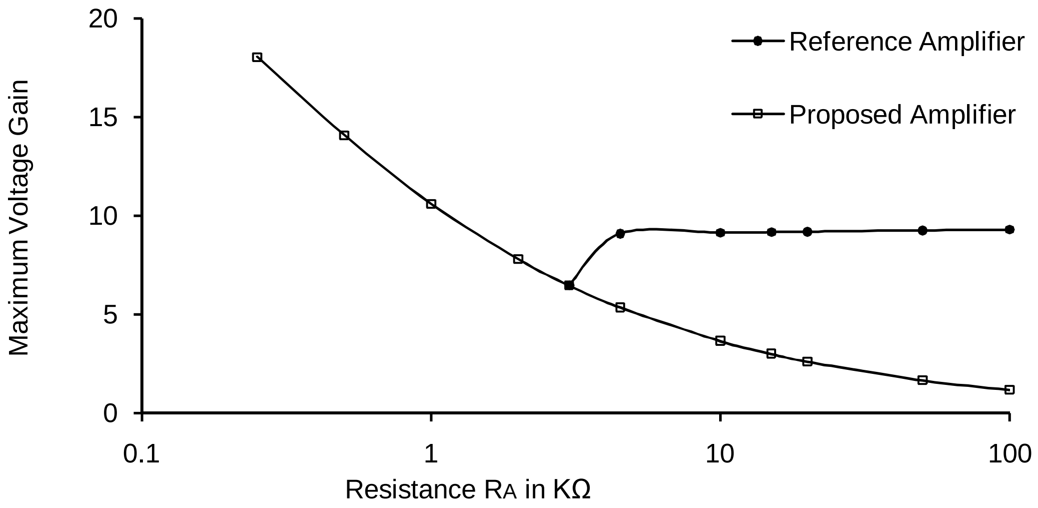

Fig.6. Variation of A_{VG} with Additional Biasing Resistance R_A

Fig.7 explains the dependency of A_{VG} on drain resistance R_D. It is observed that A_{VG} of the reference amplifier increases almost linearly with R_D but beyond the critical limit of 2KΩ amplifier doesn't behave properly [11]. However, A_{VG} of the proposed amplifier initially increases with $R_{D,}$ becomes maximum at R_D = 1KΩ, and thereafter, falls down to a non significant value at R_D=2KΩ. This behavior may be explained by AC equivalent circuit of Fig.3.5. The contribution of $V_{gS3}g_{m3}$ is found maximum at R_D=1K (91.93uA) and minimum at R_D=2KΩ (3.76nA). This reduces the current through r_{d3} and R_{SR} at R_D=1KΩ and increases the current contributed to R_L hence A_{VG} increases. The reverse situation appears for R_D=2KΩ hence A_{VG} goes down to a non-significant value.

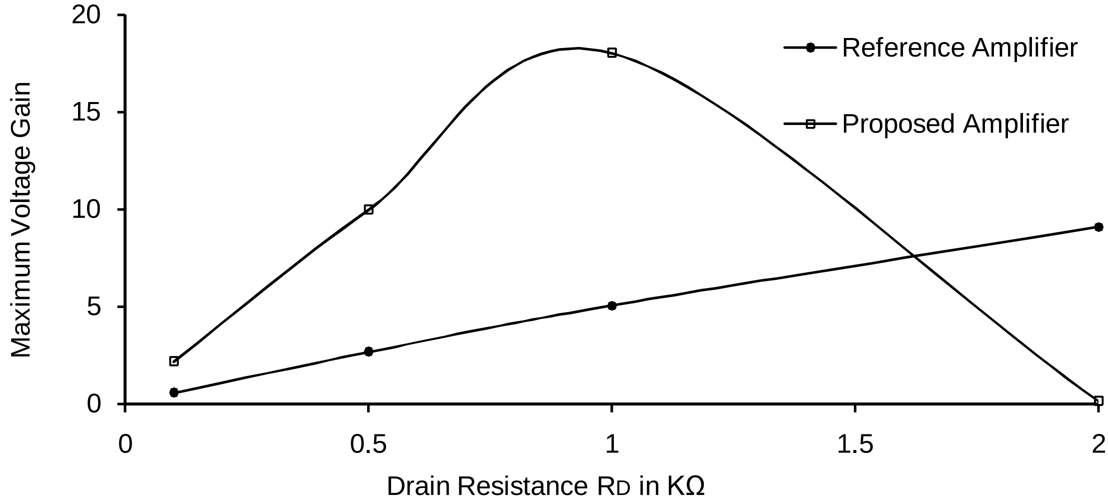

Fig.7. Variation of Maximum voltage Gain with Drain Resistance

Effect of DC supply voltage V_{DD} on A_{VG} for both the amplifiers is depicted in Fig.8. Reference amplifier produces a fruitful response in 11-50V range of V_{DD} whereas Triple Darlington JFET based proposed amplifier produces a meaningful response in 13-50V range of V_{DD}. A_{VG} of the reference amplifier rises almost linearly with V_{DD} [11] whereas it climbs up to 18.73 at 20V of V_{DD} for proposed amplifier, thereafter, adopts almost similar behaviour as of reference amplifier. The behaviour of proposed amplifier with V_{DD} resembles with the observations of Vernon et al for small-signal CS MOSFET amplifier [17].

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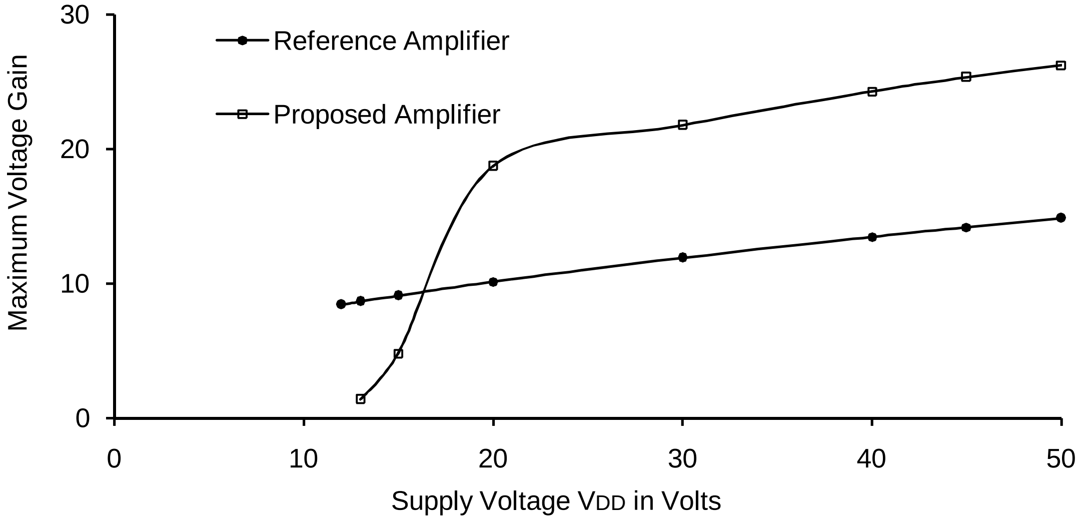

Fig.8. Variation of Maximum Voltage gain with Supply Voltage

Tuning performance of the proposed amplifier is analysed with R_A-C_A and R_L-C_L networks (C_L is shown by doted lines in Fig.2) [4], [11]-[14]. Respective observations are listed in TABLE II

TABLE II. VARIATION IN F_H, F_L, B_W, A_{VG}, & A_{IG} WITH C_A & C_L

C	Variations corresponding to C_A				
	f_H	f_L	B_W	A_{VG}	A_{IG}
0.1µF	7.64MHz	37.21KHz	7.601 MHZ	18.012	121.35
1µF	7.57MHz	3.74KHz	7.569 MHZ	18.036	147.08
10µF	7.59MHz	374.86Hz	7.593 MHZ	18.039	150.39
100µF	7.59MHz	42.54Hz	7.589 MHZ	18.039	150.73
-	Variations corresponding to C_L				
1pF	7.28MHz	42.55Hz	7.28 MHZ	18.039	150.728
10pF	5.48MHz	42.54Hz	5.48 MHZ	18.039	150.727
100pF	1.52MHz	42.55Hz	1.52MHZ	18.037	150.712
1nF	184.04KHz	42.51Hz	184KHz	18.020	150.573

Tuning with C_A is obtained for variations between 0.1µF and 100µF. Changes in C_A merely create any variation in A_{VG}, whereas it changes A_{IG} to some extent and plays a prime role in adjusting the mid-bandwidth (e.g. for C_A=0.1µF, bandwidth extends between f_L=37.211KHz and f_H=7.639MHz). It is evident that f_H remains almost constant with any variation in C_A whereas f_L considerably shifts towards lower values at increasing C_A. Similarly, inclusion of C_L across R_L also plays an important role in adjusting mid-band frequency range. Tunning is obtained for variations of C_L between 1pF and 1nF with a feature that the bandwidth of the amplifier shifts towards lower range (from MHz to KHz range) on the frequency axis. A_{VG}, A_{IG} and f_L varies in a very short range for corresponding variations in C_L, whereas f_H shifts towards lower values with increasing C_L.

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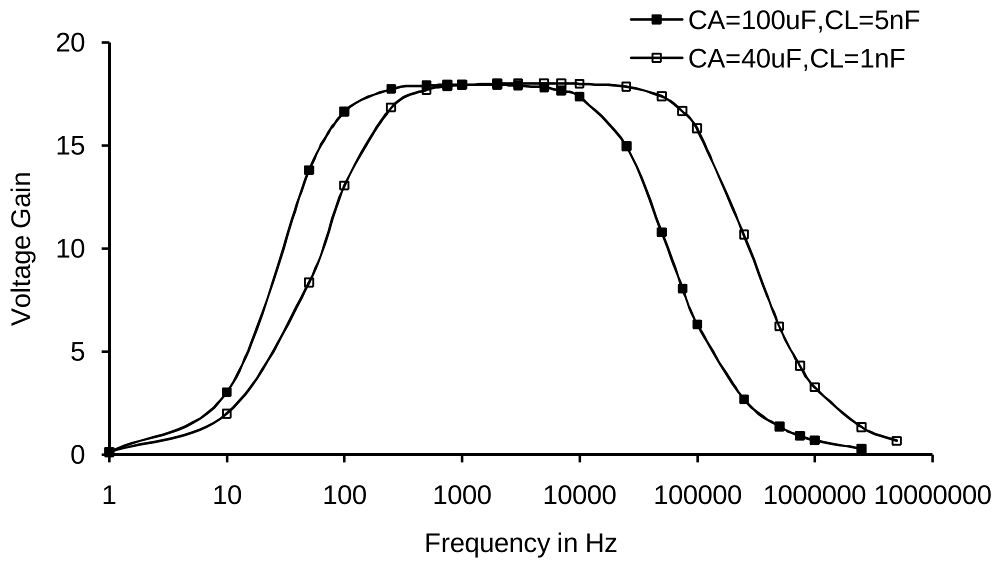

Fig.9. Tuned frequency response of JFET Triple Darlington amplifier at two different combinations of C_A and C_L

Thus, adjustment of C_A and C_L leads to a tuning which enables the central frequency of the response to coincide with frequency of a desired communication channel [4], [11], [17]. This idea is depicted in Fig.9 for two different combinations of C_A and C_L. Tuning idea in Fig.9 leads to a result that Triple Darlington configuration of JFETs can be applied to receive signal of a specific channel by filtering-out or attenuating others.

IV. CONCLUSIONS

Three identical JFETs are used in triple Darlington topology to explore the proposed circuit as high-gain-wide-band small-signal amplifier. The proposed amplifier can be tuned in permissible audible frequency range approximately extended from 42Hz to 7MHz. The additional biasing resistance R_A (range 250**Ω-100KΩ**), is to be essentially included in the proposed circuit to maintain its voltage/current amplification property. In absence of R_A, amplifier's voltage and current gains climbs-down below unity and makes it purpose-less. This amplifier can effectively scale up small-signals ranging in 1mV to 80mV at 1KHz input frequency and is free from the problem of poor response of conventional small-signal Darlington pair amplifiers at higher frequencies. With sufficiently wide bandwidth and high voltage and current gains, the proposed amplifier generates only 0.22% harmonic distortion. This logically sets the power gain of proposed amplifier considerably larger than unity. The proposed amplifiers shows a considerable response for V_{CC}, R_{SR}, R_D and R_L almost in the same way as is usually observed for small-signal RC coupled Common Source amplifiers.
Collective features provide a different shade to the proposed circuit in respective class of JFET based small-signal audio amplifiers with a possibility to use the circuit design in high-gain-low-THD-wideband-amplifiers, cascadable gain blocks for radio and TV receiver stages and high frequency power sources.

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BIOGRAPHY

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