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Small-Signal Amplifier with MOSFET and BJT in Triple Darlington Configuration

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Abstract- A new circuit model of a small-signal narrow-band amplifier is proposed and analyzed on the qualitative scale. Proposed amplifier uses two MOSFETs and a BJT in Triple Darlington configuration with two additional biasing resistances in the circuit. With low distortion percentage (1.28%), the proposed circuit successfully amplifies small-signals of 1-10mV range and simultaneously provides high voltage gain (311.593) and current gain (13.971K) with narrow bandwidth (9.665KHz). Variations of maximum voltage gain with different biasing resistances and DC supply voltage and the temperature sensitivity of various performance parameters are elaborately studied and discussed in length. Qualitative performance of the proposed amplifier is also compared with the circuit which is having BJT-MOSFET in Darlington pair configuration. The proposed amplifier can be used to process audio range signal excursions and may be useful for those applications where high voltage and current gain would be the prime requirement of amplification in narrow-band low frequency region.

Key words: Small-signal amplifiers, Common Source MOS amplifiers, Triple Darlington amplifiers, MOSFET Darlington pairs

I. INTRODUCTION

Output signals from most of the electronic systems (e.g. analog, digital, or a hybrid combination of analog and digital) are often too small in magnitude to be processed reliably for executing any useful function [1]-[3]. Thus, most of these systems require amplifiers for scaling signals to a useful level [1]-[3].

A Darlington pair, which is basically a composite unit of two similar transistors, has effectively proved its importance to amplify small signals [1], [3]-[7]. It has superior characteristics regarding current gain but a major drawback is encountered with its performance. At higher frequencies its response becomes poorer than that of a single transistor amplifier [3]-[7]. Numerous modifications are attempted in Darlington pair amplifiers to overcome this problem [8]-[12]. Some of the popular attempts are- the use of dissimilar active devices or hybrid combination of active devices in Darlington pair or in Triple Darlington topology and the use of some additional biasing resistances in respective amplifier circuits [8]-[12].

The present investigation is focused around a compound unit which uses two identical MOSFETs and a BJT in 'Triple Darlington topology' [3], [6], [9]. Though the MOSFETs are suitable for developing high speed switching circuits, memory segments, logic gates, buffer amplifiers, power amplifiers and trans-conductance amplifiers [13]-[14] but in the present exploration a MOSFET dominant Triple Darlington structure with appropriate biasing components is explored as new circuit model of a small-signal amplifier. This amplifier may be suitable for those applications where high voltage and current gain would be the prime requirement of amplification in narrow-band low frequency region. Dependency of qualitative performance of the proposed amplifier on various biasing parameters, biasing supply and operational frequency is analyzed and also compared with a high voltage gain small-signal amplifier that uses MOSFET and BJT in Darlington pair [15].

II. CIRCUIT DESCRIPTION

The present work comprises a qualitative comparison between Circuit-1 [15] and Circuit-2 amplifiers. Circuit-1 amplifier, which is stated herein 'Reference Amplifier' [15], consists a compound unit of BJT and MOSFET in Darlington pair configuration with an additional biasing resistance R_A in the circuit. However, Circuit-2 amplifier, which is termed as 'Proposed Amplifier' in the manuscript consists two identical MOSFETs and a BJT in Triple Darlington configuration. Unlike reference amplifier, the drain point of M1 and collector point of Q1 in proposed amplifier are directly connected to the biasing supply V_{CC}. In addition, two additional biasing resistances R_A and R_{AD} are introduced in the proposed circuit with bypass capacitor across the source resistance. Both the amplifier circuits are properly biased using potential divider network with biasing parameters as described in TABLE I.

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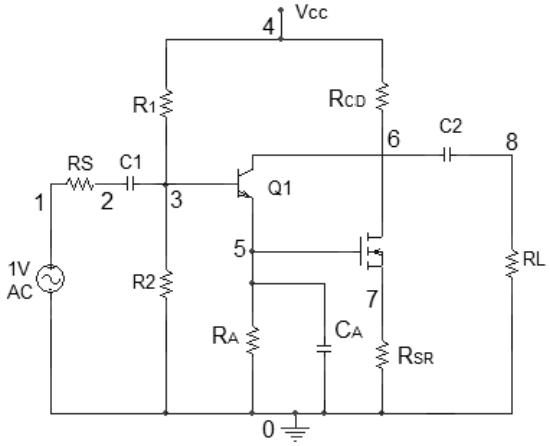
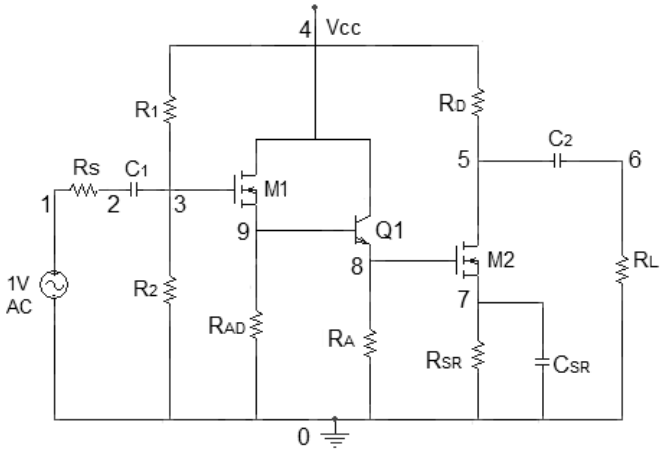
Reference amplifier [15] is biased with +15V whereas proposed amplifier is biased with +18V DC power supply. PSpice simulation (Student version 9.2) is performed to carry out present investigations [16]. Observations are procured by feeding the respective amplifier circuits with 1V AC input signal source, from which, a small-distortion-less AC signal of 1mV at 1KHz frequency is drawn as input for the amplification purpose.



Circuit-1: Reference amplifier
(BJT and MOSFET in Darlington pair configuration)



Circuit-2: Proposed amplifier
(MOSFETs and BJT in Triple Darlington configuration)

TABLE I

Components	Description	Circuit-1	Circuit-2
M1	N-Channel MOSFET (V_{TH}=2.831)	Not available	IRF150
Q1	NPN BJT (β=255.9)	Q2N2222	Q2N2222
M2	N-Channel MOSFET (V_{TH}=2.831)	IRF150	IRF150
R_S	Biasing Resistance	500Ω	500Ω
R_1	Biasing Resistance	47KΩ	1.3MΩ
R_2	Biasing Resistance	5KΩ	1MΩ
R_D/R_{CD}	Drain Biasing Resistance	10KΩ	5KΩ
R_{SR}	Source Biasing Resistance	2KΩ	1KΩ
R_A	Additional Biasing Resistance	1KΩ	10KΩ
R_{AD}	Additional Biasing Resistance	Not available	10KΩ
R_L	Load Resistance	10KΩ	10KΩ
C_1 , C_2	Coupling Capacitors	1µF	1µF
C_A/C_{SR}	By-pass Capacitors	10µF	100µF
Biasing Supply	DC Biasing Supply	+15V DC	+18V DC
AC Signal	Input AC Signal range for distortion-less output	1-15mV (1KHz)	1-10mV (1KHz)

COMPONENT DETAILS OF THE CIRCUITS UNDER DISCUSSION

III. RESULTS AND DISCUSSIONS

The amplifier of Circuit-1 [15] provides fair and distortion-less results for 1-15mV AC input signals whereas amplifier of Circuit-2 provides the same for 1-10mV.

Variation of maximum voltage gain as a function of frequency for both the amplifiers is depicted in Fig.1. The reference amplifier of Circuit-1 [15] produces 115.522 maximum voltage gain A_{VG} (with 106.607mV peak output voltage V_{OP}), 35.242 maximum current gain A_{IG} (with 10.661µA peak output current I_{OP}) and 22.258KHz bandwidth (with lower cut-off frequency f_L=443.567Hz and upper cut-off frequency f_H=22.702KHz) whereas the proposed amplifier of Circuit-2 produces 311.593 maximum voltage gain V_{AG} (with 314.923mV V_{OP}), 13.971K maximum current gain I_{AG} (with 31.494µA I_{OP}) and 9.665KHz bandwidth (with f_L=151.056Hz and f_H=9.817KHz). Clearly, the proposed amplifier produces higher voltage and current gain on the cost of reduced bandwidth.

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In fact polarity of Darlington's unit is determined by the driver device [17]. For example, a paired unit consisting BJT as driver and MOSFET as follower device (as in Circuit-1) principally behaves like a BJT dominating Darlington unit [11]-[12], [17]. Thus, due to driver MOSFET, the overall behaviour of the compound unit in proposed amplifier seems to be inclined more towards MOSFET and motivates respective circuit to produce extra ordinarily high current gain [11]-[12], [17]. However, considerably high voltage gain of the proposed amplifier is perhaps due to the presence of hybrid combination of MOSFETs and BJT along with two additional biasing resistances in the circuit configuration.

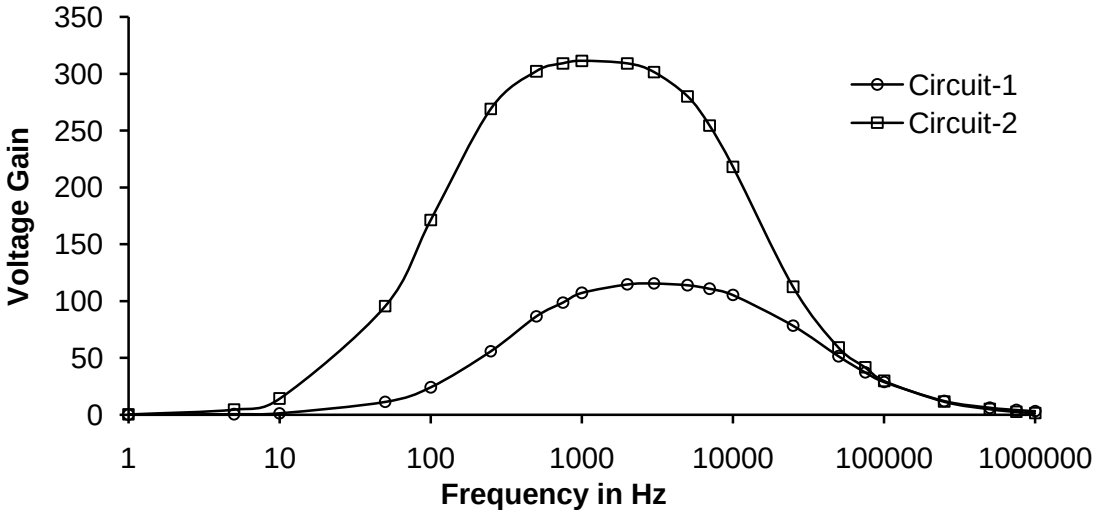

Fig.1. Variation of Voltage gain with Frequency

In addition, both the amplifiers show phase reversal in respective output waveforms [10]-[12], [15], [17]. In fact, CE and CS configurations of the respective devices independently produce phase reversal in their output waveforms. Phase switching property of the independent active devices is responsible to produce 180^{o} phase difference in the output waveform of reference and proposed amplifiers which are using compound unit of BJT-MOSFET and MOSFET- BJT-MOSFET in their circuit configurations [10]-[12], [15], [17].

It is also worth mentioning that both the amplifiers effectively remove the problem of poor response of conventional Darlington pair or Triple Darlington amplifiers at higher order frequencies in the prescribed frequency-response range [6]-[9], [10]-[12], [15], [17].

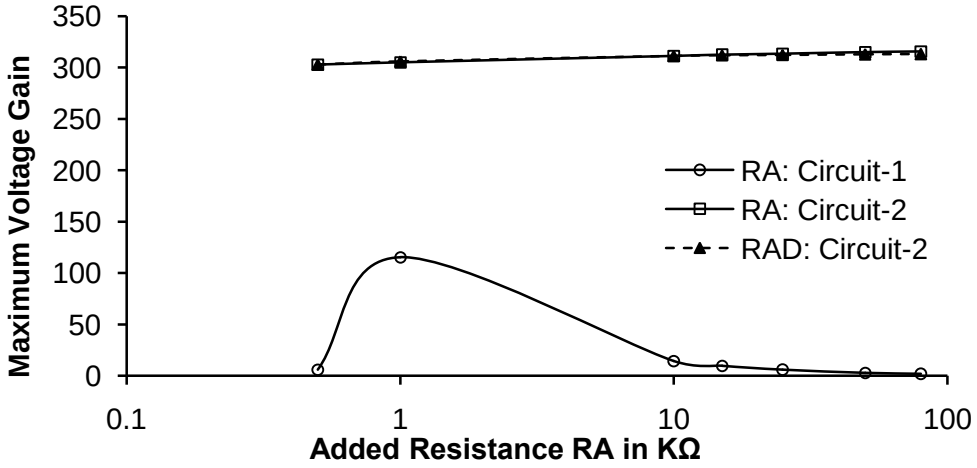

Fig.2. Variation of Maximum Voltage gain with Added Resistance R_A and R_{AD}

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Dependency of maximum voltage gain on additional biasing resistances R_A and R_{AD} for reference and proposed amplifiers is depicted in Fig.2. Both the amplifiers do not show any response for R_A<0.5KΩ [15]. Corresponding voltage gain for Circuit-1 amplifier founds its maximum at R_A=1KΩ, thereafter, it decreases almost exponentially at elevated values of R_A [15]. However for amplifier of Circuit-2, the A_{VG} increases only a bit at increasing values of R_A and R_{AD} and finally acquires a state of saturation beyond 50KΩ. Corresponding curves suggest that the proposed amplifier shows almost similar response for R_A and R_{AD} in terms of voltage gain. In addition, respective voltage and current gains for the reference amplifier without R_A and for the proposed amplifier without R_A and/or R_{AD} dips below unity. Thus, the presence of R_A and/or R_{AD} in respective amplifiers is essential to maintain the high voltage and current gain features.

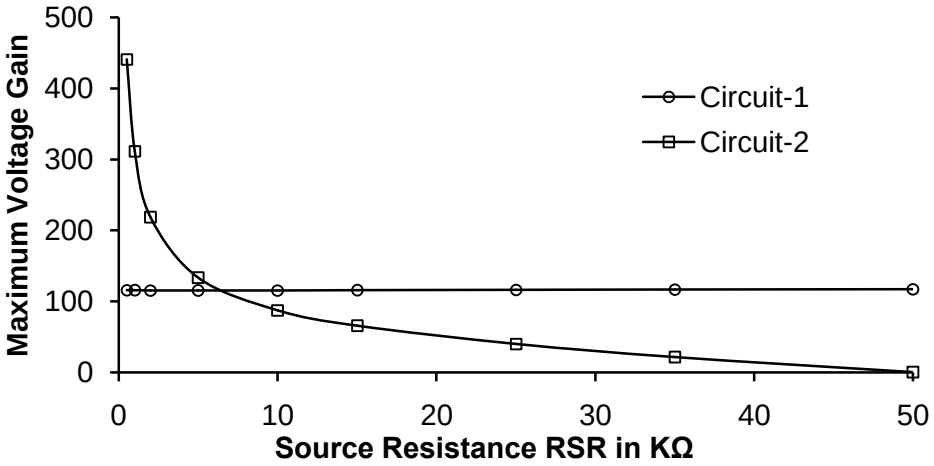

Fig.3. Variation of Maximum Voltage gain with Source Resistance R_{SR}

Variation of maximum voltage gain A_{VG} with Source resistance is shown in Fig.3. For reference amplifier, the increasing values of source resistance R_{SR} barely affect the voltage gain [15]. If R_{SR} is removed from Circuit-1, corresponding values of A_{VG}, A_{IG} and THD rises fractionally to 115.872, 35.288 and 3.50% respectively whereas bandwidth reduces to 21.458 KHz (with f_L=449.388Hz and f_H=21.908KHz). Thus, the removal of R_{SR} from reference amplifier Circuit-1 hardly affects the performance of amplifier [15]. However, A_{VG} of the proposed amplifier found its maximum at R_{SR}=0.5KΩ, thereafter, it decreases almost exponentially to reach below unity at 50KΩ. Though the voltage gain of proposed amplifier reaches to maximum at 0.5KΩ of R_{SR} but it limits the performance of the circuit to 1-4mV input AC signal. Since the resistance R_{SR} in the proposed amplifier circuit behaves as source resistance for MOS driven composite unit therefore the source degeneration property of common source MOSFET amplifier forces voltage gain to fall almost exponentially with R_{SR} (Fig.3).

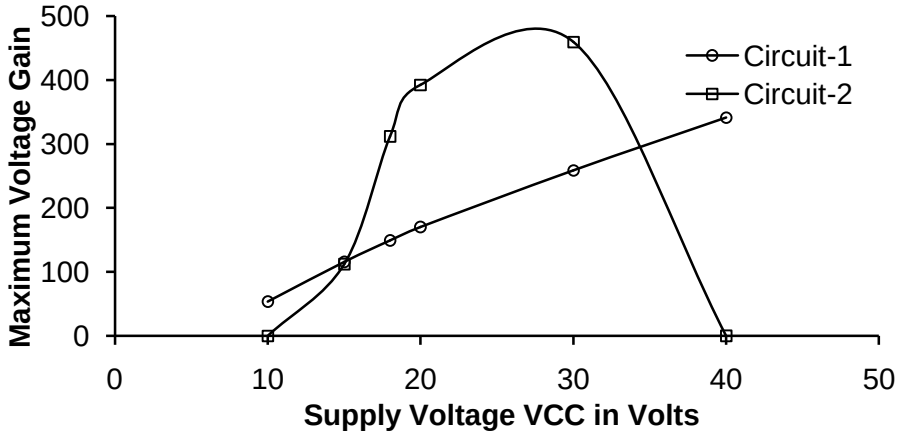

Fig.4. Variation of Maximum Voltage gain with Supply Voltage V_{CC}

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Variation of maximum voltage gain A_{VG} with DC supply voltage V_{CC} is depicted in Fig.4. Voltage gain of the reference amplifier rises almost linearly at increasing values of V_{CC} but for proposed amplifier it increases non-linearly from 10V to 30V of V_{CC}, thereafter, drops to a lowest point at V_{CC}=40V [15]. The permissible range for the reproduction of the amplified output at different V_{CC} for reference amplifiers (Circuit-1) is 10-40V whereas this range is substantially reduced to 15-30V for proposed amplifier. This is perhaps due to MOSFET driven Triple Darlington unit of the proposed amplifier which bears a threshold voltage of 2.831V along with a high driving voltage at node 3. This driving voltage (at node 3) increases with V_{CC} and reaches to 13.045V at 30V of V_{CC}. This simply means that the MOSFET conducts for a driving voltage range of 2.831-13.045V corresponding to 10-30 volts of V_{CC}. As V_{CC} increases beyond 30V, the compound unit receives a better flow of electrons from source to drain. V_{CC} exerts a heavy attractive force on electrons entering the drain from the channel region [14]. So beyond V_{CC} >30V, the drain absorbs more electrons than the channel could supply. As a result, the channel completely pinches-off and thus subsequent increase in V_{CC}>30V has minor effect on output voltage [14]. This caused the voltage gain to be rolled-off.

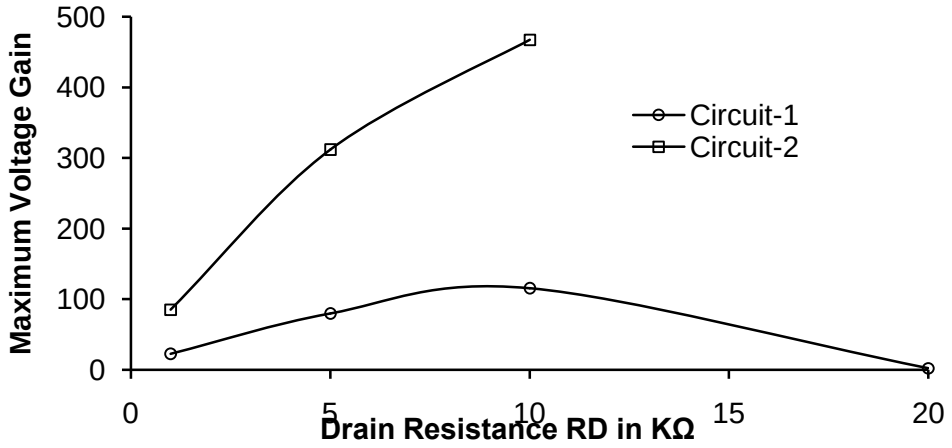

Fig.5. Variation of Maximum Voltage gain with Drain Resistance R_D or R_{CD}

Maximum voltage gain highly depends on drain resistance [10], [13]-[15]. Its variation with R_{CD} or R_D is depicted in Fig.5. For reference amplifier, the voltage gain gradually increases with R_{CD} and attains maxima at R_{CD}=10KΩ, thereafter, falls down rapidly and produces a distorted output beyond 20KΩ. However, for proposed amplifier, the voltage gain increases with R_D and attains a maximum at R_D=10KΩ, thereafter, the circuit starts producing a distorted output.

Variation of maximum voltage gain with load resistance R_L is also studied for both the amplifiers under discussion (but not shown in form of graphs). It is observed that the voltage gain gradually rises up to 100KΩ value of R_L for both the amplifiers and then tends toward a saturation tendency at higher R_L. This rising and saturation of the voltage gain with R_L is found well in accordance of the usual behaviour of small signal amplifiers [2], [4]-[15].

Total Harmonic Distortion (THD) percentage for both the amplifiers under discussion is also calculated using established rules [10]-[12], [17]. Reference amplifier holds 3.48% THD for 8 significant harmonic terms whereas proposed amplifier shows only 1.28% THD for 10 significant harmonic terms [15]. In fact, MOS driven composite unit of the proposed amplifier virtually acquires the property of a MOSFET. The fast switching property of this virtually behaved MOS composite unit perhaps reduces the propogation delay between positive and negative half cycles of the output waveform. This decreases the distortion in output waveform and causes THD of the proposed amplifier to reduce to a significant limit.

During the course of qualitative analysis of the proposed amplifier, some interesting observations are received. When the biasing resistance R_1 and/or R_2 is removed from Circuit-2, the respective amplifier doesn't behave properly. Similarly, when drain of MOSFET M1, of the proposed amplifier is detached from V_{CC} (node-4) and connected to node-5, the voltage gain falls to 265.586, bandwidth to 1.737KHz and current gain to 3.25K whereas THD increases to 4.23%. However, when collector of BJT Q1 of the proposed amplifier is detached from V_{CC} (node-4) and connected to node-5, the voltage gain falls to 282.977, bandwidth raised to 11.515KHz and current gain drops to 12.879K whereas THD reduces to 1.07%. Moreover, if M1 and Q1 of the proposed amplifier are simultaneously removed from V_{CC} and connected to node-5, the voltage gain falls to 243.745, bandwidth to 1.836KHz and current gain to 3.113K whereas THD increases to 4.18%.

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Variation of voltage gain, current gain and bandwidth with temperature is also measured and listed in TABLE II. Voltage gain and bandwidth gradually decreases whereas current gain increases throughout the rising temperature for reference amplifier [15]. However, for proposed amplifier, voltage gain, current gain and bandwidth decreases with rising temperature. In fact, the mobility of majority carriers of the semiconductor decreases at elevated temperature due to higher collision rate between them and the ions [18]. This decreases the drain current and therefore the current and voltage gains of the proposed amplifier. Similarly, effective contribution to the source capacitance due to the presence of Triple Darlington compound unit increases with increasing temperature [19] which in turn reduces the bandwidth.

TABLE II
VARIATION OF A_{VG}, A_{IG} AND BANDWIDTH WITH TEMPERATURE

Temperature (°C)	Circuit-1			Circuit-2		
	A_{VG}	A_{IG}	Bandwidth	A_{VG}	A_{IG}	Bandwidth
-30	120.142	31.488	23.312 KHz	338.311	14.932K	10.228 KHz
-20	119.305	32.261	23.102 KHz	332.871	14.740K	10.117 KHz
-10	118.474	32.982	22.917 KHz	327.795	14.559K	9.866 KHz
0	117.655	33.653	22.820 KHz	323.042	14.388K	9.850 KHz
10	116.851	34.278	22.604 KHz	318.582	14.226K	9.817 KHz
27	115.522	35.242	22.258 KHz	311.593	13.971K	9.665 KHz
50	113.811	36.370	21.885 KHz	303.150	13.658K	9.475 KHz
80	111.733	37.583	21.294 KHz	293.560	13.298K	9.234 KHz

TABLE III
VARIATION OF A_{VG}, AND BANDWIDTH WITH LOAD CAPACITOR C_L AND SOURCE CAPACITOR C_{SR}

Capacitance	Circuit-2: Load Capacitor C_L				Circuit-2: Source Capacitor C_{SR}			
	A_{VG}	f_L	f_H	Bandwidth	A_{VG}	f_L	f_H	Bandwidth
1pF	311.59	151.12Hz	9.82KHz	9.66KHz	3.266	10.68Hz	97.46KHz	97.45 KHz
1nF	310.36	150.16Hz	8.25KHz	8.10KHz	3.266	10.69Hz	101.08KHz	101.07KHz
50nF	263.26	118.89Hz	1.15KHz	1.04KHz	67.00	35.94KHz	80.52KHz	44.57KHz
100nF	227.83	100.08Hz	730.9Hz	630.81Hz	111.68	27.47KHz	54.37KHz	26.89KHz
1uF	66.03	42.22Hz	260.7Hz	218.49Hz	264.35	7.732KHz	19.62KHz	11.89KHz
10uF	7.936	25.09Hz	214.8Hz	189.75Hz	306.61	1.322KHz	11.19KHz	9.87KHz
100uF	0.805	23.40Hz	210.2Hz	186.80Hz	311.59	151.02Hz	9.816 KHz	9.66KHz

Load capacitor C_L (physically not shown in Circuit-2) and source capacitor C_{SR} considerably affects the performance of proposed amplifier [14]. TABLE III comprises the variation of A_{VG}, A_{IG} and Bandwith with C_L and C_{SR} respectively. The maximum voltage gain A_{VG} reduces appreciably if load capacitor C_L is large. Similarly, lowering the value of C_L causes mid-band frequency range to get wider. In addition, lower and upper cut-off frequencies shift towards lower side on the frequency scale at elevated values of C_L [14]. However, as source capacitance C_{SR} is increased, the voltage gain of the proposed amplifier increases but bandwidth decreases [14]. Moreover, shifting of lower and upper cut-off frequencies towards low frequency side on the similar pattern as was observed for C_L.

IV. CONCLUSIONS

A Triple Darlington configuration with two MOSFETs and a BJT is used to explore a new circuit model of RC coupled small-signal amplifier. This amplifier can effectively process small-signals swinging in 1- 10mV range of input signal at 1KHz frequency and is also free from the problem of poor response of small-signal Darlington pair or Triple Darlington amplifiers at higher frequencies. With narrow range bandwidth, the proposed amplifier generates only 1.28% harmonic distortion and simultaneously produces high voltage and current gains. Presence of load capacitor C_L and source capacitor C_{SR} considerably affects the performance of proposed amplifier whereas high voltage as well as current gain logically sets its power gain greater than unity. Presence of additional biasing resistances R_A and/or R_{AD} in proposed amplifier is essential to maintain its high voltage and high current gain features. The proposed amplifier produces 180^o phase shifted output with an optimal performance for 15-30V DC supply voltage. Collectively, these features make the proposed circuit fabulously unique in the category of small-signal amplifiers based on Darlington's topology.

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