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Small-signal Amplifier with Three Dissimilar Active Devices in Triple Darlington Topology

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Abstract: A new circuit model of a small-signal amplifier is proposed and analyzed on the qualitative scale. Apart from routine biasing components, the proposed amplifier circuit uses two additional biasing resistances and three dissimilar active devices namely MOSFET, JFET and BJT in Triple Darlington configuration. Having a considerably low amount of distortion (0.71%), the proposed circuit successfully amplifies small-signals of 1-5mV range (at 1 KHz frequency) and simultaneously provides high voltage gain (189.846) and high current gain (16.542K) with moderate range bandwidth (369.529KHz). These properties offer a flexible application range to the proposed circuit as high voltage gain or high current gain or high power gain amplifier in permissible audio-frequency range. Variations in voltage gain as a function of frequency and different biasing resistances, temperature dependency of performance parameters, bandwidth and total harmonic distortion of the amplifier are perused to provide a wide spectrum to the qualitative studies. Qualitative performance of the proposed amplifier is also compared with two different circuits which are respectively having BJT-JFET and BJT-MOSFET in Darlington pair configuration. The proposed amplifier may be useful for those applications where high voltage and current gain would be the prime requirement of amplification in audio frequency region.

Key words: Small-signal amplifiers, Darlington amplifiers, Compound configurations, Triple Darlington configuration

I. INTRODUCTION

One of the important concepts in electronics is the process of amplification through various active devices [1]-[2]. Virtually most of the electronic systems (analog, digital, or a hybrid combination of analog and digital) require amplifiers for scaling signals to a useful level [1]-[3]. The output signals from these systems are often too small in magnitude to be processed reliably for executing any useful function [2]-[4]. A Darlington pair, which is basically a composite unit of two similar transistors, can successfully amplify these signals [1]-[7]. It has superior characteristics regarding current gain due to which it is generally employed for the design of output stages in operational amplifiers [3]-[4]. However, a major drawback is encountered with its performance. At higher frequencies its response becomes poorer than that of a single transistor amplifier [3]-[7]. To overcome this problem, a number of modifications are attempted in Darlington pair amplifiers either by adding some extra biasing resistances in the circuit or by using Triple Darlington topology [5], [7]-[10]. However, use of dissimilar active devices or hybrid combination of active devices in Darlington's topology is still an area of electronic circuit designers to work with [8], [11]-[12].

The present investigation is focused around the use of a hybrid combination of MOSFET, JFET and BJT in Triple Darlington topology. This configuration with two additional biasing resistances is explored as new circuit model of a small-signal amplifier. The proposed amplifier circuit can be used in those radio and TV receiver stages which require high voltage gain, high current gain and moderate range bandwidth as a prime feature.

The present exploration is described in four sections. Section I gives the preface and the idea behind the present findings. Section II describes the detail of circuit configuration of the amplifiers under discussion. Section III contains the observational details and related discussions whereas the last section IV concludes the proposed work followed by references.

II. EXPERIMENTAL CIRCUITS

Present investigation starts with two differently configured small-signal amplifier circuits which are respectively consisting compound units of BJT-FET and BJT-MOSFET in Darlington pair [8], [12]. These circuits are depicted herein as Circuit-1 and Circuit-2 respectively and are treated as reference amplifiers for comparing with the qualitative performance of proposed amplifier. However, the proposed amplifier as depicted in form of Circuit-3, is obtained by using a compound assembly of

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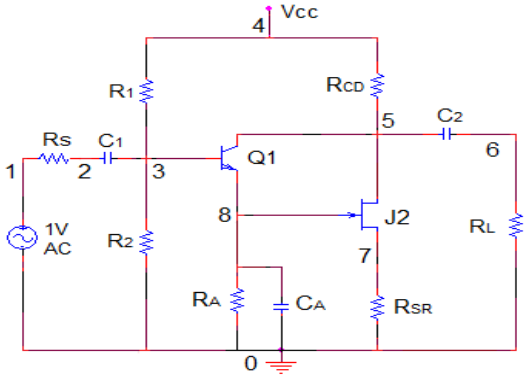
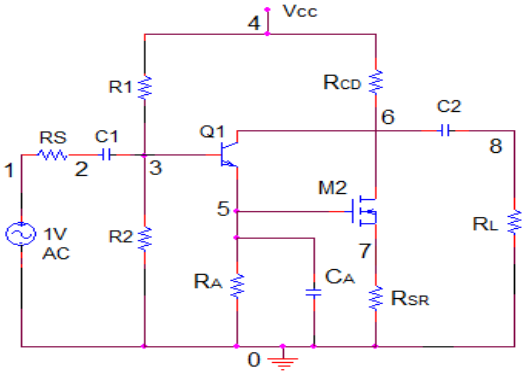
MOSFET, FET and BJT in Triple Darlington configuration [11]. Unlike reference amplifiers, the drain points M1 and J2 in proposed amplifier are directly connected to the biasing supply V_{CC}. In addition, two additional biasing resistances R_A and R_{AD} are incorporated in the proposed amplifier (Circuit-3) along with the bypass capacitor across emitter resistance. All the three amplifier circuits are properly biased using potential divider network with biasing parameters as described in Table I.

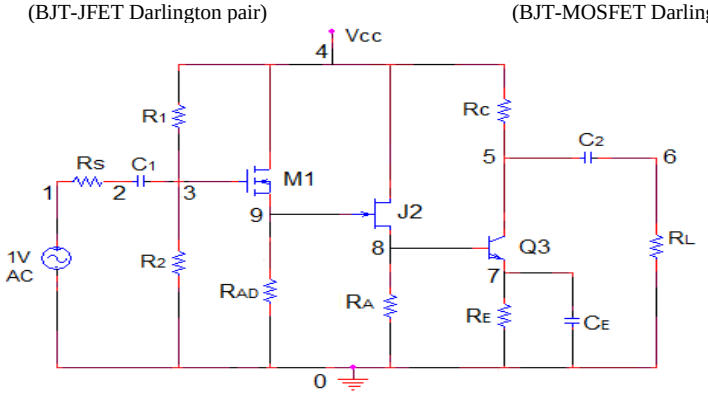
The amplifiers under discussion are biased with +15V DC power supply. Respective observations are made by feeding the amplifier circuits with 1V AC input signal source from which, a small and distortion less AC signal of 1mV for all the three amplifiers at 1KHz frequency is drawn as input for the amplification purpose. All the observations mentioned in the present manuscript are furnished through PSpice simulation software [3]-[5], [7], [9]-[13] (Student version 9.2).



Circuit.1: High voltage gain amplifier
(BJT-JFET Darlington pair)



Circuit.2: High voltage gain amplifier
(BJT-MOSFET Darlington pair)



Circuit.3: Proposed amplifier with High voltage gain and Wide bandwidth
(MOSFET-JFET-BJT in Triple Darlington Configuration)

TABLE I
COMPONENT DETAILS OF THE CIRCUITS UNDER DISCUSSION

COMPONENTS	DESCRIPTION	Circuit-1 BJT-JFET	Circuit-2 BJT-MOSFET	Circuit-3 MOSFET-JFET-BJT
Q1 / M1	NPN BJT (β=255.9)/N-MOSFET	Q2N2222	Q2N2222	IRF150
J2 / M2	N-Channel JFET (V_{TH}= -1.422)/ N-MOSFET	J2N3819	IRF150	J2N3819
Q3	NPN BJT (β=255.9)	Not available	Not available	Q2N2222
R_S	Source Resistance	500Ω	500Ω	250Ω
R_1	Biasing Resistance	47KΩ	47KΩ	4.7MΩ
R_2	Biasing Resistance	5KΩ	5KΩ	1.4MΩ
R_{CD}	Collector/Drain Biasing Resistance	5KΩ	10KΩ	10KΩ
R_E / R_{SR}	Emitter/Source Biasing Resistance	2KΩ	2KΩ	1KΩ
R_A	Added Biasing Resistance	1KΩ	1KΩ	10KΩ
R_{AD}	Added Biasing Resistance	Not available	Not available	10KΩ
R_L	Load Resistance	10KΩ	10KΩ	10KΩ
C_1 , C_2	Coupling Capacitors	1μF	1μF	1μF
C_A/C_E	Emitter By-pass Capacitor	10μF	10μF	100μF
Supply	DC Biasing Supply	+15V DC	+15V DC	+15V DC
AC Signal	Input AC Signal range for distortion-less output at 1KHz input frequency	1-15mV (1KHz)	1-15mV (1KHz)	1-5mV (1KHz)

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III. OBSERVATIONS AND DISCUSSIONS

Amplifiers of Circuit-1 and Circuit-2 provide fair and distortion-less results in 1-15mV range of AC input signals whereas for proposed amplifier of Circuit-3, it is received in 1-5mV range. However, the performance of the amplifiers are observed and discussed at 1mV, 1 KHz AC input signal.

Variation of maximum voltage gain as a function of frequency for all the three amplifiers are depicted in Fig.1. It is found that the amplifier of Circuit-1 produces 79.965 maximum voltage gain, 23.925 maximum current gain, 749.391KHz bandwidth (with lower cut-off frequency f_L=475.459Hz and upper cut-off frequency f_H=749.867KHz), 7.213µA peak output current and 72.132mV peak output voltage. However, amplifier of Circuit-2 produces 115.522 maximum voltage gain, 35.242 maximum current gain, 22.258KHz bandwidth (with f_L=443.567Hz and f_H=22.702KHz), 10.661µA peak output current and 106.607mV peak output voltage and the proposed amplifier of Circuit-3 produces 189.846 maximum voltage gain, 16.542K maximum current gain, 369.529KHz bandwidth (with f_L=66.315Hz and f_H=369.596KHz), 19.279µA peak output current and 192.786mV peak output voltage. Hence, it is clear that the bandwidth of proposed amplifier lies approximately midway of the bandwidth values of two reference amplifiers whereas maximum voltage and current gains are found to be considerably higher than both of them.

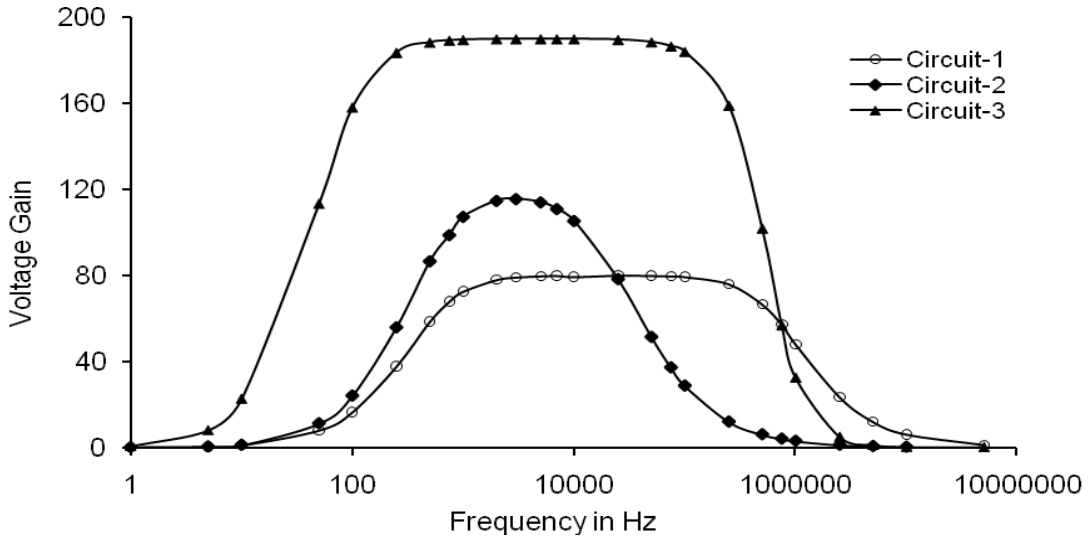

Fig.1. Variation of Voltage gain with frequency

In fact polarity of the composite unit of Darlington pair is determined by the driver device [14]. For example, a composite unit consisting BJT driver and JFET output (as in Circuit-1) will principally behaves like a BJT dominating Darlington unit. This is why the overall property of composite unit of the proposed amplifier seems to be inclined more towards MOSFET and motivates respective circuit to produce extra ordinarily high current gain. However, significantly high voltage gain of the proposed amplifier is perhaps due to the presence of complex combination of three dissimilar active devices and two additional biasing resistances in the circuit configuration.

It is to be noted that every amplifier under discussion shows phase reversal in respective output waveforms [5], [7]-[8], [12]. In fact, Common Emitter BJTs, Common Source FETs and Common Source MOSFETs independently produce phase reversal in their respective output waveforms [1]-[2], [8], [12]. This phase switching property of independent active devices is responsible to produce 180^o phase difference in the output waveform of reference and proposed amplifiers which are using composite unit of BJT-JFET, BJT-MOSFET and MOSFET-JFET-BJT in their respective circuit configurations [2]-[3], [5], [7], [10].

It is also worth mentioning that all the amplifiers under discussion effectively remove the problem of poor response of conventional Darlington pair or Triple Darlington amplifiers at higher order frequencies in the permissible frequency-response range [3], [5], [7], [10].

Maximum voltage gain of all the three amplifiers under discussion significantly depends on the added resistances. Dependency of maximum voltage gain on added resistances R_A or R_{AD} is graphically depicted in Fig.2. For reference amplifiers (Circuit-1 and Circuit-2) voltage gain found its maximum at R_A=1KΩ and thereafter decreases almost exponentially at higher

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values of R_A. However for amplifier of Circuit-3, when R_A is constant and R_{AD} is varying, the maximum voltage gain shows a non-linear increase up to 10 KΩ, and then falls abruptly to its lowest value at 25KΩ. On the other hand, when R_{AD} is constant and R_A is varying, voltage gain gradually increases to its maximum at 15 KΩ, and then starts decreasing with a slow pace.

Variation of maximum voltage gain with Source/Emitter resistance is shown in Fig.3. For reference amplifier of Circuit-1, the maximum voltage gain increases up to 2KΩ value of R_E then tends toward sustained level. It indicates that this reference amplifier provides optimum performance for $R_E \geq 2K\Omega$. However, the increasing values of source resistance R_{SR} for reference amplifier of Circuit-2 do not affect the voltage gain. It is also noticed here that if source resistance of this reference amplifier (Circuit-2) is removed, maximum voltage gain, maximum current gain and THD of the circuit rises fractionally and reaches to 115.872, 35.288 and 3.50% respectively while its bandwidth reduces to 21.458 KHz (with f_L=449.388Hz and f_H=21.908KHz). Conclusively, removal of R_{SR} from the Circuit-2 hardly affects the performance of amplifier.

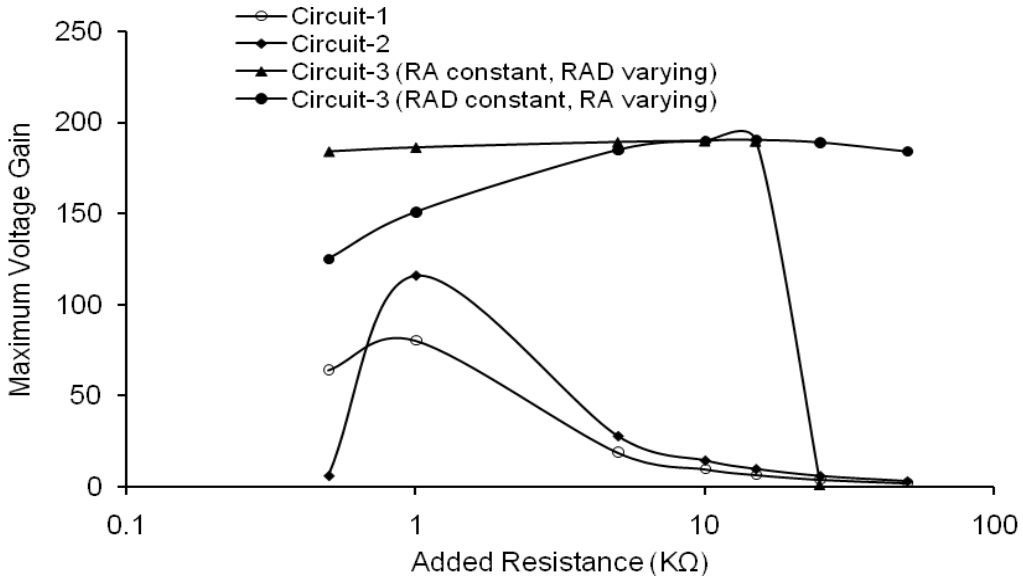

Fig.2. Variation of Maximum voltage gain with added resistance

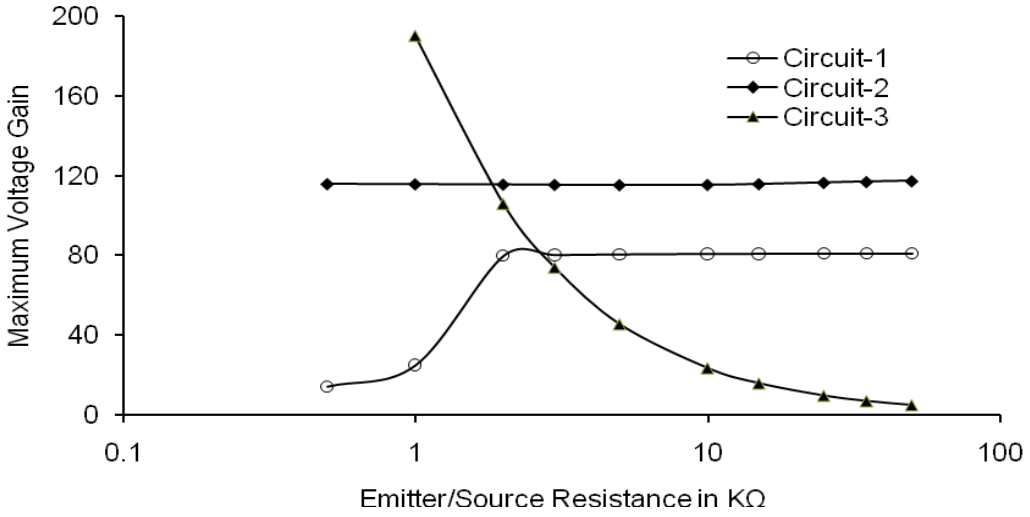

Fig.3. Variation of Maximum voltage gain with R_E or R_{SR}

Simultaneously, at increasing values of emitter resistance, the maximum voltage gain of the proposed amplifier (Circuit-3) decreases almost exponentially from 189.846 (at 1KΩ) to 4.893 (at 50KΩ). Since the resistance R_E in the proposed amplifier

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circuit virtually behaves as source resistance for MOS driven composite unit therefore the source degeneration property of common source MOSFET amplifier forces voltage gain to fall almost exponentially with R_E (Fig.3). More or less the similar situation persists for additional biasing resistance R_{AD} which causes maximum voltage gain to fall rapidly after a critical limit of 25KΩ (Fig.2).

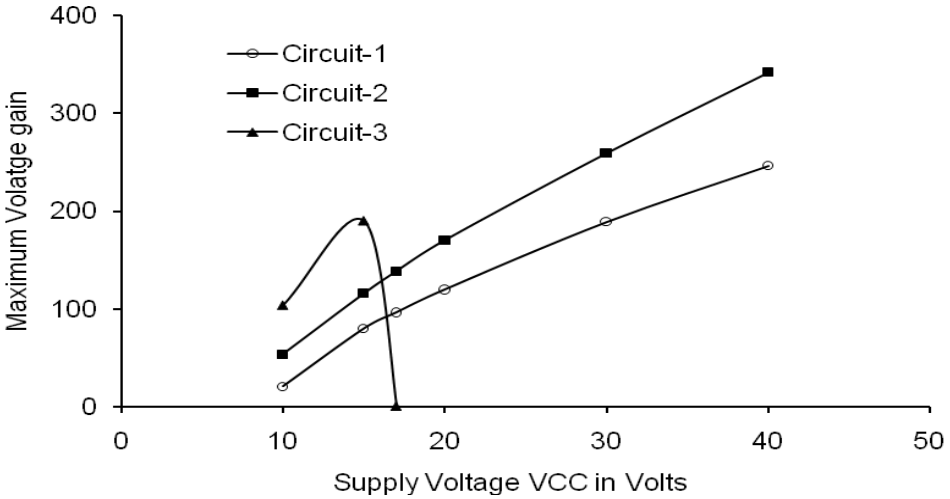

Fig.4. Variation of Maximum voltage gain with DC supply voltage V_{CC}

Variation of maximum voltage gain with DC supply voltage V_{CC} is depicted in Fig.4. Figure suggests that voltage gain of all the amplifiers under discussion rises nonlinearly at increasing values of V_{CC} but that for proposed amplifier it drops to a lowest point at V_{CC}=17V. It is also observed that the permissible range of supply voltage for reference amplifiers (Circuit-1 and Circuit-2) is 10-40V while for proposed amplifier of Circuit-3, this range is substantially reduced to 10-17V. This is perhaps due to MOSFET driven Triple Darlington unit of the proposed amplifier which bears a threshold voltage of 2.831V along with a high driving voltage at node 3. This driving voltage (at node 3) increases with V_{CC} and reaches to 3.90V at 17V of V_{CC}. This simply means that the MOSFET conducts for a driving voltage range of 2.831-3.90V corresponding to 10-17 volts of V_{CC}. As V_{CC} increases beyond 17V, the channel width broadens and causes sudden enhancement in I_D. This in turn forces for an abrupt voltage drop across the load and distorts the frequency response curve.

During the course of qualitative analysis, authors attempted to study the performance of proposed amplifier (Circuit-3) by imposing some changes in the circuit configuration. Respective observations are listed below-

1. When the added resistance R_A is removed from the proposed amplifier (Circuit-3) opposite half cycles of the output voltage/current waveforms do not remain identical. Instead, the negative half cycle gets slightly suppressed and widen but the periodicity of positive and negative half cycles is retained and THD of the circuit increases in multifold. However, when the added resistance R_{AD} is removed from proposed amplifier (Circuit-3), the maximum voltage gain reaches below unity, THD increases to a little and the output waveform bears only 43.55^o phase difference instead of usual state of phase reversal.

2. It is also observed that when drain point of the MOSFET in proposed amplifier (Circuit-3) is detached from V_{CC} (node-4) and connected to node-5, the voltage gain falls to 169.421, bandwidth to 3.782KHz and current gain to 2.61K whereas THD increases to 2.01%. However when drain point of the JFET in proposed amplifier (Circuit-3) is detached from V_{CC} (node-4) and connected to node-5, the voltage gain falls below unity to a value 0.235. On the other hand if drain point of the MOSFET and JFET in proposed amplifier (Circuit-3) are simultaneously detached from V_{CC} and connected to node-5, the amplifier provides poor response at lower frequencies.

3. Similarly, when biasing resistance R_1 is removed from the proposed amplifier (Circuit-3), voltage gain falls to 121.076, bandwidth to 364.797KHz, current gain to 128.997 but THD increases heavily.

Variation of voltage gain, current gain and bandwidth with temperature is also measured and listed in Table II. Table indicates that voltage gain of reference amplifier of Circuit-1 gradually decreases at increasing temperature. However, current gain increases but bandwidth decreases to a critical point of temperature (50°C) and thereafter the obtained nature reverse itself. For reference amplifier of Circuit-2, voltage gain and bandwidth gradually decreases whereas current gain

increases throughout the rising temperature. On the other hand, for proposed amplifier (Circuit-3), voltage gain increases up to a critical limit of 27°C and then it reverses its nature. Similarly current gain also increases up to the critical limit (27°C) but decreases on 50°C, then again increases on 80°C and finally decreases on 100°C. However bandwidth decreases up to a critical limit of 50°C, then increases at 80°C and finally decreases at 100°C.

TABLE II
VARIATION OF VOLTAGE GAIN $A_{V\text{-}MAX}$, CURRENT GAIN $A_{I\text{-}MAX}$ AND BANDWIDTH WITH TEMPERATURE

Temperature (°C)	BJT-FET (Circuit-1)			BJT-MOSFET (Circuit-2)			MOSFET-FET-BJT (Circuit-3)		
	$A_{V\text{-}MAX}$	$A_{I\text{-}MAX}$	Bandwidth (KHz)	$A_{V\text{-}MAX}$	$A_{I\text{-}MAX}$	Bandwidth (KHz)	$A_{V\text{-}MAX}$	$A_{I\text{-}MAX}$	Bandwidth (KHz)
-30	82.815	21.20	791.38	120.142	31.488	23.312	184.429	16.18K	497.353
-20	82.300	21.75	785.11	119.305	32.261	23.102	185.756	16.27K	469.715
-10	81.788	22.27	778.63	118.474	32.982	22.917	186.904	16.35K	458.122
0	81.282	22.76	776.51	117.655	33.653	22.820	187.891	16.41K	434.432
10	80.785	23.21	767.38	116.851	34.278	22.604	188.728	16.47K	414.702
27	79.965	23.926	749.39	115.522	35.242	22.258	189.846	16.54K	369.529
50	78.913	24.76	743.47	113.811	36.370	21.885	186.771	16.30K	222.171
80	56.882	18.82	936.36	111.733	37.583	21.294	0.486	49.62K	490.369
100	50.365	17.18	1018	110.478	38.253	20.628	0.233	24.37K	464.434
120	46.513	16.31	1078	109.294	38.830	20.008	Distortion		

Variation of maximum voltage gain with load resistance R_L is also studied for all the three amplifiers under discussion (but not shown in form of graphs). It is observed that the voltage gain gradually rises up to 100KΩ value of R_L for all the three amplifiers and then tends toward a saturation tendency at higher R_L. This rising and saturation of the voltage gain with R_L is found well in accordance of the usual behaviour of small signal amplifiers [2], [4], [5], [7], [12].

Total Harmonic Distortion (THD) percentage for all the amplifiers under discussion is also calculated for 8 significant harmonic terms using established rules [12], [15]. It is found that the amplifiers of Circuit-1 and Circuit-2 show 3.75% and 3.48% THDs respectively whereas the proposed amplifier (Circuit-3) shows only 0.71% THD. In fact, MOS driven composite unit of the proposed amplifier virtually acquires the property of a MOSFET. The fast switching property of this virtually behaved MOS composite unit perhaps reduces the propogation delay between positive and negative half cycles of the output waveform. This decreases the distortion in output waveform and causes THD of the proposed amplifier to reduce to a significant limit.

IV. CONCLUSIONS

As a novel approach, three dissimilar active devices namely MOSFET, JFET and BJT are used in Triple Darlington configuration to explore a small-signal amplifier using RC coupling. This amplifier can effectively process small-signals ranging below 5mV at 1KHz in the frequency band of 66.315Hz to 369.596KHz.

The proposed small-signal audio amplifier (Circuit-3) is free from the problem of poor response of conventional small-signal Darlington pair or Triple Darlington amplifiers at higher order frequencies in the permissible frequency band.

With a moderate range bandwidth, proposed amplifier generates only 0.71% harmonic distortion and simultaneously produces high voltage and current gains of considerable value. High voltage as well as current gain logically sets its power gain greater than unity. All these features together make this amplifier fabulously unique in its class.

The proposed amplifier shows a considerable response in 0.5KΩ - 15KΩ range of additional biasing resistances R_{AD} and R_A. Its optimum performance is received for 10-17V DC supply voltage and voltage gain is observed maximum for 1KΩ value of emitter resistance R_E.

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BIOGRAPHY

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Susmrita Srivastava received her M.Sc. degree in Electronics from Department of Physics and Electronics of Dr. Ram Manohar Lohia Avadh University, Faizabad, U.P., India in 2008. Presently she is pursuing Ph.D. degree in Electronics and published 13 research papers on various topics of Circuit designing and simulation in International /National journals and Conference Proceedings.