

Space Vector Pulse Density Modulation Scheme For Multilevel Inverter With 18-sided Polygonal Voltage Space Vector

Anilett Benny¹, Dr.T. Ruban Deva Prakash²

PG Student, Sree Narayana Gurukulam College of Engineering, Kadayiruppu, Kerala, India¹

Professor, Sree Narayana Gurukulam College of Engineering, Kadayiruppu, Kerala, India²

Abstract: Space Vector Based Pulse Density Modulated scheme for multilevel inverter is proposed in this paper. A two level and three level inverters with three different DC input voltages are used to produce 18 stepped output sinusoidal voltage. First order sigma delta modulator is used to obtain Pulse Density Modulation. The vector space is divided into 18 segments for spatial quantization. Sixty degree co-ordinate system is used to avoid fractional arithmetic. The proposed scheme uses only switching vectors which lie on the vertices of 18 sided polygon. The scheme uses only sector identification for selecting the switching vectors without using lookup table and timer. The proposed scheme with 18 sided polygonal multilevel inverter results in elimination of 5th, 7th, 11th and 13th order harmonics when compared to two level inverter schemes. Simulation results of the proposed scheme are compared with that of two level inverter schemes. From the results, the total harmonic distortion (THD) of the output voltage of SVPDM based 2-level inverter is 31.13% and the 18-sided multilevel inverter with SVPDM is 10.11%. From the results, the validity of the SVPDM based 18-sided multilevel inverter has been confirmed. Zero voltage switching can be incorporated in future for achieving high efficiency.

Keywords: Space vector pulse density modulation, multi-level inverter, two level inverter, harmonics, sigma delta modulator.

I. INTRODUCTION

Pulse density modulation (PDM) control method is applied in order to reduce the switching loss of the inverter side. In this method the density and the plus/minus of the constant width pulse is controlled, and then these pulse signals are used as switching pulses [5]. In general, delta-sigma conversion is used for analog-digital conversion. These PDM signals are used to turn on/off the inverter arm in PDM inverters. Delta-sigma conversion generates the inverse voltage pulses in order to cancel the quantization error. In order to resolve this problem, the PDM based SVM is proposed [6]. In PDM based SVM, the phase error between the voltage and current does not occur rapidly, because the SVM controller can select the switching pattern and hence the phase change on the voltage becomes smaller. Space vector based pulse density modulation (SVPDM) is proposed for two-level inverters. The total harmonic distortion in 2-level inverter is large.

Multilevel inverters have become more superior to conventional two level voltage inverters [1][2]. Different topologies of multilevel inverters are explained in literature [3], [7], [10]. SVPWM is commonly used [8] for generating switching pulses where the switching losses are more. Hence we propose SVPDM for multilevel inverter. Pulse density modulation scheme consists of a first order delta sigma modulator and a space vector quantizer [4]. 12-sided polygonal voltage space vector concept for PWM is proposed in [9]. In this paper, the principle of vector quantization is applied for 18 sided polygonal voltage space vector.

A two level inverter and a three level inverter feeding both ends of a load are used to produce the stepped output voltage. Three level inverter is made by cascading two 2 level inverters fed with asymmetrical voltages. The advantage of using multilevel inverters is the reduction of EMI and harmonics. Also the power circuit can be realised with low voltage devices and can be operated with low switching losses. The proposed 18 sided polygonal voltage space vector

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structure gives an increased modulation range with the absence of 5th, 7th, 11th and 13th harmonics from the output voltage [7]. So this scheme can be considered as available alternative for low and medium voltage high power drive applications.

II. SPACE VECTOR PULSE DENSITY MODULATION SCHEME

Fig. 1 represents proposed space vector pulse density scheme for multilevel inverter with 18 sided polygonal voltage space vector. The instantaneous values of three phase voltages are converted into reference voltage space vector V_{ref} . The instantaneous values are resolved into sixty degree (m-n) coordinate system (Fig. 2). The m-axis is placed along A phase. The transformation equations are given below:

$$V_m = \sqrt{\frac{2}{3}} (V_a - \frac{1}{2}V_b - \frac{1}{2}V_c)$$

$$V_n = \sqrt{\frac{2}{3}} (\frac{1}{2}V_a + \frac{1}{2}V_b - V_c)$$

$$V_0 = \sqrt{\frac{2}{3}} (\frac{1}{\sqrt{2}}V_a + \frac{1}{\sqrt{2}}V_b + \frac{1}{\sqrt{2}}V_c)$$

Each forward path consists of a first order sigma delta modulator consisting of a difference node, discrete time integrator, a quantizer and a digital to analog converter. The space vector quantizer consists of two parts, m-n to three phase voltage converter and a space vector quantizer.

The difference between reference space vector V_{ref} and analog estimate of quantizer output vector S_a is integrated to obtain error vector V_e in delta sigma modulator. The error vector is quantized to obtain switching sectors S . The m-n frame components are converted back to three phase voltages.

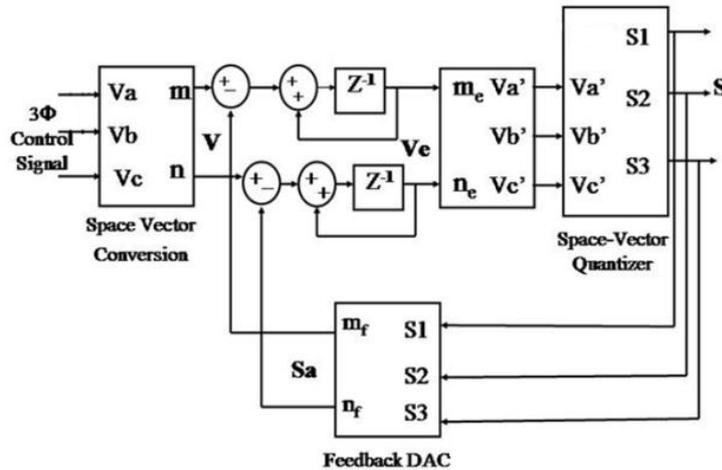


Fig. 1 Proposed vector quantized space vector pulse density modulator

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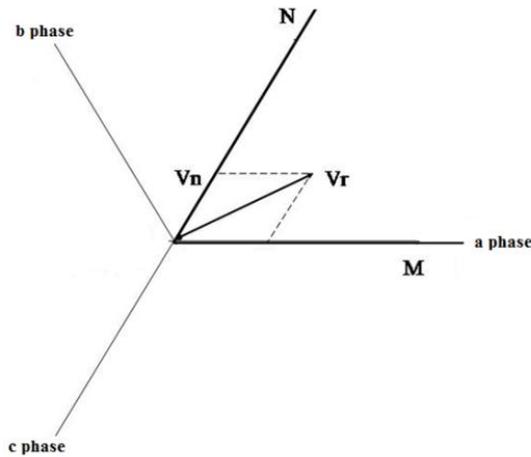


Fig. 2 abc to mn transformation

In space vector quantizer the three phase components are again converted to $\alpha\beta$ frame components (Fig.3) to produce the reference voltage vector and angle of sector selection using the transformation equations given below:

$$V_{\alpha} = \sqrt{\frac{2}{3}} \left(V_a - \frac{1}{2} V_b - \frac{1}{2} V_c \right)$$

$$V_{\beta} = \sqrt{\frac{2}{3}} \left(\frac{\sqrt{3}}{2} V_b - \frac{\sqrt{3}}{2} V_c \right)$$

$$V_{ref} = \sqrt{V_{\alpha}^2 + V_{\beta}^2}$$

$$\theta = \tan^{-1} \left(\frac{V_{\beta}}{V_{\alpha}} \right)$$

The sector in which the voltage space vector is located is determined (as per table-1) for finding out the multilevel inverter switching states.

TABLE-1 SECTOR SELECTION

θ°	SECTOR	VOLTAGE VECTOR
0-19	1	V1
20-39	2	V2
40-59	3	V3
60-79	4	V4
80-99	5	V5
100-119	6	V6
120-139	7	V7
140-159	8	V8
160-179	9	V9
180-199	10	V10
200-219	11	V11
220-239	12	V12
240-259	13	V13
260-279	14	V14

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280-299	15	V15
300-319	16	V16
320-339	17	V17
340-359	18	V18

The output voltage is fed back and converted to m-n frame components. The m and n components are added to delta sigma loop as shown in the figure.

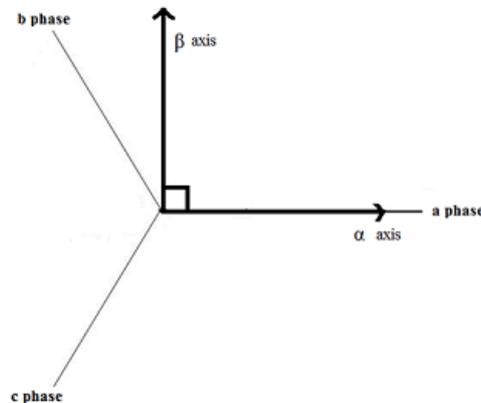


Fig. 3 'abc' to ' $\alpha\beta$ ' transformation

III. MULTILEVEL INVERTER WITH 18 SIDED POLYGONAL VOLTAGE SPACE VECTOR

Multilevel inverter to generate 18-sided polygonal voltage space vectors is shown in Fig.4. It consists of a 2-level inverter on one side and a 3-level inverter on the other side of load. The 3-level inverter is made by cascading two conventional 2-level inverters. Asymmetrical DC link voltages are used for the inverters.

For the proposed inverter we can achieve 6 different voltage levels in each winding. Therefore a total of $6^3 = 216$ switching states can be generated. Out of these switching states, vectors which lie on the vertices of 18 sided polygon are selected to generate 18-sided voltage space vector. Each pole A, B or C in INV1 can be independently connected either to $0.742V_{dc}$ or to the zero voltage. The poles A^1 , B^1 or C^1 of INV2 can be connected to any of three levels 0, $0.258V_{dc}$ or $0.395V_{dc}$ independently. This can be used to generate 18 polygonal voltage space vectors. The top and bottom switches in each leg of the inverter compliments to each other. The state of upper switch determines the state of lower switch.

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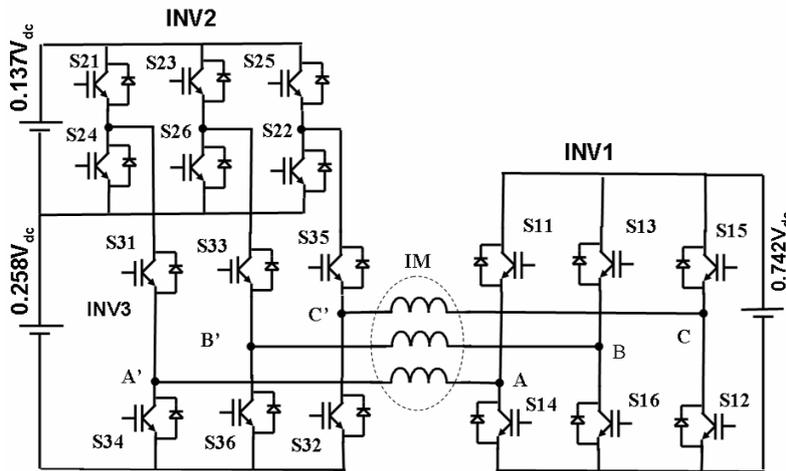


Fig. 4 Power circuit of inverter with 18 sided polygonal voltage space vector

The 18 voltage space vectors are shown in Fig.5. The angle between two adjacent voltage vectors is 20° . Resultant sum of vector OA and AB gives vector 1. In first segment INV1 produces vector OA by connecting the pole A to $0.742V_{dc}$. Vector AB has a magnitude of $0.258V_{dc}$ and is generated as shown in the Fig. 6. Pole voltages A^1 , B^1 , and C^1 of INV2 are subtracted from the pole voltages A, B, C of INV1. When B^1 is connected to $0.258V_{dc}$ it is along the negative B-axis and when C^1 is connected to $0.258V_{dc}$ it is along the negative C-axis. Their resultant is AB with magnitude $0.258V_{dc}$ along A-axis. The vectors AB and OA gives vector 1 of magnitude V_{dc} .

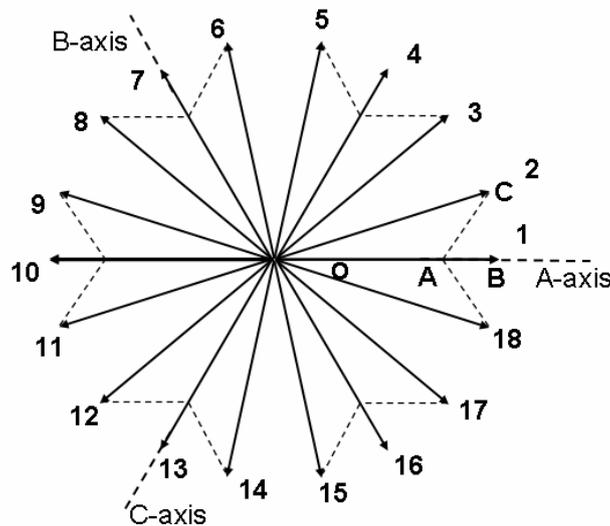


Fig. 5 18-polygonal voltage vectors

In the second sector, pole A of INV1 is connected to $0.742V_{dc}$, poles B and C at zero level. Hence vector OA is produced. Pole voltages A^1 and B^1 are at zero voltage levels and C^1 at $0.395V_{dc}$. Vector sum of the above vectors yields vector 2 in Fig. 7.

Vector-3 is generated as follows. In INV1 pole voltages A and B are maintained at $0.742V_{dc}$, while C is at $0V_{dc}$. Hence a vector is produced along the negative C-axis with a magnitude equal to $0.742V_{dc}$. In INV2 pole A^1 is at zero level

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while B^1 and C^1 are at levels $0.395V_{dc}$. This produces a vector with magnitude of $0.395V_{dc}$ along the positive A axis. Together the vector sum produces vector 3 in Fig.5.

TABLE -2 18-SIDED POLYGONAL VECTORS

Vector No.	Pole A	Pole B	Pole C	Pole A ¹	Pole B ¹	Pole C ¹
1	0.742Vdc	0	0	0	0.258Vdc	0.258Vdc
2	0.742Vdc	0	0	0	0	0.395Vdc
3	0.742Vdc	0.742Vdc	0	0	0.395Vdc	0.395Vdc
4	0.742Vdc	0.742Vdc	0	0	0	0.258Vdc
5	0.742Vdc	0.742Vdc	0	0.395Vdc	0	0.395Vdc
6	0	0.742Vdc	0	0	0	0.395Vdc
7	0	0.742Vdc	0	0.258Vdc	0	0.258Vdc
8	0	0.742Vdc	0	0.395Vdc	0	0
9	0	0.742Vdc	0.742Vdc	0.395Vdc	0	0.395Vdc
10	0	0.742Vdc	0.742Vdc	0.258Vdc	0	0
11	0	0.742Vdc	0.742Vdc	0.395Vdc	0.395Vdc	0
12	0	0	0.742Vdc	0.395Vdc	0	0
13	0	0	0.742Vdc	0.258Vdc	0.258Vdc	0
14	0	0	0.742Vdc	0	0.395Vdc	0
15	0.742Vdc	0	0.742Vdc	0.395Vdc	0.395Vdc	0
16	0.742Vdc	0	0.742Vdc	0	0.258Vdc	0
17	0.742Vdc	0	0.742Vdc	0	0.395Vdc	0.395Vdc
18	0.742Vdc	0	0	0	0.395Vdc	0

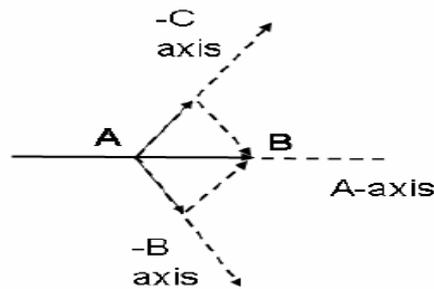


Fig. 6 Generation of voltage vector AB from INV2



Fig. 7 Generation of vector OC (OA+AC)

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IV. SECTOR IDENTIFICATION

The angle calculation in space vector quantizer is used to identify the sector. Depending upon the value of angle calculated in $\alpha\beta$ frame, one of the 18 sectors is selected and switching vector corresponding to that specific sector is applied to multilevel inverter.

TABLE-3 VOLTAGE LEVELS FOR 18 VECTORS

VECTOR	A	B	C	A ¹	B ¹	C ¹
1	1	0	0	0	1	1
2	1	0	0	0	0	2
3	1	1	0	0	2	2
4	1	1	0	0	0	1
5	1	1	0	2	0	2
6	0	1	0	0	0	2
7	0	1	0	1	0	1
8	0	1	0	2	0	0
9	0	1	1	2	0	2
10	0	1	1	1	0	0
11	0	1	1	2	2	0
12	0	0	1	2	0	0
13	0	0	1	1	1	0
14	0	0	1	0	2	0
15	1	0	1	2	2	0
16	1	0	1	0	1	0
17	1	0	1	0	2	2
18	1	0	0	0	2	0

Voltage level in A, B, C: 0=0 & 1=0.742V_{dc}; Voltage level in A¹, B¹, C¹: 0=0, 1=0.258V_{dc} & 2=0.395V_{dc}

TABLE-4 GATE PULSES FOR INVERTER SWITCHES

SECTOR AND VOLTAGE VECTOR →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
	SWITCH ↓																	
1	0	0	0	0	1	0	0	1	1	0	1	1	0	0	1	0	0	0
2	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0
3	0	0	0	0	1	0	1	1	1	1	1	1	1	0	1	0	0	0
4	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	1	1	1
5	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1
6	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
7	1	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
8	0	1	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
9	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0
10	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
11	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0
12	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	1

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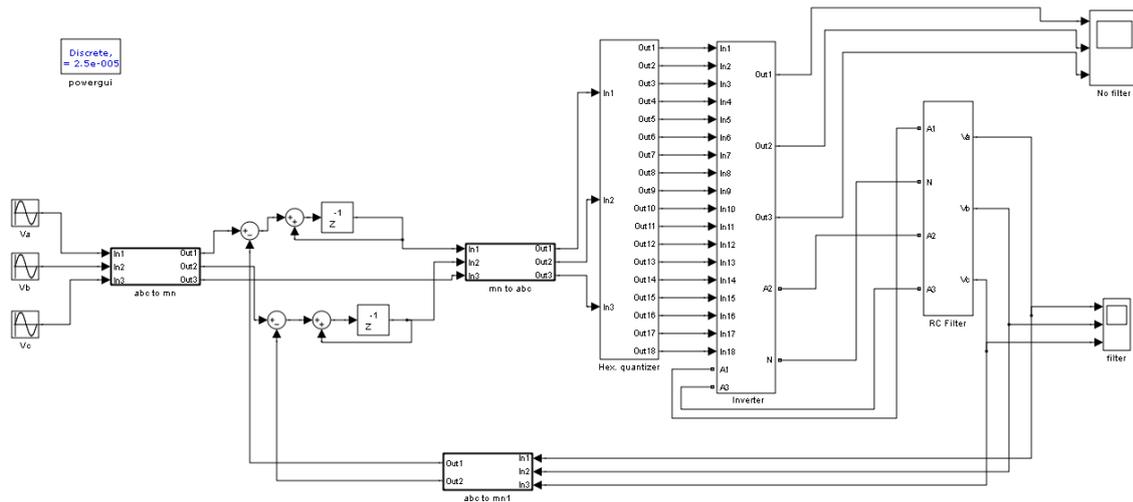
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13	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
14	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
15	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
16	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
17	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
18	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1

Gate pulses for each inverter switches are generated individually by calculating the voltage levels for each vector from table-3. Hence sector identification is performed. The switching pulses for inverter switches are shown in table-4.

V. SIMULATION RESULTS

The simulink model of the proposed SVPDM scheme for 18-sided multilevel inverter is shown in Fig.8. The inverter sub system is also shown in the figure. The simulink model of SVPDM for two-level inverter is shown in Fig.9.



(a)

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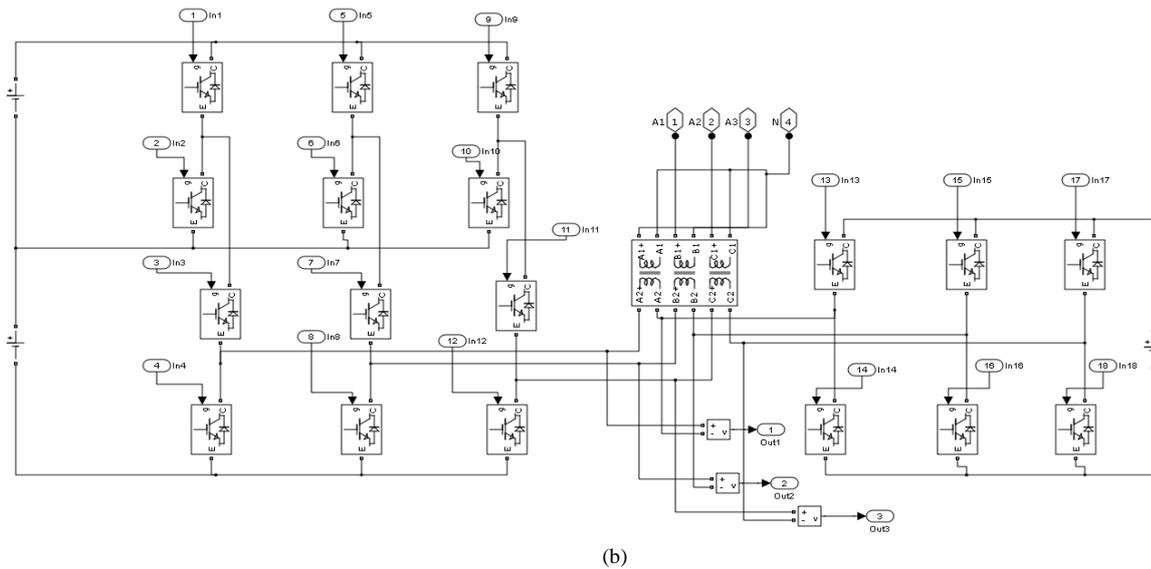


Fig. 8 Simulink model (a) Main model (b) 18-sided multilevel inverter subsystem

The phase voltage of 18-sided voltage space vector and its FFT analysis are shown in Fig. 10 and Fig. 11. The total harmonic distortion is found to be 10.11%. The phase voltage of two-level inverter with hexagonal quantizer and its FFT analysis are shown in Fig. 12 and Fig. 13. The total harmonic distortion is found to be 31.13%

From simulation results it is found that the phase voltage for multilevel inverter with 18 sided voltage space vector produces 18 stepped output waveform. For a two level inverter with hexagonal quantizer, the phase voltage is 6-stepped waveform. When harmonic analysis is performed, the proposed scheme with multilevel inverter is found to eliminate 5th, 7th, 11th and 13th order harmonics. The Total Harmonic Distortion (THD) factor for the proposed scheme is very less when compared with the two-level inverter with hexagonal quantizer.

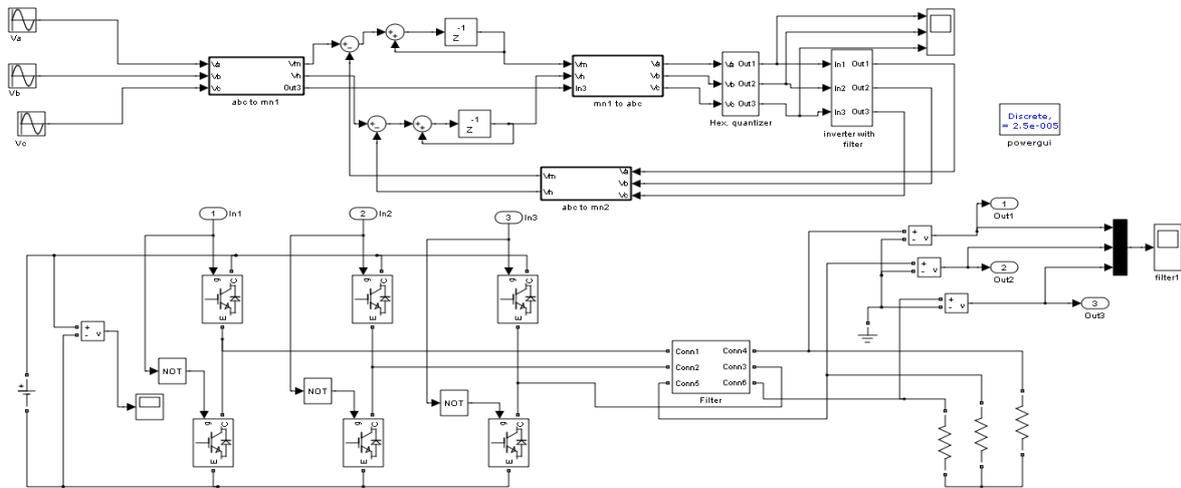


Fig. 9 Simulink model of SVPDM for 2-level inverter

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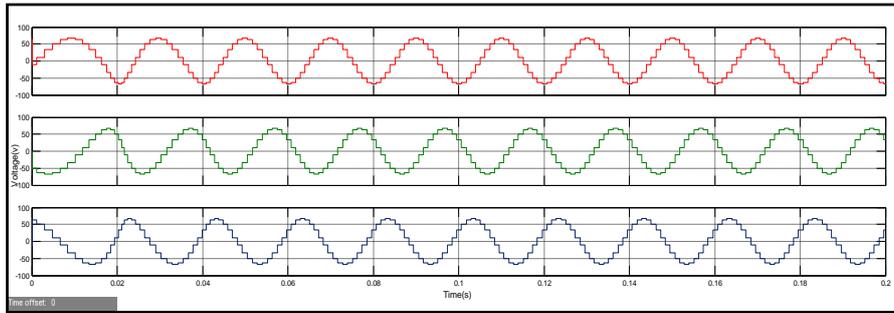


Fig. 10 Phase voltage of 18-sided voltage space vector for modulation index m=1

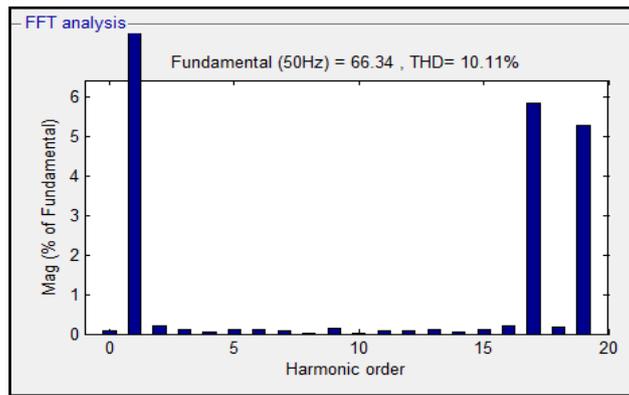


Fig. 11 FFT analysis of voltage waveform of 18-sided voltage space vector

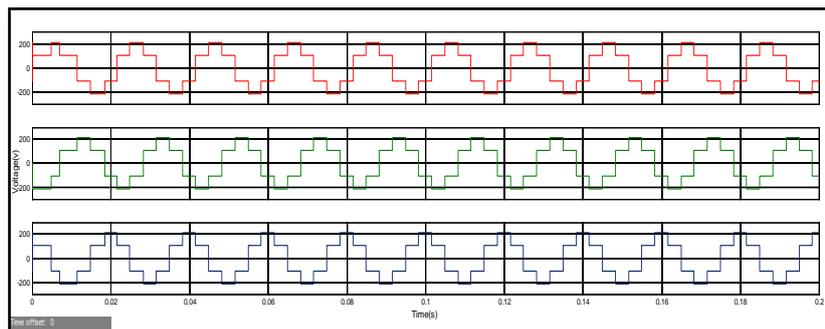


Fig.12 Phase voltage across load

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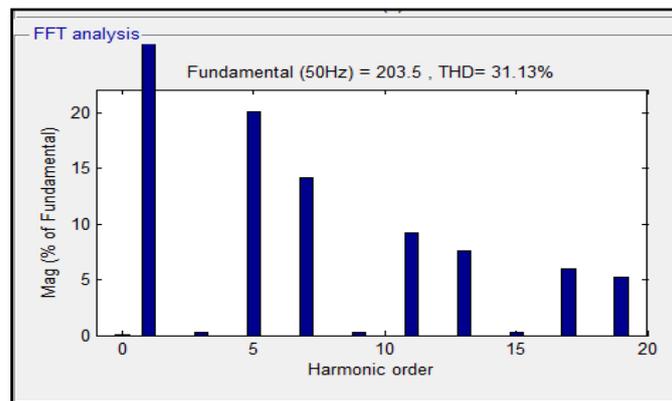


Fig. 13 FFT analysis of voltage waveform

V. CONCLUSION

An 18-sided multilevel inverter control scheme using space vector pulse density modulation is proposed. Sigma delta modulation and vector quantization principles are used in this scheme. The vector space is divided into 18 segments for spatial quantization. Sixty degree co-ordinate system is used to avoid fractional arithmetic. The proposed scheme uses only switching vectors which lie on the vertices of 18 sided polygon. The scheme uses only sector identification for selecting the switching vectors without using lookup table and timer.

Simulation studies are performed for SVPDM based 2-level and multilevel inverter with 18-sided voltage space vectors. Pulse density modulation scheme for multilevel inverter with 18 sided voltage space vector yields low switching losses and very less harmonic content as compared to pulse width modulation techniques in multilevel inverters. The proposed scheme can be implemented for multilevel inverter with 12 sided voltage space vectors. Zero voltage switching can be incorporated in future for achieving high efficiency. This scheme is simple and timing calculations for voltage vectors are eliminated.

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