ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

To Mitigate the Voltage Sag Using Diode Clamped Multi Level Inverter with DVR Technique

J. Shanmuga Priya[1], A.Kiruthiga[2], R.Vanithamani[3], M. Mahendiran[4]

Assistant Professor, Dept. of EEE, Sasurie Academy of Engineering, Coimbatore, India[1, 2, 3, 4]

Abstract— In this paper a Dynamic Voltage Restorer (DVR) based on a multi level inverter with energy storage devices is proposed. It describes the problem of voltage sag and swells and its severe impact on non linear loads or sensitive loads. The dynamic voltage restorer (DVR) has become popular as a cost effective solution for the protection of sensitive loads from voltage sags and swells. The control of the compensation voltages in DVR with diode clamped multilevel inverter and PDPWM technique is proposed. Multilevel inverters have become more popular over the years in high power electric applications without use of a transformer and with promise of less disturbance and reduced harmonic distortion. These Pulse Width Modulation (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PSPWM) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. The Total Harmonic Distortion (THD), V_{RMS} (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK.

Keywords— CF, DCMLI, FF, PWM, THD, V_{rms}

I. INTRODUCTION

Voltages in power distribution systems are commonly affected by disturbances. According to the Canadian Electric Associate (CEA) and the Electric Power Research Institute (EPRI), among various power quality problems the majority of events are associated with either voltage sag or a voltage. Such events are a common reason for failures in production plants, loads malfunctions, and economic losses. Many solutions to these problems have been published in recent years. The existing methods include matrix converter with DVR techniques. Using this technique efficiency reduced and harmonics are introduced. In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Depending on voltage levels of the output voltage, the inverters can be classified as two- level inverters and multi level inverters.

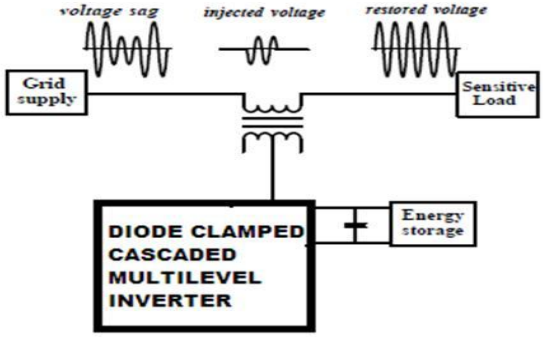

Fig 1. Principle of operation DVR

This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI fed IM employing

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

sinusoidal switching strategies. Simulations are performed using MATLAB- SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

II. MULTI LEVEL INVERTER

Numerous industrial application have begun to require higher power apparatus in recent years a multilevel power converters structure has been introduced as an alternative in high power and medium voltsge situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel converter system for a high power application. The concept of multilevel converter system has been introduced since 1975. The term multilevel began with the three level convertor. Subsequently, several multilevel converter topologies have been developed. In recent days the research on multilevel inverters has been widely increasing due to its capability of high power medium voltage application. In low level inverters the harmonic content of output current can be reduced by increasing the switching frequency. But the switching frequency is restricted by switching loss in high power and high voltage applications. In such applications multi level inverter has been used. Mostly there are three kinds of multilevel inverter they are Diode clamped inverter, Flying capacitor inverter and Cascaded multilevel inverter.

A. Diode Clamped Multilevel Inverter

A three-phase five level diode-clamped inverter is shown in fig 2. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is Vdc, and the voltage stress across each switching device is limited to Vdc through the clamping diodes. The increase of the voltage level, and the requirement of additional dc-link capacitors, makes the use of multipulse attractive. These types of rectifiers enable the desired voltage operation while reducing the input-current harmonics.

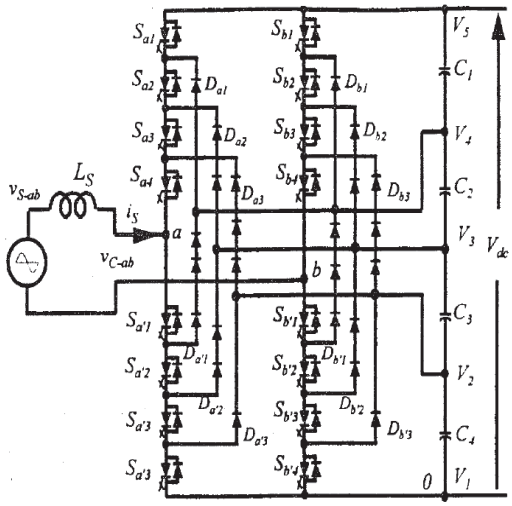

Fig 2. Five level diode clamped multilevel inverter

Table 1.lists the output voltage levels possible for one phase of the inverter with the negative dc voltage Vo as a reference. State 1 means the switch is ON, and 0 means the switch is OFF. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the complementary switch be turned off. The complementary switch pairs for the phase leg a are (sa1, sa'1), (sa2,sa'2), (sa3,sa'3), (sa4,sa'4) and (sa5,sa'5).Table also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series . For a six-level inverter, a set of five switches is on at any given time. Figure 4 shows one of the three line-line voltage wave forms for a six level inverter. The line voltage Vab consists of a phase leg a voltage and a phase leg b voltage. The resulting line voltage is an 11- level staircase waveform. This means that an M- level diode-clamped inverter has an m-level output phase voltage and a (2m-1) level output line voltage.

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

Sa_1	Sa_2	Sa_3	Sa_4	Sa_1'	Sa_2'	Sa_3'	Sa_4'	V_{an}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-
0	0	0	0	1	1	1	1	-

Table 1. Diode clamped five level inverter voltage and corresponding switching states

Although each active switching device is required to block only a voltage of Vdc, the clamping diodes require different ratings for reverse blocking. Using phase a of fig 3 as an example, 1 D4 must block four voltage levels, or 4Vdc. Compare to cascaded multi level inverter it is advantages process and produce less harmonics. Incresing the level of multi level inverter we can improve the efficiency.In this paper fifteen level diode clamped multi level inverter is used.

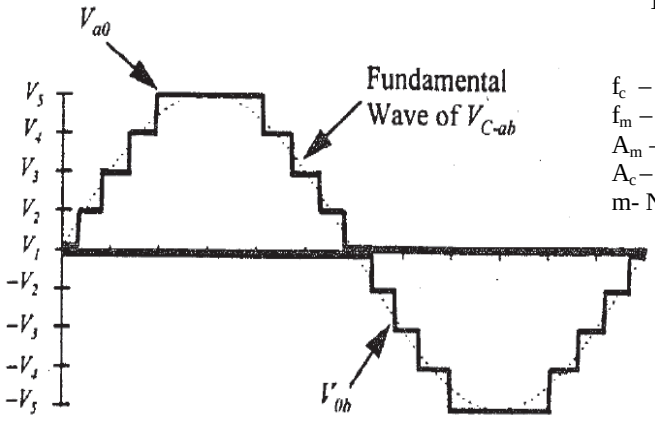

Fig 3. Output Voltage Of A Phase

Similarly, D3 must block 3Vdc, D2 must block 2Vdc, and D1 must block Vdc. If the inverter is designed such that each locking diode has the same voltage rating as the active switches , Dn will require n diodes in series; consequently, the number of diodes required for each phase would be (m-1)x(m-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter.

II. TRANSIENT VOLTAGE,NOISE,SAG AND UNDER VOLTAGE

A. *Phase Disposition PWM Strategy*

The rules for phase disposition method Fig 8. for a multilevel inverter are

1) 4 carrier waveforms in phase are arranged.
2) The converter is switched to + Vdc/2 when the sine wave is greater than both upper carrier.
3) The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
4) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.
5) The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.
6) The converter is switched to - Vdc/2 when the sine wave is less than both lower carrier.

The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD.

The frequency modulation index

$$m_f = f_c/f_m$$

The Amplitude modulation index

$$m_a=2A_m/(m-1)A_c$$

f_c – Frequency of the carrier signal.
f_m – Frequency of the reference signal.
A_m –Amplitude of the reference signal.
A_c – Amplitude of the carrier signal.
m- Number of levels.

Fig 4. Transient voltage

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

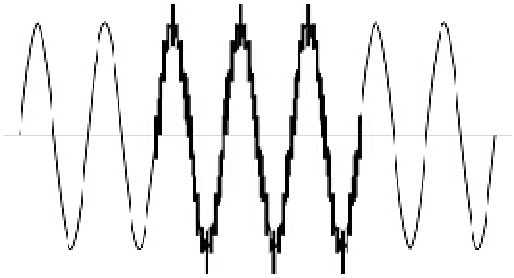

Fig 5. Noise voltage

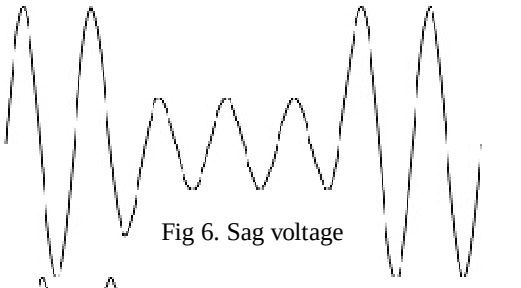

Fig 6. Sag voltage

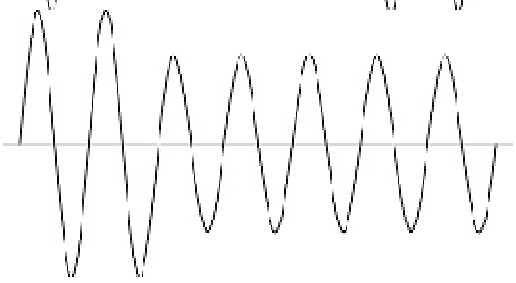

Fig 7. Under voltage

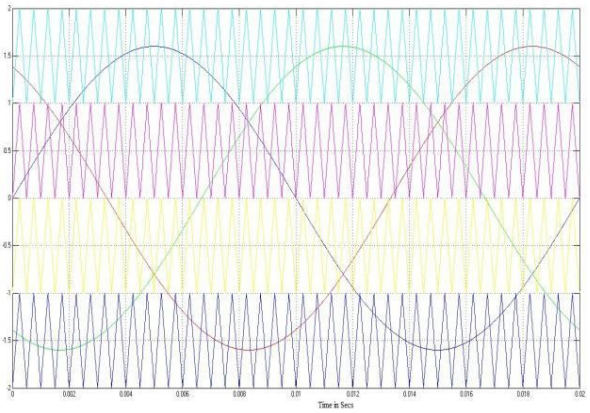

Fig 8. Carrier arrangement for PDPWM strategy

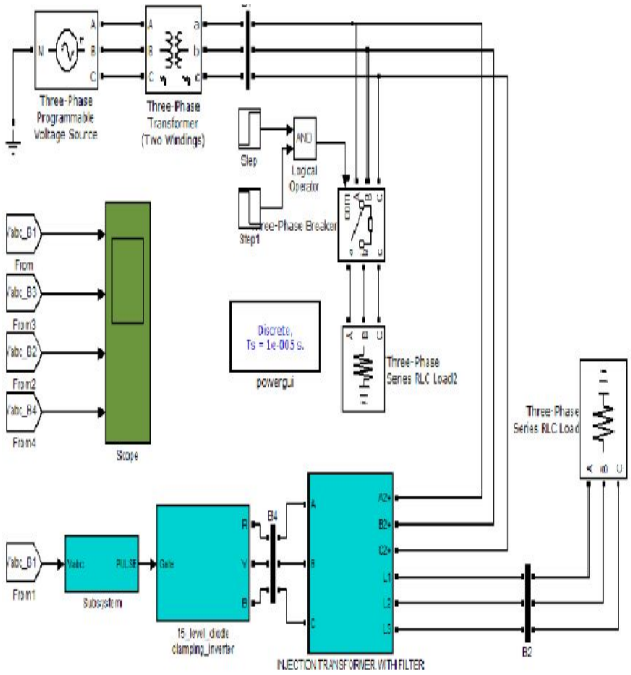

Fig 9. Proposed DVR system

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

Fig 9. shows the proposed DVR system. This consists of 15 level diode clamped multi level inverter and injection transformer with filter. When the grid supply produce the voltage sag in the load side and DVR start to inject the voltage. It will compensate the missing voltage and finally we get the pure sinusoidal wave form. According to the proposed topology (Fig. 10), even with a severe sag condition in the supply voltage, the inverter theoretically can inject as much as 90% of nominal voltage, by the proper control structure. Two control methods may generally be used for DVRs, being either open loop control, or closed loop control. The three phase diode clamped fifteen level inverter is modelled in SIMULINK using power system block set.

III. SIMULATION RESULTS

MATLAB is an interactive, matrix-based package for scientific and engineering numeric computation and visualization. It can solve complex numerical problems in a fraction of the time required. The name MATLAB is derived from MATrix LABoratory. To satisfy the specific needs for diversified engineering applications and to extend the functionality of the base program, MATLAB comes with a variety of tool boxes (collection of special files). The tool boxes are designed to serve various disciplines such as control, optimization, statistics, neutral networks, graphical user interface, signal processing, fuzzy logic, and many others. The number of different tool boxes increases with newer MATLAB.

IV. CONCLUSION

In this project dynamic voltage restorer and phase disposition pulse width modulation of diode clamped multi level inverters are discussed. This method is very simple in formulation, brings great flexibility to the series active filter design, and thus substantially broadens the solution space. MATLAB/simulink models were developed to examine the voltage sag in multi level inverters.

REFERENCES

[1] D.O. Koval and M. B. Hughes, "Canadian national power quality survey: Frequency of industrial and commercial voltage sags," IEEE Trans. Ind. Appl., vol. 33, no. 3, pp.622-627, May/Jun. 1997.

[2] D.D. Sabin, "An assessment of distribution system power quality," Elect. Power Res. Inst., Palo Alto, CA, Rep. TR-106294-V2, May 1996.

[3] Berrezzek Farid and Berrezzek Farid, "A Study of New Techniques of Controlled PWM Inverters", *European Journal of Scientific Research, ISSN 1450-216X,Vol.32, No.1*, 2009, pp.77-87.

[4] Anshuman Shukla, Arindam Ghosh and Avinash Joshi, "Control Schemes for DC Capacitor Voltages Equalization in Diode- Clamped Multilevel Inverter Based DSTATCOM", *IEEE Trans. on Power Delivery, Vol.23, No.2*, 2008, pp.1139-1149.

[5] Berrezzek Farid and Berrezzek Farid, "A Study of New Techniques of Controlled PWM Inverters", *European Journal of Scientific Research, ISSN 1450*-216X, Vol.32, No.1, 2009, pp.77-87.

[6] Engin Ozdemir, Sule Ozdemir and Leon M.Tolbert, "Fundamental-Frequency- Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand- Alone Photovoltaic System", *IEEE Trans. on Power Electronics, Vol.56, No.11*,2009, pp.4407-4415.

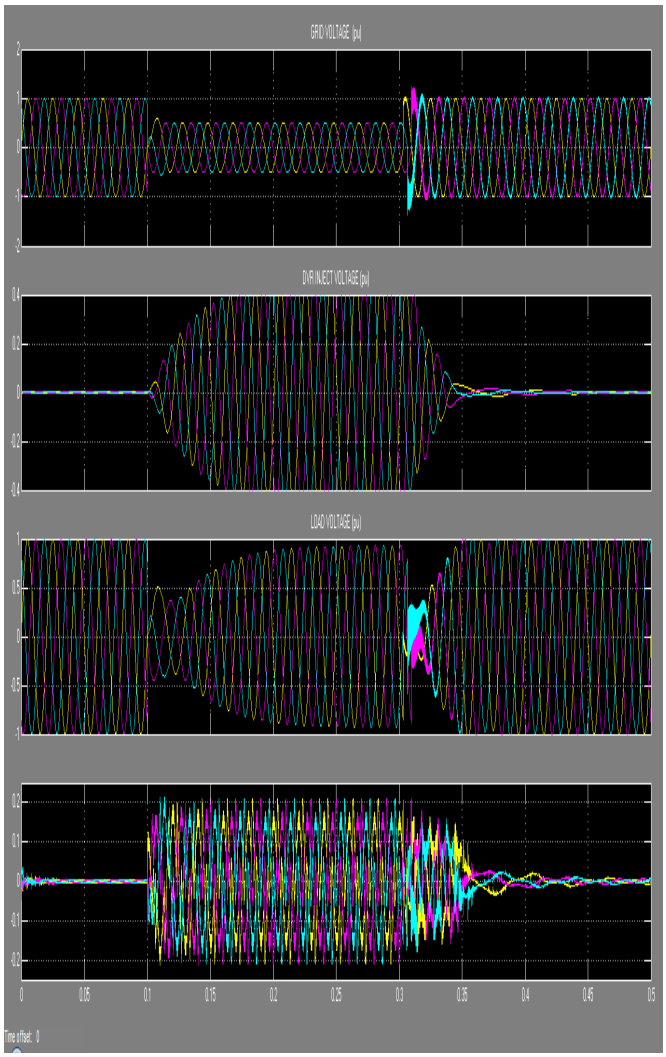

Fig 10. Output Waveform

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

[7] J.G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, " Control and testing of a dynamic voltage restorer (DVR) at medium voltage level,"IEEE Trans. Power Electron., vol. 19, no. 3, pp. 806-813, May 2004.

[8] J.G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump,"in *Proc. IEEE APEC'01*, vol. 2,2001, pp. 1267-1273.

[9] J. Perez, V. Cardenas, L. Moran, C.Nuñez, "Single-Phase AC-AC converter operating as a dynamic voltage restorer (DVR)," IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on, Nov 2006, pp. 1938-1943.

Jose M Lozano and Juan M.Ramirez, "AC-AC Converter for unbalanced supply,"19th International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Ischia, Italy, June 2008, pp. 54-59.