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6-Bit Charge Scaling DAC and SAR ADC

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ABSTRACT: A system which processes a signal is a combination of a number of mixed signal circuits, which require both analog and digital domain functions. To change from one domain to other, analog-to-digital (A/D) and digital-to-analog (D/A) converters are used. In this work, 1.1V, 6-bit charge scaling DAC using split array is designed and simulated. This design consists of parallel array of binary weighted linear capacitors to achieve high resolution as compared to other types of DACs. A 2:1 Multiplexer is designed to act as a switch and differential amplifier is designed to amplify the convoluted inputs in charge scaling architecture. The concept of split array is employed to reduce the total area of the capacitor required for high resolution DACs. Design uses 20fF, 40fF, 80fF capacitors to build charge scaling DAC. Design of charge scaling architecture using split array is implemented in cadence 90nm technology. Further Successive approximation register (SAR) ADC is designed using the binary weighted capacitor array as its DAC for charge redistribution purpose. Design of 1.2V, 6-bit SAR ADC is implemented using cadence at 90nm CMOS process, which consumes 802.6µW.

KEYWORDS: *Switch, DAC Logic, CMOS, op-amp, CADENCE, SAR ADC.*

I. INTRODUCTION

Analog-to-digital (A/D) conversion and digital-to-analog (D/A) conversion, lie at the heart of most modern signal processing systems. As digital signal processing (DSP) integrated circuits become increasingly sophisticated and attain higher operating speeds more processing functions are performed in the digital domain. In most of the electronic systems the input and output signals are analog in nature. Hence, there are analog processing devices like amplifiers as input and output devices. However most of the modifications to be carried out on the input signals before obtaining the outputs are carried out in digital domain. Therefore, there is a need to convert the analog input signals into digital signals at the input end, and after processing them in the digital domain, they have to be converted back into analog signals in most of the applications. The circuits that convert analog signals to digital signals are known as A/D Converters and the circuits that convert digital signals to analog signals are known as D/A Converters. Charge scaling DACs operate by binary dividing of the total charge applied to a capacitor array. This process is implemented by using capacitor to attenuate the reference voltage is shown in Figure 1. Advantage of charge scaling DAC is that it is compatible with switched capacitor circuits [1].

High resolution DACs have been investigated very intensely, due to very high demands for miscellaneous applications such as Analog to Digital Converters (ADC) as well as other industrial applications [2]. Depending on a

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specific request, many types of high resolution DACs have been introduced [1, 3]. In general they can be classified into two groups: calibrated and non-calibrated

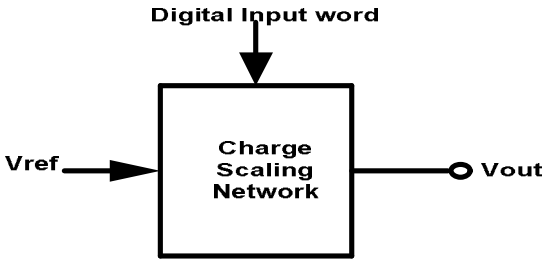

Figure 1. *General charge scaling DAC.*

DACs. The slower calibrated DACs are using dynamic element matching in order to achieve higher resolutions. On the other hand fast non-calibrated DACs feature, lower resolution as they rely only on matched components. They directly convert any digital code to an analog value. Due to limited matching and linearity performance of the basic device elements, using this kind of converters only up to 12-bit resolution can be achieved. Speed performance in data converters has traditionally been reached with bipolar technologies. However, recent advances in CMOS processes driven by the feature size reduction have led to a considerable improvement in the performance of CMOS devices. Deep sub-micron technologies are expected to improve further, the conversion speed, thus becoming competitive with Bi-CMOS technologies [2]. A new C-2C digital-to-analogue converter (DAC) has been investigated [4], which uses C and 2C capacitors. It is difficult to realize the C-2C DAC scheme on a silicon wafer because of the large parasitic capacitance. The C-2C DACs require considerably less area and power than conventional weighted capacitor (WC) DACs, and operate at a much higher conversion rate.

The DAC serves two purposes in a SAR converter: it samples the input charge and it generates an error voltage between the input and current digital estimate [5]. The conventional DAC choice is a binary-weighted capacitor array, which is insensitive to stray capacitance [6]. However, the conventional capacitor array uses charge inefficiently during the conversion. The split capacitor array has both the lowest switching energy and does not require an extra clock phase that would limit high speed operation.

The paper is organized as follows: Section I gives an introduction and brief literature survey. Section II deals with the basics of Charge Scaling DAC architecture. Section III details the design of 6-bit Charge Scaling DAC using split array. Section IV presents the design of SAR ADC, Section V gives the simulation results and Section VI conclusions.

II. CHARGE SCALING DAC

A very popular DAC architecture used in CMOS technology is the charge-scaling DAC. Shown in Figure 2, a parallel array of binary-weighted capacitors, totaling $2^N C$, is connected to an op-amp. The value, C, is a unit capacitance of

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any value. After initially being discharged, the digital signal switches each capacitor to either V_{ref} or ground, causing the output voltage,V_{out}, to be a function of the voltage division between the capacitors.

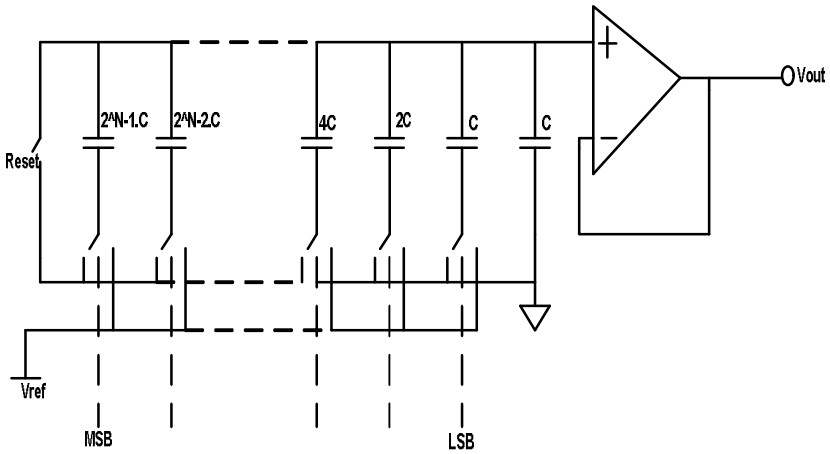

Figure2. *A Charge Scaling DAC.*

The capacitor array totals $2^N C$, therefore, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, V_{out}, becomes as in (1).

$$V_{out} = V_{ref} \cdot \frac{2^{N-1}C}{(2^{N-1}+2^{N-2}+\ldots+4+2+1+1)C} = V_{ref} \cdot \frac{2^{N-1}C}{2^N C} = \frac{V_{ref}}{2} \quad (1)$$

which confirms the fact that the MSB changes the output of a DAC to $(\frac{V_{ref}}{2})$. The ratio between V_{out} and V_{ref} due to each capacitor can be generalized to, (2).

$$V_{out} = \frac{2^K C}{2^N C} \cdot V_{ref} = 2^{K-N} \cdot V_{ref} \quad (2)$$

where it is assumed that the k^{th} bit, D_k, is one and all other bits are zero. Superposition can then be used to find the value of V_{out} for any digital input word by (3).

$$V_{out} = \sum_{k=0}^{N-1} D_k \, 2^{k-N} \cdot V_{ref} \quad (3)$$

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used

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technology to be implemented in VLSI chips [1].

III. 6-BIT CHARGE SCALING DAC USING SPLIT ARRAY

The 6-bit DAC is based on the charge scaling split array method. The block diagram of a 6-bit charge scaling DAC using the spilt array method is shown in Figure 3. This circuit converts a 6-bit digital input word to a respective analog signal by scaling a voltage reference that is obtained by the capacitive network. Various building blocks of Figure 3. are operational amplifier, capacitive network and multiplexer switches to which the digital word is given. Initially the input digital word is given to a multiplexer circuitry. Depending on the logic value of each bit of the word, the multiplexer chooses the particular voltage to which the capacitor is to be charged. If the input bit in the digital word is logic '0' then the multiplexer chooses input which is connected to the 'GND' and the capacitor is charged to 0 V. If the input bit in the digital word is logic '1' then the capacitor is charged to V_{ref} , which is 1.1 V.

The output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. LSB, b0, now corresponds to the leftmost switch and that the MSB, b5, corresponds to the rightmost switch. The value of the attenuation capacitor can be found by,

$$C_{atten} = \frac{\text{Sum of LSB Array Capacitors}}{\text{Sum of MSB Array Capacitors}} °C$$

The capacitor at the end of the network is used as a 'terminating capacitor'. Depending on the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The analog voltage is passed through the op-am and appears as an analog voltage[1].

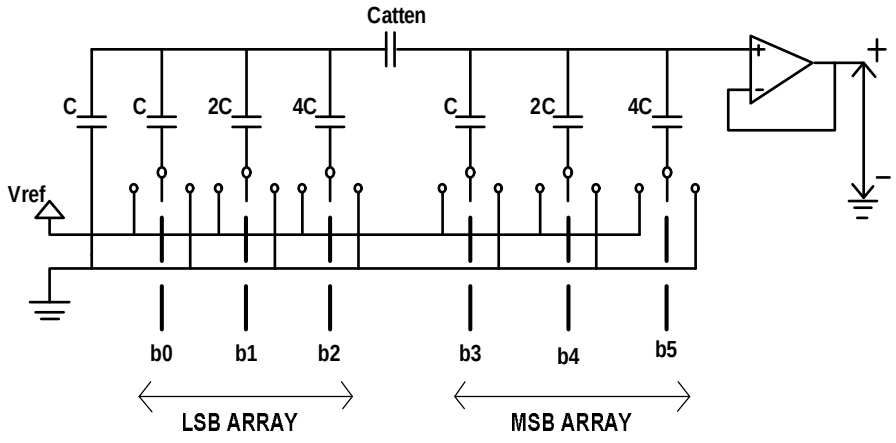

Figure 3. *A 6-Bit Charge-Scaling DAC using a split array*

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A. Switch Design

A 2:1 multiplexer is very simple to implement in CMOS technology, as only two transmission gates and one inverter are needed. The selection signal (V_{in}) is used to enable one or the other of the transmission gate switches. When V_{in} is HIGH, V_{high} is connected to the output V_{out} . When V_{in} is LOW, V_{low} is connected to the output. Figure 4 shows the schematic of 2:1 multiplexer.

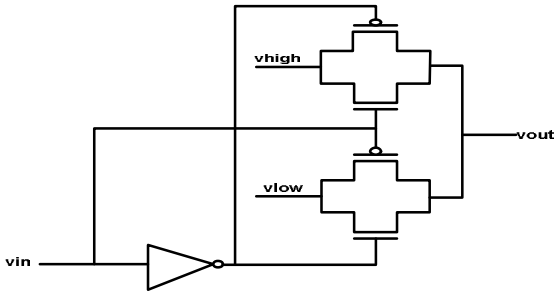

Figure 4. *Schematic of 2:1 multiplexer.*

B. Double Differential Amplifier

The differential amplifier is most often used with a current source load as shown in Figure5. If gate voltage of M1 is greater than gate voltage of M2, then drain current of M1 increases with respect to drain current of M2. This increase in drain current of M1 implies an increase in drain currents of M3 and M4. Therefore, the only way to establish circuit equilibrium is for output current to become positive and output voltage V_{out} to increase. If gate voltage of M1 is less than the gate voltage of M2 then output current become negative and V_{out} decreases. Biasing is also used for the second structure, with a complementary MOS transistor, which is also driven closely to the corresponding threshold voltage. The extra feature, which is added to the schematic shown in figure 5, to improve the performance of the differential amplifier, is the current mirror at the biasing circuit of the differential amplifier [7].

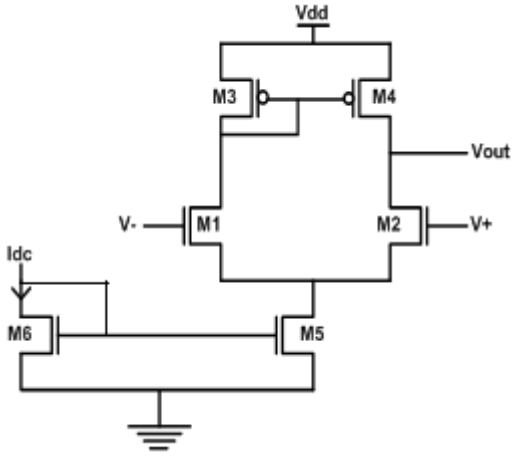

Figure 5. *Schematic view of differential amplifier.*

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IV. APPLICATION DESIGNED: SAR ADC

The SAR ADC is widely used in many communication systems, such as ultra-wideband and wireless sensor networks which require low-to-medium-resolution converters, with low power consumption. Analog input voltage,V_{in}, is held on a Sample/Hold device. A SAR ADC architecture is shown in Figure 6. To implement the binary search, N-bit code register in SAR logic block is first set to midscale: N'b100…00, where MSB is logic 1. This forces the DAC output (V_{dac}) to be half of the reference voltage (V_{ref}). Then comparator performs a comparison between V_{in} and V_{dac}: if V_{in} is greater than v_{dac}, the comparator output is a logic HIGH and the MSB of the N-bit code register remains at logic 1, if Vin is less than V_{dac}, the comparator output is a logic LOW and the MSB of the register cleared to logic 0. The SAR logic then moves to the next bit down, forces that bit HIGH, and does another comparison. The sequence continues all the way down to LSB. Once this is done, the conversion is complete and the N-bit digital word is available in the SAR's code register [8].

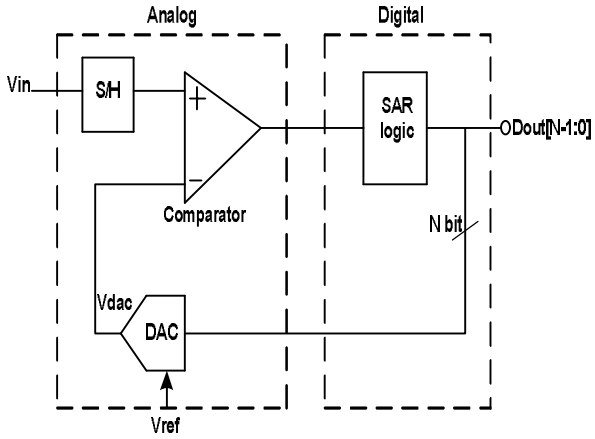

Figure 6. *SAR ADC architecture.*

A. Sample and Hold Circuit

Sample and hold circuit is used to sample an analog signal and to store its value for length of time. The circuit of sample and hold is shown in Figure 7. The inputs to a sample and hold circuit are sine wave with peak to peak voltage 1.2V and clock signal respectively. During ON period of clock, sampling of input takes place and during OFF period of clock, capacitor holds the sampled value and it is applied to the comparator input. And also during OFF period of clock, conversion from analog to digital takes place. The capacitance of 5pF with initial voltage 0V is taken.

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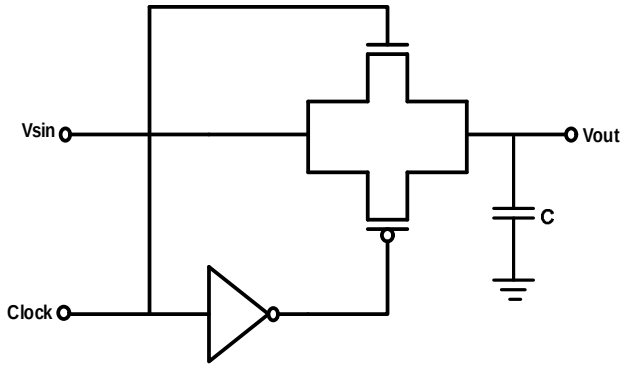

Figure 7. *Schematic of sample and hold circuit.*

B. **Dynamic Latched Comparator**

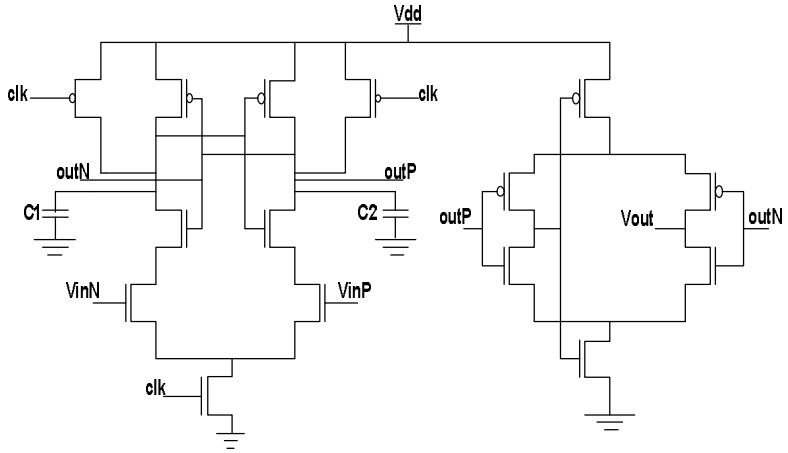

Figure 8. *Schematic of dynamic latched comparator.*

The dynamic latched comparator is composed of two stages as shown in Figure viii. The first stage is the interface-intermediate stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is covered of the two cross coupled inverters, where at each stage input is connected to the output of the other. It operates in two phases I) Interface phase and II) Regeneration phase. It has single NMOS tail transistor connected to ground. When clock is low tail transistor is turns off and depending on Vp and Vn output reaches to VDD or ground, if Vp>Vn output of Vp discharge faster than output of Vn. When clock is high (clk = Vdd) tail transistor is turns on and both the outputs discharges to ground [9].

C. **Synchronous SAR Control Logic**

The schematic of the SAR logic consists of shift register and code shift register using D-flip flop as shown in figure ix. Initially the reset line goes low. This line controls set line of FF1 and reset lines of all other sequencer flip flops.

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The same reset signal also controls the reset line of code register flip flops. Q and Qb of FF1 are set to 1 and 0 respectively. Qb also controls the set line of CF1. Hence the CF1 output is forced to 1. This is the MSB bit and the weight for VFSR/2. It should be noted that since sequence register is reset initially, the set input of all the code registers flip flops except CF1 is logic 1. Hence all the other code register output states are logic0 0. We get a sequence MSB=1 and all other set to 0. The analog equivalent of this weight will be generated by the DAC. When reset goes high and clock is triggered, Q becomes 0 and FF2 outs logic high. This low to high transition of FF2 triggers or clocks the code register flip flop CF1 to store control bus value to its output. When clock runs further, the code register flip flop retains the set value as FF2 output goes to zero. This process is repeated for each of the flip flops until after N clock cycles a high state comes out of sequencer flip flop controlling the code register LSB flip flop [10].

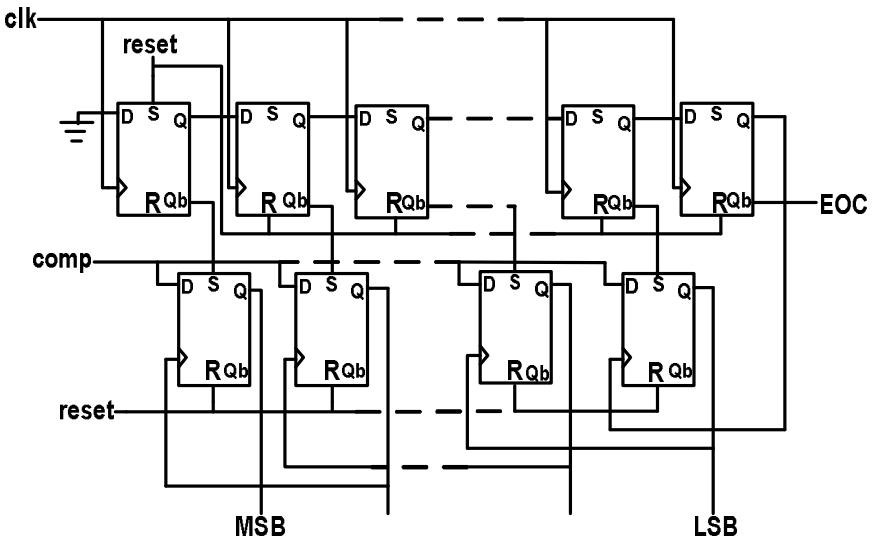

FIGURE 9. *SYNCHRONOUS SAR LOGIC TO CONTROL SINGLE-ENDED DAC.*

V. SIMULATION RESULTS

All simulations are performed using GPDK 90nm CMOS process technology files in cadence design environment. To design and simulate the charge scaling DAC and its application SAR ADC, Cadence virtuoso schematic editor is used and functionality is verified through simulations using Cadence virtuoso spectre tool. Using cadence virtuoso ADE visualization and analysis XL Browser and XL Calculator, Delay and Power consumption of the overall system is measured. The output waveform of 6-bit charge scaling DAC using split array is shown in Figure 10. Tablle 1 details the simulation results of DAC. A 1.2V, 6-bit SAR ADC and simulated in Cadence Environment. It is observed that, this SAR ADC consumes 802.6µW power.

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Figure 10. *Output waveform of 6-bit charge scaling DAC using Split Array.*

Table 1. Simulation Results of DAC

No. of Bits	Method Used	Signal Propagation Time (ns)	Power Consumption (nW)
3	Conventional	47.28	194.7
6	Regular Array	53.09	371.5
6	Split Array	47.83	366.3

VI. CONCLUSION

A 1.1V, 6-bit charge scaling DAC using split array is designed by considering power consumption of the circuit and chip area. Using split method in charge scaling architecture, total area of capacitor is reduced to achieve high resolution of DACs. A 1.1V, 6-bit charge scaling architectures are designed using cadence 90nm technology. The designed 6-bit charge scaling DAC is used in the SAR ADC for the purpose of charge redistribution. A 1.2V, 6-bit SAR ADC is implemented using cadence 90nm technology.

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