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Optimal Design of a Multi-Level Modular Capacitor-Clamped Dc-Dc Converter

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ABSTRACT: Magnetic-less multilevel dc-dc converters attract much attention in automotive industry due to their small size, high efficiency, and high temperature operation features. A multilevel modular capacitor-clamped dc-dc converter (MMCCC) is one of the most promising topologies among them with simple control and reduced switch current stress. This paper presents a quasi-resonant technique for multi-level modular switched capacitor dc-dc converter (MMSCC) to achieve zero current switching (ZCS) without increasing cost and Sacrificing reliability. In order to design the converter with the highest efficiency, the analytical power loss equation of an MMCCC should be derived. Also, by considering the stray inductance in the circuit, the optimal design approach should be divided into two cases, over damped case and under damped case. The converter can be designed to achieve high efficiency in both cases by varying circuit parameters. If the circuit is designed in over damped case, huge electrolytic capacitor bank has to be used whereas in under damped cases mall-size multilayer ceramic capacitor can be utilized due to the low capacitance requirement. This ZCS-MMSCC employs the stray inductance distributed in the circuit as the resonant inductor to resonate with the capacitor and provide low dv/dt and di/dt switching transition for the device. The ZCS-MMSCC does not utilize any additional components to achieve ZCS, and meanwhile solves the current and voltage spike problem during the switching transition, thus leading to reliable and high efficiency advantages over traditional MMSCC. Furthermore, the ZCS-MMSCC reduces the capacitance needed in the circuit to attain high efficiency. In this case, the bulky capacitor bank with high capacitance in traditional MMSCC to reduce voltage difference and achieve high efficiency is not necessary any more.

KEYWORDS: Multilevel Modular Capacitor-Clamped dc-dc converter (MMCCC), zero current switching (ZCS), stray inductance, analytical power loss equation

I. INTRODUCTION

In order to obtain the light weight, small size, high efficiency, high power density and integrated dc-dc converter, switched-capacitor circuits have been investigated since 1970's. Conventional switched-capacitor dc-dc converters have some common drawbacks like weak output regulation ability and structurally determinate voltage conversion ratio, pulsating input current and high current spike, high voltage spike across the switching device, high electromagnetic interference (EMI), unidirectional power conversion ability. Many approaches have been proposed to achieve voltage regulation by using duty cycle control. But all this methods have to sacrifice efficiency to achieve the voltage regulation, which is only acceptable in low power conversion field. Several ZCS techniques by inserting an inductor to switched-capacitor circuit have been proposed to solve the voltage spike, current spike and EMI problem. However, by adding a relatively big resonant inductor into the switched-capacitor circuit to achieve ZCS is a contradiction by itself. Switched-capacitor circuit with a magnetic core is not a switched-capacitor circuit any more, and the good features such as, high temperature operation, good integration, and small size will be lost.

In order to solve theproblemsoftraditionalconverters like high voltage conversion ratio, high current automotive application A multi-level modular switched-capacitor dc-dc converter (MMSCC) was proposed recently. MMSCC has modular structure, complementary control scheme, capability of reaching high voltage gain and reduced switch current stress. It shows good potential in automotive application. Nevertheless, because MMSCC stilluse hard switching, there still exist several problems limiting its power rating, such as high current spike, high voltage spike, high switching loss



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and severe EMI noise. With the increasing of power rating or current rating of the MMSCC, the voltage spike and switching loss problems become more andmore serious. Also, in order to increase the total system efficiency by reducing voltage difference between capacitors, higher capacitance electrolytic capacitors have to be used. The current rating of the electrolytic capacitor is small to some extent. In order to meet the high current ripple requirement, a huge electrolytic capacitor bank has to be used, which will increase the size of the converter significantly. Multi-layer chip type ceramic (MLCC) capacitor has much better performance than the electrolytic capacitor, such as equivalent series resistance (ESR), life time, and size in terms of current rating. But the capacitance of MLCC capacitor is very small, so it is not feasible to use MLCC capacitor for the traditional MMSCC.

In this paper presents a quasi-resonant technique for MMSCC that is able to achieve ZCS without increasing cost and sacrificing reliability. The proposed ZCS strategy employs the distributed stray inductances present in each module of the circuit resonating with the capacitors to provide zero current turn-on and turn-off to the devices. Because the MMSCC is especially suitable for high voltage gain with high input current application, the ZCS version also inherits all the benefits from it. By using the ZCS, the switching loss of the traditional MMSCC is minimized, current spike, voltage spike and EMI is reduced

II. PROPOSED CIRCUIT TOPOLOGY

Figure 2.1 shows the proposed four-level ZCS-MMSCC as an example. The circuit works as a four times step-up converter.

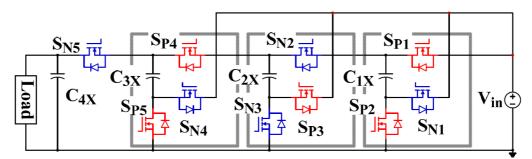


Figure 2.1: Four-level ZCS-MMSCC with three modular blocks

By using N-1 modular blocks, a switch and a capacitor, N-level ZCS-MMSCC with *n* timesvoltage gain can be generated. V_{in} represents the ideal input voltage source. L_{S} represent the equivalent stray inductance present in each module of the circuit. S_{P} and S_{N} are the sameswitching devices controlled complementary at 50% duty cycle. C_{1X} to C_{4X} are the capacitors with the average voltage from one time to four times of input voltage. L_{S} does not have to be in the position drawn in Figure 2.1, it could be distributed anywhere in series with switches or capacitors in the circuit. L_{S} is the sum of the connection wire parasitic inductance L_{SW} , capacitor parasitic inductance L_{SP} . Usually the connection wire parasitic inductance L_{SW} is the major part of the stray inductance. Because all the stray inductance is in series, when the current flows through it

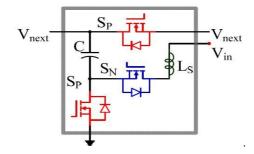


Figure 2.2: Proposed ZCS-MMSCC Modular Block



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Due to the modular structure of the circuit and the stray inductance is distributed equally in each module. The required stray inductance for resonant is more than 100 times smaller (2nH~13.5 nH) than other ZCS strategies using the same switching frequency. In case the stray inductance is not sufficiently large or equally distributed in each module, a small air core could be utilized to promise each module have the same stray inductance for resonant.

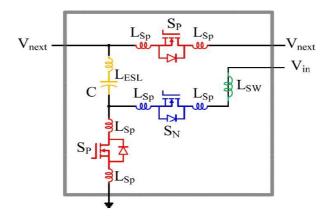


Figure 2.3:ZCS-MMSCC Modular Block With All The Stray Inductance

For traditional MMSCC in high power and high current application, a huge capacitor bank has to be employed in order to sustain current and increase efficiency, which increases the converter size in a significant manner. The huge switching loss and voltage spike caused by the large turn-off current is another problem. Considering the stray inductance present in each module of MMSCC, the capacitance can be designed to resonate with the stray inductance at switching frequency to provide the zero current switching to the devices. In this case, small size, low ESR, high current rating and high temperature rating MLCC capacitor with relatively small capacitance can be utilized. The switching loss of device is minimized, capacitor conduction loss and EMI is also reduced accordingly. Smaller size and higher efficiency is achieved by using ZCS in MMSCC. Hence, ZCS-MMSCC is more suitable to high power, high current and high temperature application.

III. OPERATION PRINCIPLE

Figure 3.1 shows the idealized waveform of proposed ZCS-MMSCC under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assuming the input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switch is turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switch S_P , S_N and stray inductance will decrease to zero when the switch is turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of the switch is achieved in both turn on and turn off. The capacitor is charged in half-period with the sinusoidal current waveform and discharged in another half period also in the sinusoidal shape. So, the current through the capacitor is the sum of the current through the scapacitor discharges, the current is negative. The voltage across the capacitor has a dc offset with a sinusoidal ripple. The dc voltage offset is determined by the capacitor current and capacitance. The operation of the circuit can be described in two states as shown in Figure 3.2 and Figure 3.5 with different switch turned on.



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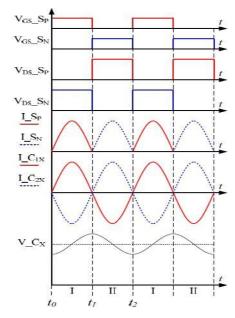


Figure 3.1: Typical Waveforms Of Proposed ZCS-MMSCC



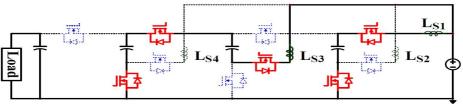


Figure 3.2: Operation Mode State I SP is ON

Figure 3.2 shows the state when S_P is turned ON at $t = t_0$ while S_N is OFF. During this state C_{1X} is charged by V_{in} . C_{3X} is charged by V_{in} and C_{2X} in series. Figure 3.3 and Figure 3.4 show the two simplified equivalent circuits of state I. Figure 4.3 shows the situation when V_{in} , L_{S1} , S_{P1} , C_{1X} and S_{P2} form a resonant loop. Because of the presence of the equivalent stray inductance L_S , before the switch is turned ON, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned ON, so S_P is turned ON at zero current. For the case shown in Figure 3.3, after L_{S1} and C_{1X} resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} should be turned OFF at this point, so that the switches are turned ON at zero current. In this case there is only one capacitor in the equivalent circuit other than two capacitors in series in other equivalent circuits.

Figure 3.4 shows the situation when V_{in} , L_{S3} , S_{P3} , C_{2X} , S_{P4} , C_{3X} and S_{P5} form a resonant loop. For this case after L_{S3} resonate with C_{2X} and C_{3X} in series for half cycle, the current through S_{P3} , S_{P4} and S_{P5} will decrease to zero too. So, zero current turn off is also realized on these switches.

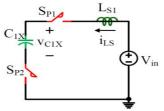


Figure 3.3: Simplified equivalent circuits of state I (a)

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The required stray inductance value is two times smaller than the other circuits assuming the capacitance are the same. This will not be a problem in the real circuit design and layout; one only need to pay attention to make sure the stray inductance of all the other loops is twice as large as that of the first resonant loop.

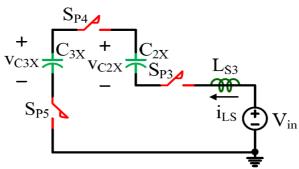


Figure 3.4: Simplified equivalent circuits of state I (b)

State II (S_N is ON)

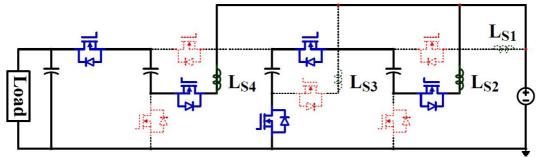


Figure 3.5: Operation modes State II S_N is on

Figure 3.5 shows the state when SN is turned on at $t = t_1$ while SP is off. During this state, C_{2X} is charged by the V_{in} and C_{1X} in series; C_{4X} is charged by Vin and C_{3X} in series. Figure 3.6 and Figure 3.7 show the simplified equivalent circuits of state II.

Figure 3.6 shows the situation when V_{in} , L_{S2} , S_{N1} , C_{1X} , S_{N2} , C_{2X} and S_{N3} form a resonant loop. Because of the presence of the L_S , the current through S_N will also increase its value from zero in a resonant manner. The zero current turn-on of S_N is achieved. For the case shown in Figure 3.6, after L_{S2} , C_{1X} and C_{2X} resonate for half cycle at $t = t_2$, S_{N1} , S_{N2} and S_{N3} will have a zero current turn-off when the current through them decreases to zero.

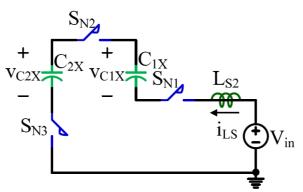


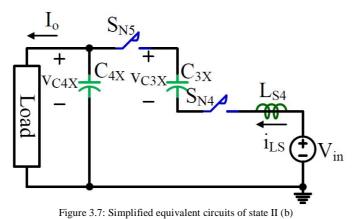
Figure 3.6: Simplified equivalent circuits of state II (a)



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Figure 3.7 shows the situation when V_{IN} , L_{S4} , S_{N4} , C_{3X} , S_{N5} and C_{4X} form a resonant loop. After L_{S4} resonate with C_{3X} and C_{4X} in series for a half cycle, the current through S_{N3} , S_{N4} and SN5 will also decrease to zero. Hence, zero current turn off is also realized on these switches.



IV. SIMULATION RESULTS

Figure 4.1 shows the overall simulation model of the proposed topology and is simulated using SIMULINK MATLAB software. Three level of boosting the output is taking place. That is here we are giving an input of 12V and in simulation we are nearing the value of 38.69V. It is approximately equal to three times of the input. So we can justify that the simulated prototype model is having three level of boosting the output voltage. The simulation result is consistent with the theoretical analysis, which verifies the above analysis.

Figure 4.2 shows the simulation output with three times boosting of the input voltage

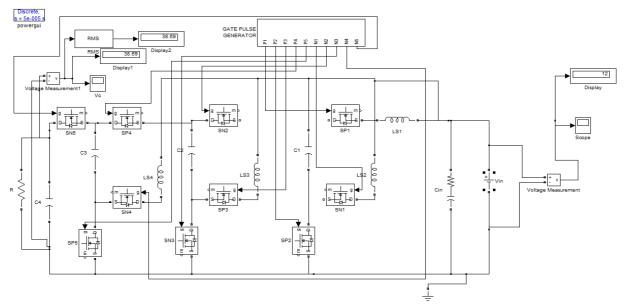
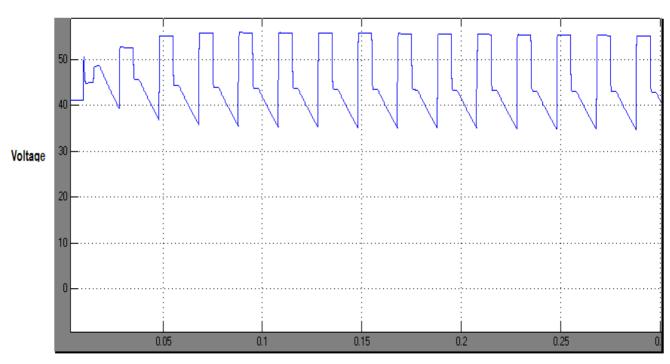


Figure 4.1: Overall Simulation for the proposed model



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Time period

Figure 4.2: Three level Boosting Output

V. EXPERIMENT RESULTS



Figure 5.1: Hardware Setup



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The hardware set up of the proposed Multi Level Modular Capacitor Clamped DC-DC converter with three level boosting was done and is shown in Figure 5.1. The hardware model consists of three sections mainly Controller circuit section, Driver circuit section and the main circuit section. In addition we are using two multi taps transformer with fivetapping each for providing the gate voltages for the corresponding switches.

In this project we are making use of PIC series micro controller 16F877A for producing switching pulses. The micro controller has got many coding with in it. PIC will execute these coding lines according to the switching pulses, and a crystal oscillator is introduced. The crystal oscillator can produce pulses at a rate of 20KHz/sec. Thus finally the switching pulses are produced and it reaches the Driver circuit. The driver circuit has got two main functions to do they are listed below

1. Amplification of the 5V pulse from the controller to 12V (because, the MOSFET require 12 V DC supply to function).

2. Isolation (to isolate the main circuit from the controller circuit). So damage to MOSFET is prevented.

A. HARDWARE OUTPUT

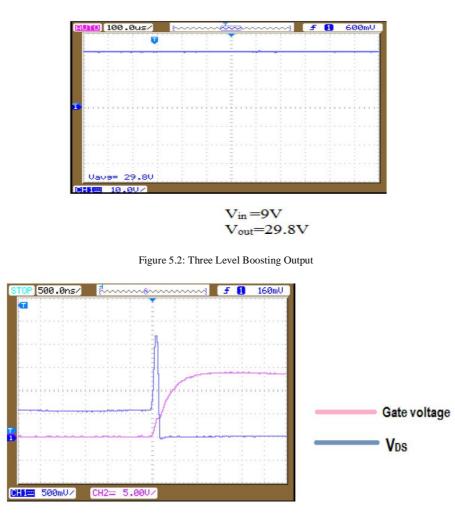


Figure 5.3: Soft Switching Output



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VI. CONCLUSION

The presented ZCS-MMSCC has all the advantages of ZCS and MMSCC. And it has some special features besides the features got from ZCS and MMSCC. All the features can be concluded as follows:

- 1. Reduces dv/dt, di/dt and EMI because of ZCS;
- 2. Reduces the switching loss which improves efficiency;
- 3. Uses simple control strategy and possesses modular structure and bidirectional power conversion;
- 4. Increases the potential power rating by using MLCC capacitor;
- 5. Reduces the capacitance and capacitor size, which lowers the cost
- 6. Utilizes distributed stray inductance to achieve ZCS which improves reliability.

A new soft-switching operation strategy to the existing MMSCC has been proposed and validated by both simulation and experiment results. A 40 W, 12 V input three-level converter prototype for automotive application has been built and tested based on proposed circuit. The ZCS-MMSCC overcomes the current and voltage spike problems of traditional MMSCC and provides a technically viable soft-switching strategy with circuit layout stray inductance. This technique could also be applied to the switched-capacitor circuits on a semiconductor chip with very small stray inductance in the circuit without pushing the switching frequency to megahertz. The proposed ZCS-MMSCC also shows great potential to high voltage gain and high input current applications.

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BIOGRAPHY



Sujith K received his B. Tech degree in Electrical and Electronics Engineering from Chettinad College of Engineering & Technology, Anna University Chennai in 2012. He is currently pursuing his final year M-Tech degree in Power Electronics in the Department of Electrical and Electronics Engineering, Mar Athanasius College of Engineering, Mahatma Gandhi University, Kerala. His areas of interests are Power Electronics and Drives, Power Quality and Power Transmission.