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Efficient Implementation of Adaptive Noise Canceller Using FPGA for Automobile Applications

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ABSTRACT: This paper presents the architecture and implementation of a real time adaptive NLMS filter for non-stationary noise cancellation in a car environment.The active noise control techniques using adaptive digital filters are very much suitable and well proven.The proposed efficient Adaptive Noise Canceller is realized using Xilinx System Generator 12.3 on Spartan 3E FPGA. System Generator is a DSP design tool from Xilinx that enables the use of The Mathworks model-based design environment ,Simulink for FPGA design.All FPGA implementation steps including Synthesis, place and Route are automatically performed to generate an FPGA programming file and the design is evaluated in terms of speed, hardware resources and power dissipation.

Keywords: LMS Adaptive filter, Noise canceller, Xilinx system generator 12.3, Spartan 3E, VHDL

I. INTRODUCTION

The purpose of active noise control is to generate an anti-noise signal from a speaker to minimize the noise level of the original signal. Traditional noise control techniques use passive treatments to minimize the noise level [1, 4, 5]. In automobile industry, the noise level in the car cabin is minimized by using mufflers to absorb the engine noise. However, these techniques cannot minimize noise that has a low frequency. An adaptive filter is used to generate the anti-noise signal thus minimizing noise as shown in figure 1[6, 7]. An efficient LMS adaptive filter is implemented to achieve this noise cancellation.

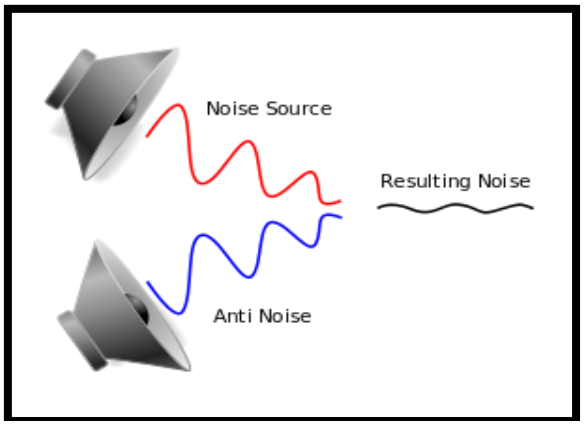

Figure 1.Graphical depiction of Active Noise Reduction

II. ADAPTIVE NOISE CANCELLER

The Adaptive Noise Canceller employs a directional microphone to measure and estimate the instantaneous amplitude of ambient noise and another microphone is used to take the speech signal which is contaminated with noise[13]. The ambient noise is processed by the adaptive filter to make it equal to the noise contaminating the speech signal and then

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is subtracted to cancel out the noise in the desired signal. In order to be effectively removed, the ambient noise must be highly correlated with the noise components in the speech signal.
The Least Mean Square (LMS) adaptive filter is used for implementing the noise cancellation because of its simplicity and suitability for real-time applications [14][15].The block diagram of Adaptive Noise Canceller is shown in figure 2.

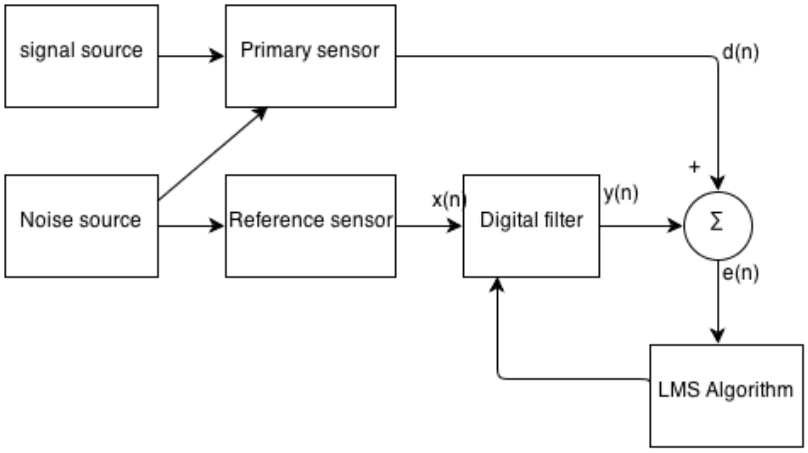

Figure 2. Block Diagram of Adaptive Noise Cancellation

In figure 2,The error at the output of the filter can be expressed as,

$$e_n=d_n-W_n^T u_n \quad (1)$$

which is simply the desired output minus the actual filter output. The step size parameter,μ in the weight update equation ,

$$W_{n+1}=W_n+2\mu.e_n.u_n \quad (2)$$

determines how fast the algorithm converges to the optimal weights

$$0<\mu<2/M.S_{max} \quad (3)$$

Where M is the number of filter taps and S_{max} is the maximum value of the power spectral density of the tap inputs μ.[17]

From each set of equations(1),(2) and (3), we can construct a block diagram consisting of an interconnection of delay elements, multipliers, and adders. Such block diagrams are called realizations of the system or equivalently structures for realizing the system[18].

III. REALIZATION FACTORS

The major factors that influence the choice of realization are
1. Computational Complexity
2. Memory Requirements
3.Finite Word-length Effects
4. Ease of Implementation.
Computational complexity refers to the number of arithmetic operations (multiplications, divisions, and additions) required to compute an output value y(n) for the system.
Memory requirements refer to the amount of memory required to store the system parameters, past inputs, past outputs and any intermediate computed values.
Finite word-length effects or finite precision effects refer to the quantization effects that are inherent in any digital implementation of system, either in hardware or in software [8].
The filter could be implemented by cascading as many units of the unit cell as the length of the filter as shown in figure 3and figure 4.The basic elements of filter structure are shown in figure 5.[10][12].

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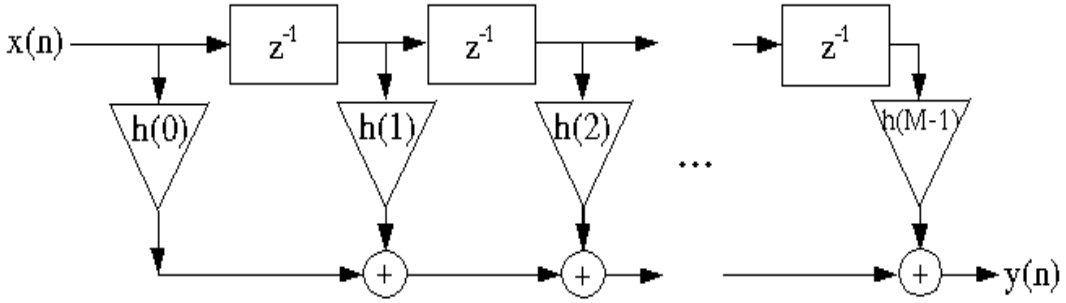

Figure3.FIR filter structure representation 1

Or as

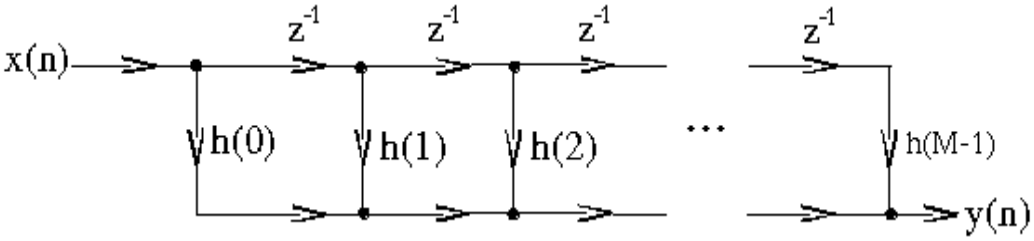

Figure 4.FIR filter structure representation 2

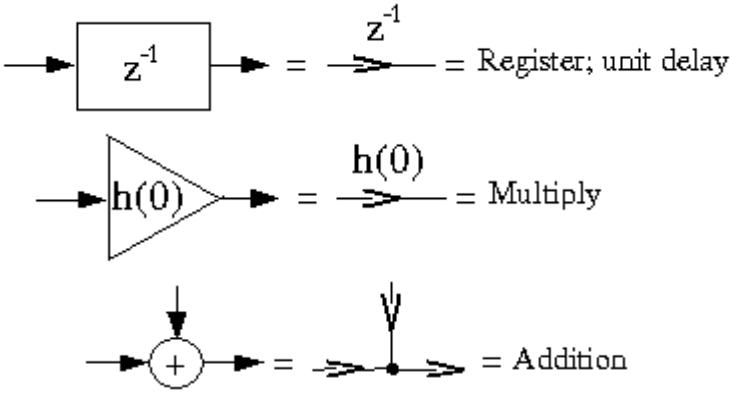

Figure 5.Elements of Filter Structure

IV. FPGA IMPLEMENTATION OF ANC

A The SPARTAN-3E FPGA

The FPGA used to implement the Adaptive Noise Canceller is 500,000-gate Xilinx Spartan-3E XC3S500E as shown in figure 6.Spartan-3E devices contain a two-dimensional row and column based architecture to implement custom logic. For implementing ANC using LMS filter, the number of operations for an N-tap filter has been reduced to 2* N multiplications and N additions per coefficient update. Numerous techniques have been devised to efficiently calculate the convolution operation when the filter's coefficients are fixed in advance [20]

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Figure 6. Spartan-3E kit

B Implementation of LMS Algorithm

The LMS algorithm uses an FIR filter structure. The design shown in figure represents a structural view of the filter. From the figure, the main components of the filter consist of L-1 Unit Delay Registers and L Weight Updates. The Unit Delay Registers are simply D flipflops.Each weight Update component consists of a multiplier, an adder and a buffer to store the new weights' update of the filter coefficient. [15]According to equation (2), the filter output is subtracted from the desired signal to produce an error signal. The error signal is then multiplied with μ and then with the input signal, which produces next sets of filter coefficients.

C Fixed point representation of data

Fixed point is a step between integer mathematics and floating point. This has the advantage of being almost as fast as integer arithmetic and able to represent numbers with fraction. It uses a smaller area in FPGA than floating point to process arithmetic operations [19]. A fixed-point number has an assigned width and an assigned location for the decimal point. As long as the number is big enough to provide enough precision, fixed point is fine for most DSP applications. Because it is based on integer math, it is extremely efficient as long as the data does not vary too much in magnitude [2][3].

D Word length Selection

The most essential task is the right selection of word lengths for the various variables in the system. Short word lengths may result in extra round-off errors, which can cause instability or poor performance. On the other hand, the use of excessively long word lengths increases system complexity which in turn reduces its maximum speed and increases the used area of the FPGA.So balance should be achieved between the system round-off errors and the maximum speed of operation together with the used area of the FPGA[9][10][12].

The training algorithm for the adaptive filter usually use a direct form FIR structure that has a delay which is determined by the depth of the output adder, which is dependent on the filter's order.
A direct form FIR filter of length 16 is used for the purpose of noise cancellation.

V. TESTING AND RESULTS

The efficient fixed point LMS based adaptive filter is designed using VHDL.The design is synthesized and simulated on Xilinx System Generator 12.3.The simulation results after implementation of the Adaptive Noise

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Canceller on FPGA are shown in figure 7.The hardware resources required to implement this filter can be obtained from the simulation results shown in figure 7 from the device utilization summary and synthesis report.

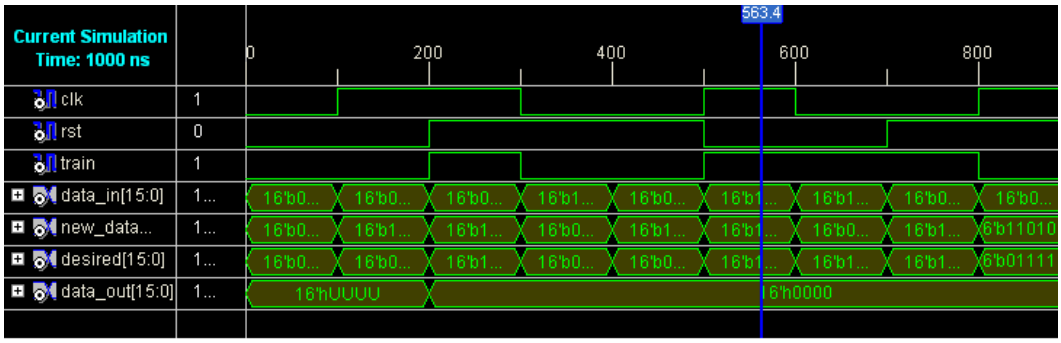

Figure 7.Simulation Results of Adaptive Noise Canceller

VI. RESOURCE UTILISATION

Table 1. Device Utilization summary represents implementation result mentioning resource utilization of the device Xilinx SPARTAN 3E kit. The synthesized outputs are given below. The number of gates required to implement the Adaptive Noise Canceller and the utilization percentage of the total hardware in the FPGA kit is summarized in Table 1.The number of Slice flipflops,Look-up table,number of bonde IOBs,number of GCLKs are summarized in Table 1.

The results prove that the LMS adaptive filter implemented for the Adaptive Noise Cancellation satisfy the desired demand by providing stability after period of time.(time of Convergence) in a non-stationary (car)environment.Efficient implementation is justified by the resource utilization efficiency as shown in the Table1.

Table1.Device Utilization summary

D Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	368	4656	7%
Number of Slice Flip Flops	585	9312	6%
Number of 4 input LUTs	319	9312	3%
Number of bonded IOBs	67	190	35%
Number of MULT18X18SIOs	16	20	80%
Number of GCLKs	1	24	4%

The experimental set up for Implementation of Adaptive Noise Canceller is shown in figure 8.The experimental set up is done using FPGA SPARTAN 3E kit along with Computer loaded with Xilinx System Generator Software as shown in figure 8.

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Figure 8.Experimental set up for Implementation of Adaptive Noise Canceller

VII. CONCLUSION

The implementation of Adaptive Noise Canceller using VHDL for a non-stationary environment is presented and the word length requirement for the design has also been discussed.The performance of the Adaptive Noise Canceller in a non-stationary environment is expressed by its simplicity to implement and its stability when the step size parameter is selected appropriately by proven results.

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BIOGRAPHY

S.THILAGAM graduated from Government College of Technology, Coimbatore, affiliated to Anna University in M.E-VLSI Design. She is an Assistant Professor in the Department of Electronics & Communication Engineering in Kumaraguru College of Technology, Coimbatore. She has a wide academic and teaching experience of eight years. Her area of interest in Research is VLSI Signal Processing.