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# Harmonic Orientation of Multi Carrier Modulation in Neutral Point Clamped Inverter

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**Abstract— in this paper, a novel technique used to balancing the capacitor voltage of neutral point clamped inverter without transformer and also reduces the total harmonic distortion at the output by using multi carrier pulse width modulation technique. This paper presents orientation of higher order harmonics of fifteen level neutral point clamped inverter. The total harmonic distortion will be carried out using fast Fourier transformation. The effectiveness of the proposed method is verified by simulations.**

**Keywords— FACTS, IGBT, multilevel, multi carrier PWM, NPC inverter, total harmonic distortion.**

## I. INTRODUCTION

The necessity of increasing power quality in the past years leads to the development of inverter due to its efficiency and control methods. An inverter is a device which converts the direct current (DC) into an alternating current (AC) without changing the magnitude. The converted current may contain the required voltage and frequency, switching devices and control circuits. In order to improve the quality of an inverter by performs the power conversion of small voltage steps resulted in lower harmonics. The output voltage of an AC side contains several numbers of discrete levels of equal magnitude.

The harmonic content of a multilevel inverter is reduced compared to inverter voltage waveform. This method is known as multilevel inverter. Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. The semiconductor devices are not connected in series for one single high-voltage switch. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Multi-level power inverters employ power semiconductor switches in the inverter to select the DC voltage source to produce a staircase voltage waveform at the output of inverter. The output of a multilevel inverter is in the form of staircase waveform, so that the harmonics get reduced thereby the voltage gain get increased and the power quality increases.

The general purpose of the multilevel inverter is to synthesize a nearly sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources. As the number of level increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also as more steps added to the waveform, the harmonic distortion of the output waveform decreases, approaching zero as the level increases. As the number of level increases, the voltage that can be summing multiple voltage levels also increases.

Several multilevel inverter topologies are proposed over the past few years, the most popular multilevel inverters which are mostly used are Diode-clamped, Flying capacitor and the H-bridge multilevel inverter. Neutral Point Clamped Inverter is more preferred than other topology. In this paper is concentrated for the improvement of output voltage waveform, reduction of harmonics and for reactive power compensation by using multi carrier pulse width modulation (PWM) technique. It used to balance the dc split voltage and improve the efficiency of the system and reduce the voltage fluctuation. To take benefit of the advantages of the multilevel inverter, Low Electromagnetic interference, Low Total harmonic distortion, reduce conversion losses, it is used to boost the voltage based on the requirement, Reduce Switching losses.

In the proposed system Multi Carrier Pulse Width Modulation is used to control the dc split capacitor and reduce the harmonics. The simulation of the proposed control method will be carried out using Mat lab simulation tool wherein the detailed analysis and design aspects can be emphasized.

## II. NEUTRAL POINT CLAMPED INVERTER

In response to the growing demand for high power inverter units, multilevel inverters have been attracting

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growing attention from academia as well as industry in the recent decade. The multilevel inverter refers to using a converter in the inverting mode. Power can flow from DC side to AC side.

Multilevel inverters are extensively used in medium voltage levels with high-power applications. The field applications include use in laminators, pumps, conveyors, compressors, fans, blowers, and mills. Subsequently, several multilevel converter topologies have been developed. Multilevel inverter is a power electronic device built to synthesize a desired ac voltage from several levels of dc voltages. Such inverters have been received increasing attention in the past few years for high power application. A small total harmonic distortion is the most important feature of these inverters. In the adjustable speed drive application, the multilevel inverters can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency AC source and the output to the variable frequency AC load. The major differences when using the same structure for ASDs and for back-to-back interties are the control design and the size of the capacitors. Because the ASD need to operate at different frequencies, the DC link capacitor needs to be large enough to avoid a large voltage swing under transient state.

Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricate cells), and the neutral point clamped inverter. As reported in the literature, the NPC inverter has been used in several practical instances for broadcasting amplifier, plasma, industrial drive as well as FACTS applications etc.

For FACTS application the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates over-sizing of the dc link capacitors. The capacitor clamping inverter, though the three-level scheme of which was published in the early 1980's had been rarely discussed until the introduction of the "imbricate cells". The individual clamping capacitor needs only to smooth the switching frequency ripple voltage and the required capacity for each clamping capacitor is therefore small. However, as the number of level increases, such problems as thermal designing, low-inductance designing, as well as insulation designing of the system will become critical.

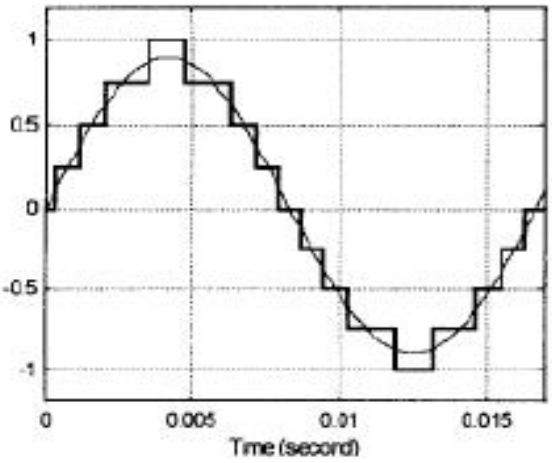

Fig.1. A typical output waveform

The neutral point clamped inverters provide high quality output, low switching frequency and high voltage capability. But these features are obtained when the dc split voltage is balanced. To balance the dc split voltage used pulse width modulation. In this project multi carrier pulse width modulation is used and hysteresis controller is used. This controller is used to avoid unwanted rapid switching. The hysteresis controller is very popular because of its inexpensive, simple and easy to use. And also the total harmonic distortion is reduced by using of multi carrier pulse width modulation technique.

PWM techniques minimize the magnitude of the harmonics but not removed completely. The multilevel inverter is used to remove the particular harmonics completely. Fig 1 shows the multi level inverter waveform. In the multi level inverter the output level equal to the source which I applied to the inverter. In this diagram sinusoidal waveform and multilevel approximation is indicated.

## III. MULTI CARRIER PULSE WIDTH MODULATION

Multi Carrier pulse width modulation is the extension of two level carrier based modulation. The multi carrier pulse width modulation technique consists of one reference signal and several triangular carrier signals. The basic principle of multi carrier pulse width modulation (MC-PWM) is comparison reference waveform with carrier waveform. To generate m level it required m-1 carrier. Both carrier and reference signals have same frequency and amplitude. A frequency of sine reference waveform is $f_r$ and peak to peak value of reference waveform is $A_r$. Each carrier is compared with

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modulating signal at every instant. If the triangular carrier is greater than reference signal the result is 1 otherwise 0. Sum of the different comparison which represents voltage level is output modulator. The scheme is characterized by amplitude modulation index $m_a$ and frequency modulation index $m_f$.

For a sine waveform (reference) cantered in the carrier bands, the duration of time that the waveform exists. For an m-level inverter, m-1 carriers with the same frequency $f_c$ and the same amplitude $A_c$ are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude $A_m$, a frequency $f_m$, and its zero centred in the idle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active devices corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active devices corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index, $m_a$, and the frequency ratio, $m_f$, are defined as

$$M_a = A_m / (m-1).\ A_c$$
$$M_f = f_c / f_m.$$

Having more than two levels to build sinusoidal shape it is instinctual that it can reduce the harmonics in load. However, the improvement of current is depends on the controller employed. The sub harmonic pulse width modulation is more popular because of its simplicity and a good result for all the operating condition includes over modulation. In the case of three phase inverter three legs are produced. Requirements of three phase system $120^0$ phase shifted modulation sinusoids are needed. Two possibilities are renowned by use of carrier signal. The carriers have the same frequency and same amplitude and are disposed so that the bands are continuous. This method takes the instantaneous average of the maximum and minimum of the voltages ($v_a^*$, $v_b^*$,$v_c^*$) and subtracts this value from each of the individual reference voltages i.e

$$V_{offset} = \frac{\max(v_a^*, v_b^*, v_c^*) + \min(v_a^*, v_b^*, v_c^*)}{2}$$

$where,$

$$v_a^* = v_a^* - V_{offset}$$
$$v_b^* = v_b^* - V_{offset}$$
$$v_c^* = v_c^* - V_{offset}$$

Fig 2 shows that the multi carrier pulse width modulation. Multi carrier pulse width modulation has one reference waveform and multi carrier waveforms. These carrier and reference waveforms are produce pulses. These pulses are applied to the converter gate. The multi carrier Pulse Width Modulation produces high quality output and reduces the harmonics.

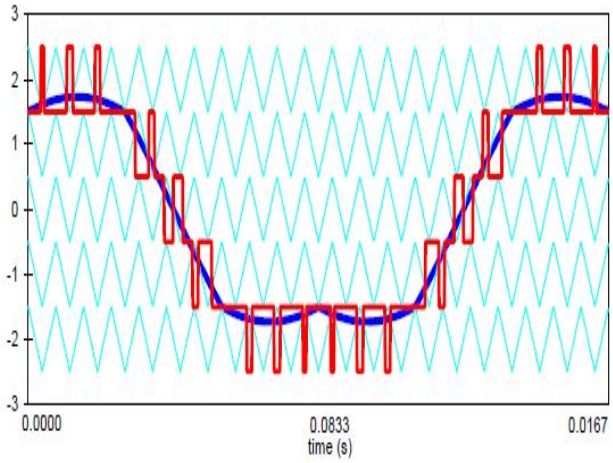


Fig:2 .Multilevel Carrier Based PWM Showing Carrier Bands

## III. HYSTERESIS CONTROLLER

The current control plays an important role in power electronics circuits. The main role of the control systems in current regulated inverters is to force the current in the three phase load. Among the several PWM techniques, the hysteresis current control is used very often because of its simplicity implementation. Also give fast response current control loop and it does not need any knowledge of load parameters. But it has the disadvantage when the current control with fixed hysteresis band that the frequency varies within band.

It controls the switches of the voltage source inverter and to ramp the current, so that it follows the reference current. If the value for the minimum and maximum error should be the same, the hysteresis bandwidth is equal to two times of error. When the error reaches an upper limit, the transistors are switched to force the current down

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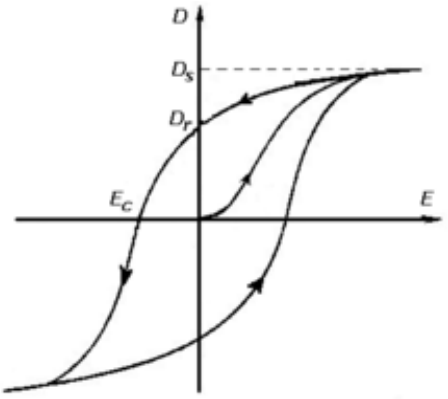


Fig.3. Hysteresis Controller

Electric displacement field D of a ferroelectric material as the electric field E is first decreased, then increased. The curves form a hysteresis loop. The ramping of the current between the two limits where the upper hysteresis limit is the sum of the reference current and the maximum error or subtraction of the reference current and maximum error is shows in the figure 4.

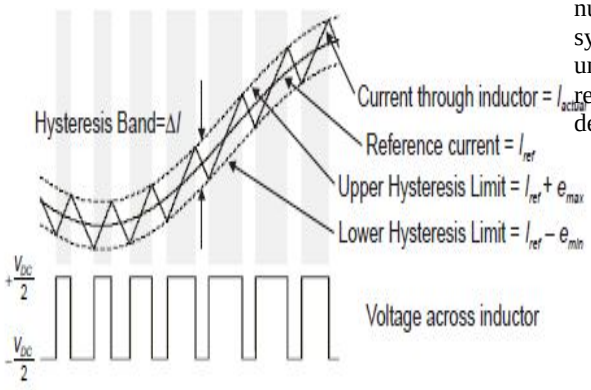


Fig.4. Hysteresis Band

## IV. ANALYSIS OF FIFTEEN LEVEL NEUTRAL POINT CLAMPED INVERTER

The most commonly used multilevel topology is the neutral point clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The key difference between the two-level inverter and the three-level inverter are the diodes $D_{1a}$ and $D_{2a}$. These two devices clamp the switch voltage to half the level of the dc-bus voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is 1/− n dc V. Although each active switching device is only required to block V, the clamping devices have different ratings.

The neutral point clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. Due to capacitor voltage balancing issues, the neutral point clamped inverter implementation has been limited to the three levels. Because of industrial developments over the past several years, neutral point clamped inverter is now used extensively in industry applications.

In general for an N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N is sufficiently high, the number of diodes and the number of switching devices increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.

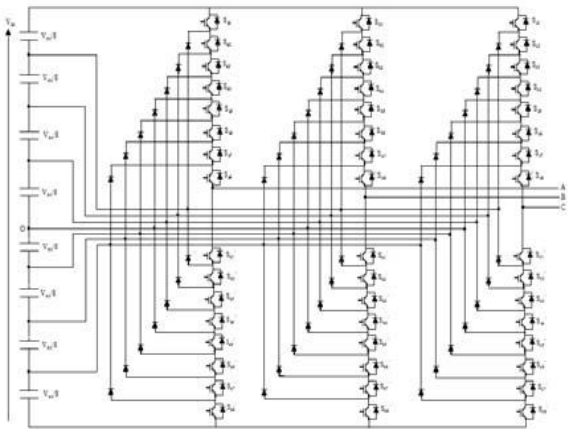

Fig.5. A typical Multilevel Inverter.

The structure is more complicated than two level inverter; the operation is straightforward and well known. In summary, each phase node (a, b, or c) can be connected to any node in the capacitor bank ($V_3$, $V_2$, $V_1$). Connection of the a-phase to positive node, $V_3$ occur

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when $S_{1ap}$ and $S_{2ap}$ are turned on and to the neutral point voltage, when $S_{2ap}$ and $S_{1an}$ are turned on and the negative node $V_1$ is connected when $S_{1an}$ and $S_{2an}$ are turned on. There are some complementary switches and in a practical implementation, some dead time is inserted between the gating signals and their complements meaning that both switches in a complementary pair may be switched off for a small amount of time during a transition. However, for the discussion herein, the dead time will be ignored. Switching state, the a-phase current $I_a$ will flow into the junction through diode $D_{1a}$ if the current is negative or out of the junction through diode $D_{2a}$ if the current is positive. The dc currents $I_3$, $I_2$, and $I_1$ are the node currents of the inverter.

A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level. For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor signals are established, general expressions for the a phase line-to-ground voltage and the a-phase component of the dc currents can be written as

$$V_{ao} = H_{aN}V_{No} + H_{aN-1} - V_{N-1o} + \ldots\ldots\ldots + H_{a1}V_{1o}$$
$$V_{bo} = H_{bN}V_{No} + H_{bN-1} - V_{N-1o} + \ldots\ldots\ldots + H_{b1}V_{1o}$$
$$V_{co} = H_{cN}V_{No} + H_{cN-1} - V_{N-1o} + \ldots\ldots\ldots + H_{c1}V_{1o}$$

The node currents for the N level inverter are given by

$$I_N = H_{aN} I_a + H_{bN} I_b + H_{aN} I_a$$
$$I_{N-1} = H_{aN-1} I_a + H_{bN-1} I_b + H_{cN-1} I_a$$
$$I_{1\ldots\ldots} = H_{a1} I_a + H_{b1} I_b + H_{a1} I_a$$

If the offset value is low, a slow voltage-balancing dynamic on the dc-split capacitors is produced. If the value of the offset is high the system dynamic is slow. The voltage balancing control variable is the neutral point current $i_o$. In the steady state condition the average value of this variable is zero. The current injected into the neutral point inverter which the output phases are connected to that point and the output currents are $\{i_a, i_b, i_c\}$.by the following expression are described the currents $i_{c1}$and $i_{c2}$:

$$I_{c1} = i_{cm} - \frac{i_o}{2}$$
$$I_{c2} = i_{cm} - \frac{i_o}{2}$$

The relationship between the modulation signals and the compensation is determined by taking into account the value of the duty cycle. Its shows in the following expression:

$$d'_a = \left|v_{an} - v_{ap} + 1\right| - \left|2v_{a-off}\right|$$

By adding an offset to the modulation signals, the duty cycle $d_a$ is changed. The NP current can be calculated as follows.

$$\bar{I}_o(k+1) = \frac{d'_a i_a(k+1) + d'_b i_b(k+1) + d'_c i_c(k+1)}{i_a(k+1)}$$

Fig 6 shows that the current in the capacitors. The above expressions are used to found the capacitor current. The mathematical process for the other phases is the same as the phase a. The equations define the optimal offset value they include the relevant variables and the system dynamics, the modulation index, the carrier frequency, the dc split capacitor values and the corresponding capacitor voltages.

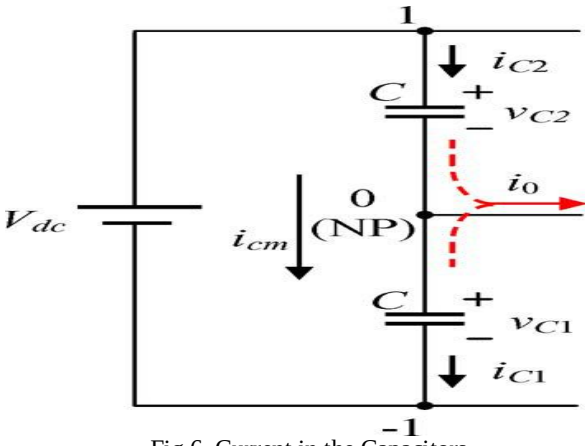


Fig.6. Current in the Capacitors.

## V. SIMULATION RESULT

In this symmetric multilevel inverter 28switches is used. In this the diode clamped inverter. Basically the inverter operation is to convert the variable DC into an AC. The input dc source is given by using batteries. Here hysteresis controller is used to control the output voltage of the inverter. The output volatge has some harmonic. This harmonics are reduced by the using of filter. Fourteen sources are used these are capacitor sources. Each source has 100V.

This dc split capacitor is balanced by using the Multi Carrier Pulse Width Modulation. And also this Pulse Wdth Modulation Strategy reduce the harmonics. The

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harmonics pushes by PWM into a high frequency range around the switching frequency. The frequencies at which the voltage harmonics occur can be described. By using multi carrier PWM the total harmonic distortion is reduced. Its shows in the simulation result. And also compensate the reactive power. The efficiency is high. By using graphical user interface the total harmonic distortions are obtained.

The total harmonic distortion is calculated by the fast fourieBy using multi carrier pulse width modulation technique the triggering pulse given to the switches are controlled. The input voltage to the dc source is 100V.The level creator part produces an output voltage which is always positive and the bridge part is to change the polarity of the output. The THD get reduced to 4.28%. its shows in fig.7.

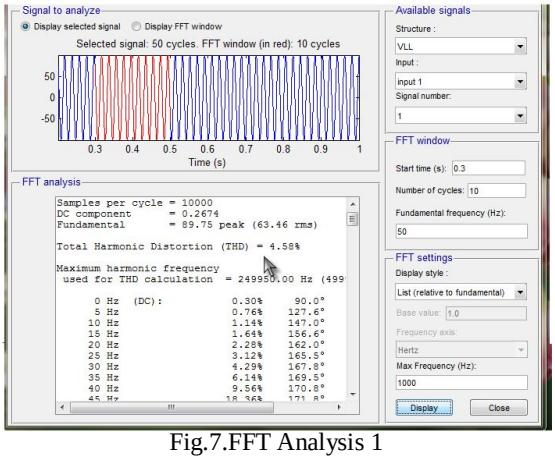


Fig.7.FFT Analysis 1

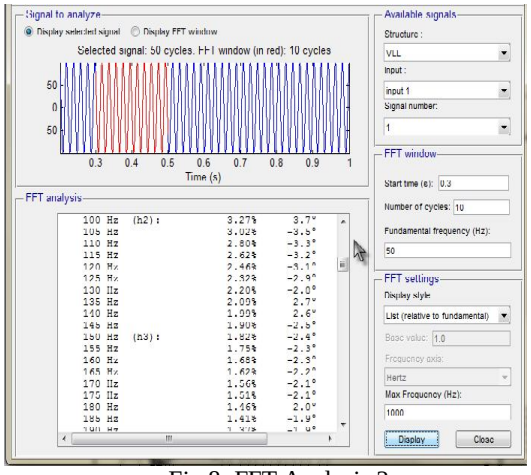


Fig.8. FFT Analysis 2

Fig 8. shows that total harmonic distortion of 100HZ and 150HZ. For a 100HZ it provides the 3.27% total harmonic distortion, for a 150HZ it gives the 1.82% total harmonic distortion. This multilevel inverter contains fourteen switches. Each dc sources has 100V it produces 1000V output voltage. This output voltage contains fewer amounts of harmonics. The output voltage of neutral point clamped inverter is shows in the fig.9.

This output voltage of neutral point clamped inverter contains some harmonics. By using low pass filter this harmonics are reduced. The filtered output voltage of neutral point clamped inverter is shows in fig.10. Then this filtered output voltage is separated by using of isolator and this output voltage without certain order harmonics is applied to high power applications, FACTS applications and renewable energy interface.

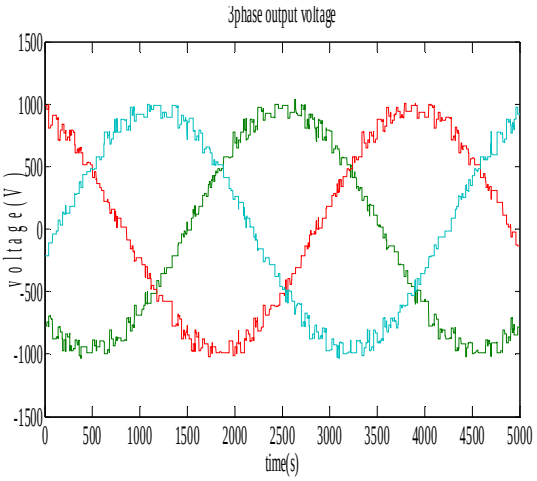


Fig.9. Simulation Result For 3 Phase Output Voltage.

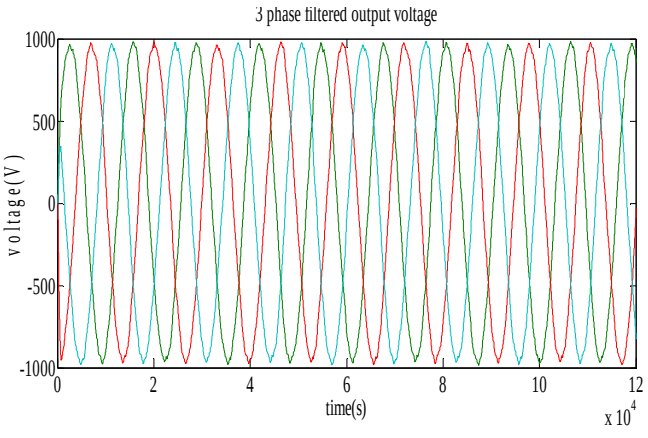


Fig.10. Three Phase Filtered Output Voltage.

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## VI. CONCLUSION

The disturbances in power electronics equipment are often periodic and rich in higher harmonics. They have been frequencies and are often above the bandwidth of regulators used to control fundamental components. Therefore the 'regular' control can only partially reduce their effects on the distortion of control variables. This hysteresis control technique enables us to obtain better selective harmonic reduction in the output AC voltage. Finally, we obtained the output AC voltage waveform. Besides that, it realized better multilevel output and achieved desired results. Balance the voltage of the dc split capacitors of 15-L neutral point clamped inverter, and reduce the harmonics when multi carrier PWM modulation is employed. The total harmonic distortion is reduced to 4.58%.The number of level is increase in the Neutral point clamped multilevel inverter in order to reduce the selective harmonics elimination and to increase the voltage gain and power quality.

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