



# LOW POWER FRACTIONAL-N PLL FREQUENCY SYNTHESIZER USING 45NM VLSI TECHNOLOGY

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**ABSTRACT:** power has become one of the most important parameter in various communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. This paper presents the design and simulation of VLSI based low power fractional- N Phase locked loop frequency synthesizer for Bluetooth application. Among variety of frequency synthesis techniques , phase locked loop (PLL) represents the dominant method in the wireless communications industry. PLL, like most wireless communication technologies, is relatively new and has matured only in the last decade. This phase locked loop is designed using VLSI technology, which in turn offers high speed performance at low power. For improving the performance of fractional-N phase locked loop, Loop filter and Sigma-Delta modulator are the most important factors. The loop filter bandwidth limits the speed of switching time between the synthesized frequencies. The Periodic operation of dual modulus divider introduces phase noise in the PLL. To eliminate this phase noise, the digital Sigma-Delta modulator is used which generates a random integer number with an average equal to desired fractional ratio and pushes the spurious contents to higher frequencies. Noise shaping concentrates the quantisation noise produced at the PFD output into the higher frequencies where it is removed by the low-pass filter.

**Keywords:** Sigma-Delta modulator; Phase Noise, Phase Locked Loop; Fractional-N Frequency Synthesizer

## I. INTRODUCTION

PLL is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal. A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another.

Phase lock loop is an electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e. lock) on the frequency of an input or reference signal. . It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. A phase locked loop (PLL) can be divided into two architectures, an integer-N PLL and a fractional-N PLL. The fractional-N PLL solves the trade-off issue between channel spacing and loop bandwidth found in the integer-N PLL, offering a lower phase noise, higher frequency resolution and a larger loop bandwidth. The output frequency of the fractional-N PLL is  $f_{out} = (N.\alpha) * f_{ref}$ , where N is an integer, and  $\alpha$  is the fractional part. A dual modulus divider is used to average many integer divider cycles over time to obtain the desired fractional division ratio. The main problem of this method is that by using the dual modulus divider periodically generates a spurious tones that is called fractional spur. The best method to remove the fractional spurs is using a Sigma-Delta Modulation technique. Basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure 1.

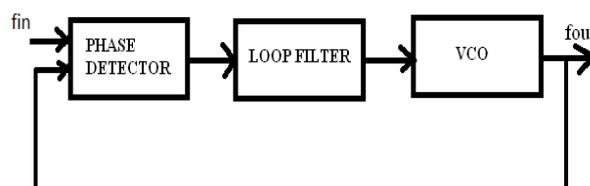


Figure 1. Block Diagram of PLL

A phase detector or phase comparator is a frequency mixer, analog multiplier or logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL).

Three components are connected as a feedback system. The reference signal is periodic such as square wave which is compared with the output of VCO using a phase detector. The output of phase detector is then applied to the low pass filter and used as a control signal to drive a VCO. The VCO will lock onto the reference signal thus can be used to tracked a periodic signal as its phase and frequency varies.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to recover a signal from a noisy communication channel, generate stable frequencies at a multiple of an input frequency (frequency synthesis), or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz. Frequency is the time derivative of phase. Keeping the input and output phase in lock step implies keeping the input and output frequencies in lock step. Consequently, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency.

Due to the current demand in communication technology, the proposed Fractional-N phase-locked loop or phase lock loop (PLL) is decided to design using 45 nanometre (nm) CMOS/VLSI technology to achieve the low power consumption and high stability. The main novelties related to the 45nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. Here for the design using VLSI technology, microwind 3.1VLSI backend software is used. This software allows designing and simulating an integrated circuit at physical description level. For low power, low leakage transistors will be used and will Compromise on little bit frequency. VLSI is dominated by the CMOS technology and much like other logic families, this too has its limitations which have been battled and improved upon since years. Taking the example of a processor, the process technology has rapidly shrunk from 180 nm in 1999 to 60nm in 2008 and now it stands at 45nm and attempts being made to reduce it further (32nm).

As the number of transistors increase, the power dissipation is increasing and also the noise. If heat generated per unit area is to be considered, the chips have already neared that of the nozzle of a jet engine. At the same time, the Voltage scaling of threshold voltages beyond a certain point poses serious limitations in providing low dynamic power dissipation with increased complexity. The number of metal layers and the interconnects be it global and local also tend to get messy at such nano levels.

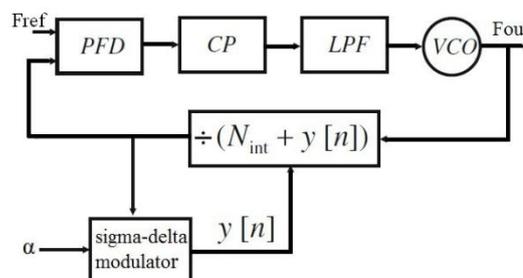


Figure 2. Block Diagram of PLL using Sigma-delta fractional –N frequency synthesizer

The proposed fractional N-PLL is shown in figure 2. It consist of Phase detector, low pass filter, charge pump, voltage controlled oscillator and Sigma delta modulator. Phase detector suitable for square wave signals can be made from an exclusive-OR (XOR) logic gate. Phase detector is a comparator that compares the input frequency  $f_s$  with output frequency of VCO and generates a d.c voltage that is proportional to the phase difference between the two frequencies. The function of the low pass filter is to remove high frequency components from the output of the phase detector. This low pass filter controls other characteristics of the PLL including bandwidth, capture range, lock range and transient response. The VCO is the most important functional unit in the PLL. The VCO is commonly used for clock generation in phase lock loop circuits.

The proposed work consists of additional sigma delta modulator block with fractional input. This block gives DC output proportional to the fractional inputs which then add with divide by N integer value.

## II. IMPLIMENTATION OF PLL USING 45 NM VLSI TECHNOLOGY

### A. Phase detector

The first block of Phase Locked Loop is the phase detector. The phase detector of the PLL is the XOR gate. The XOR gate output produces a regular square oscillation when the clock input and signal input have one quarter of period shift ( $90^\circ$  or  $\pi/2$ ). For other angles, the output is no more regular. A phase detector suitable for square wave signals can be made from an exclusive-OR (XOR) logic gate. When the two signals being compared are completely in-phase, the XOR gate's output will have a constant level of zero. The XOR detector compares well to the analog mixer in that it locks near a  $90^\circ$  phase difference and has a square-wave output at twice the reference frequency. The square-wave changes duty-cycle in proportion to the phase difference resulting. Applying the XOR gate's output to a low-pass filter results in an analog voltage that is proportional to the phase difference between the two signals. Figure 4. shows layout of Phase detector and figure 5. shows output waveform.

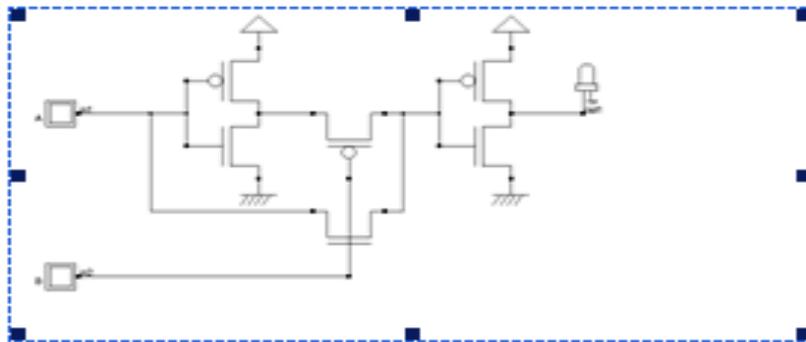


Figure 3.CMOS circuit of Phase Detector

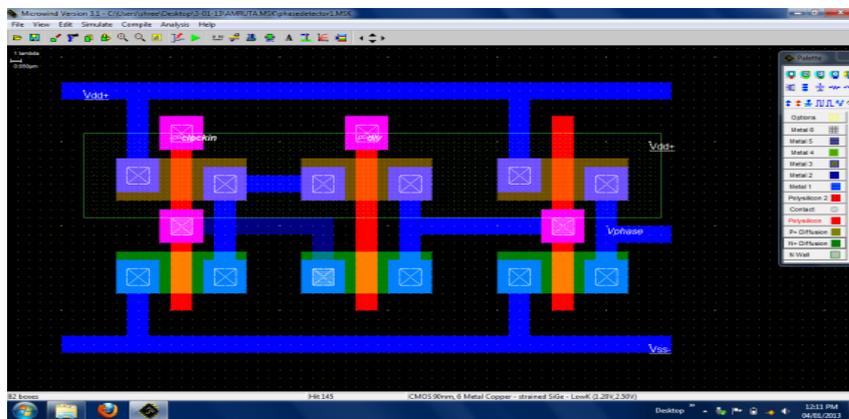


Figure 4.Layout of Phase Detector

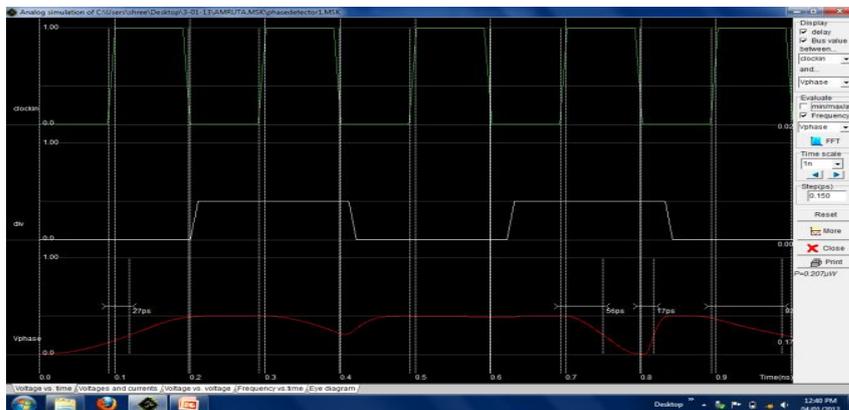


Figure 5.Voltage vs Time output

### B. Loop filter

Filters are the electronic circuits used alongwith rectifiers to get pure d.c. voltage. These are basically frequency selective circuits which select the band of frequency and attenuate the frequencies out of the band. Loop filter is used to filter out the unwanted spur and also suppress noise of the control line for VCO. This helps the overall phase noise. Here the filter may simply be a large capacitor C charged and discharged through the  $R_{on}$  resistance of the switch. The  $R_{on}C$  delay creates a low-pass filter. Figure 6. Shows a CMOS circuit of XOR gate with the output charged with a large capacitor and a serial resistance to create the desired analog control voltage.

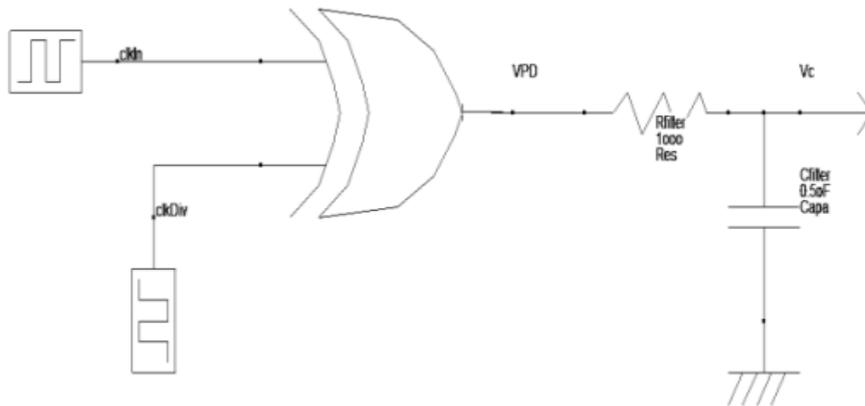


Figure 6.CMOS circuit of Filter

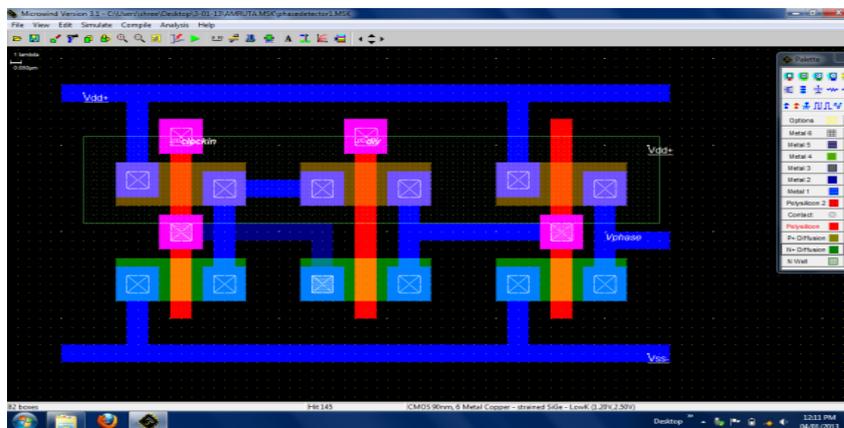


Figure 7.Layout of Loop filter

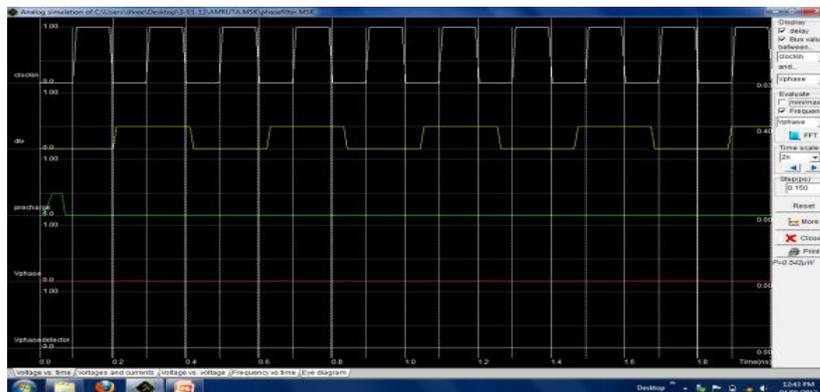


Figure 8.Voltage vs Time output





### III.CONCLUSION

The current technology up to 2008-2009 was 90 nm technology. Hence considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the selection of 45nm technology for the proposed project is the proper choice of technology. To implement fractional N-PLL using VLSI technology, first each block of PLL such as Phase detector, loop filter and VCO had been implemented using 45nm CMOS technology with microwind 3.1 backend software of VLSI. For individual blocks of PLL, analog circuits are designed using CMOS transistor and power consumption found less. Thus very efficiently phase detector, loop filter and VCO are designed. In remaining part of design all these blocks will be cascaded to have the fractional N-PLL.

### REFERENCES

- [1] N. Fatahi and H. Nabovati, "Design of low power fractional-N frequency synthesizer using sigma delta Modulation technique," 27<sup>th</sup> International Conference of Microelectronics, IEEE, 2010.
- [2] Ms. Ujwala A. Belorkar and Dr. S. A. Ladhake, "Design of low power phase lock loop using 45nm VLSI technology" International journal of VLSI design & Communication Systems ( VLSICS ), Vol.1, No.2, June 2010
- [3] Aamna Anil and Ravi Kumar Sharma, "A high efficiency charge pump for low voltage devices," International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012
- [4] B. K. Mishra, Sandhya Save and Swapna Patil, "Design and Analysis of Second and Third Order PLL at 450MHz" International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011
- [5] Kyoungho Woo, Yong Liu, Eunsoo Nam, and Donhee Ham, "Fast-Lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidths" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 2, FEBRUARY 2008 379
- [6] Michael H.Perrott July 2008, "Fractional-N Frequency Synthesizer Design Using The PLL Design Assistant and CppSim Programs"