Low Power High Speed Differential Current Comparator

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ABSTRACT: A low power high speed differential current comparator having weak current operation has been presented in this paper. The comparator proposed is a three stage process. It utilizes a modified Wilson's current mirror circuit for current to voltage conversion for its first stage followed by differential amplifier stage and buffer stage. The current comparator is simulated using Cadence Virtuoso 0.18μm CMOS technology and it can successfully generate valid output response for a range of input frequencies. Working at a supply of 1.8V, the comparator is capable of sensing a minimum difference of 22nA for 4μA reference current. In addition power dissipation of this circuit is as low as 226μW and shows a swift response resulting in a propagation delay which is less than 0.8ns for an input difference of 1μA.

KEYWORDS: current comparator, Wilson's current mirror comparator, single-ended differential amplifier, buffer, inverter

I. INTRODUCTION

Current mode comparator in CMOS technology has gained a lot of attention in the past years [1]-[4]. Due to the switch from voltage mode to current mode operation in numerous digital and analog circuits, current comparator has become one of the important building blocks. The striking attributes of the current mode approaches over voltage mode are the possibility of large bandwidth, high speed, better noise figure and smaller supply voltage. Current comparator finds its applications in circuits like current steering DACs where fast computation is necessary, neuromorphic electronic system [5] where less area occupancy is an important factor and also in circuit requiring low current comparison for the detection of minute current signals such as in temperature sensors and photo sensors.

The basic purpose of current comparison process is to compare the two currents flowing into the comparator and distinguish if the current is higher or lower in comparison with the reference current. Although the logic behind the comparison is fairly simple but its execution becomes complex. The circuit implementation becomes more critical when detection of very low current at high speed is required. The first consideration for building a current mode comparator is low input impedance followed by swift time response.

II. REVIEW OF WILSON'S CURRENT MIRROR COMPARATOR

Fig. 1 shows the existing Wilson's current comparator [1]. The circuit completes two tasks: 1) it generates the current difference between the input current and the reference current; 2) it reduces the input impedance by means of negative feedback within the circuit.

M1-M4 are connected in an improved Wilson current mirror topology and M5 is a diode connected load. The circuit compares the reference current I_{ref} with the input current I_{in}. The operation of the circuit is as follows: the reference current flowing through M3 makes the current at the drain node of M1 and M2 equal to I_{ref}. This results in the drain current (output current) flowing through M4 to become equal to the subtracted current between reference current and input current. Thus if I_{in} is greater than (or less than) I_{ref}, the output current I_o decreases (or increases) pulling up (or down)the voltage at the output node. The input impedance is very low given by eq.(1),

$$R_{in} \cong \frac{1}{g_{m2} + g_{m4} + g_{m1}g_{m4}(r_{o1} \parallel r_{oB})} \tag{1}$$

However if transconductance, g_m, is same for M1-M4, then eq.(2) follows,

$$R_{in} \cong \frac{1}{g_m^2 (r_{o1} \parallel r_{oB})} \qquad (2)$$

where g_m is the transconductance of the MOS transistors, r_{o1} and r_{oB} are the drain-source impedence of M1 and biasing current source I_b.
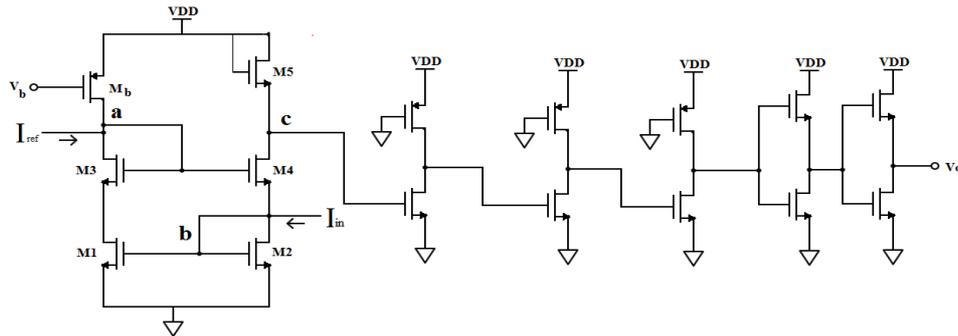

Fig.1. Wilson's current mirror comparator

III. PROPOSED CURRENT COMPARATOR

A stage wise vision of the proposed comparator is presented here which are as follows:

A. *Current to Voltage Converter Circuit:*

The Wilson's current mirror comparator circuit suffers from a few drawbacks such as poor power supply noise rejection and other intrinsic limitation faced by a single ended topology. Due to limited voltage swing at node c in Fig.1 it suffers from high offset current which makes it incompatible to be used in circuits where detecting current in the range of nA at high speed is necessary. To overcome these difficulties the circuit is modified to propose a differential current comparator employing the Wilson current mirror comparator presented in [1] with added modification for better performance.
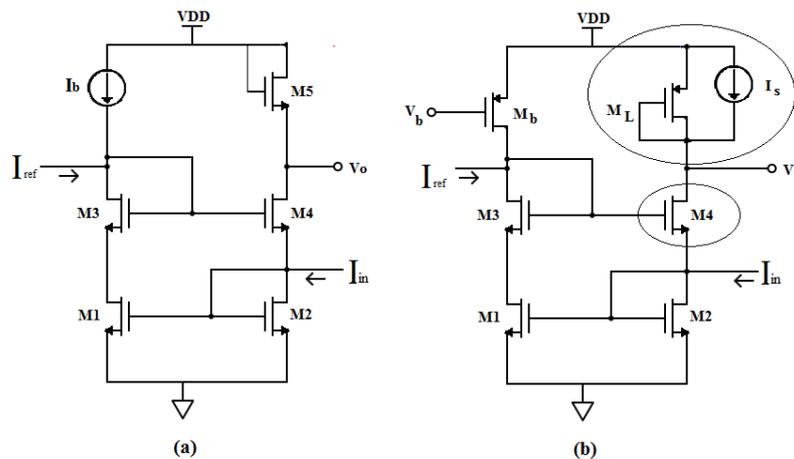

(a) **(b)**

Fig.2. Circuit diagram of (a)Existing Wilson's current mirror comparator (b) Modified Wilson's current mirror comparator

For increasing the voltage swing at the output the following modifications are made as shown in Fig. 2(b):

- Using common-source stage with diode connected PMOS load topology instead of NMOS load. Since PMOS load does not consume voltage headroom as a result of which a higher swing is conveyed to the output in comparison to NMOS load.
- The gain is further increased by adding a constant current source I_s which is equal to $0.33I_{d4}$ as shown in Fig. 2(b). This is because for a given $|V_{GSL}-V_{thL}|$, if the current decreases by a factor, say X, then $(W/L)_L$ must

decrease which in turn lowers $g_{mL}=\sqrt{2\mu_L C_{ox}(W/L)_L I_{DL}}$ by the same factor, thus increasing the gain of the circuit.

- To further decrease the response time while discharging of the charge at the output, Vo, $(W/L)_4$ is made twice of $(W/L)_3$.

B. *Dual input single-output differential amplifier:*

The second stage circuit employs a differential pair with active current mirror configuration [7] which is used for amplification of the differential input and converted into a single-ended output shown in Fig. 3. Hence the outputs from the first stage is then connected to the inputs of the differential amplifier for additional amplification. The operation of the differential stage is as follows: When V_{in} is less than V_{ref}, M_1 is turned off. Since M3 and M4 forms a basic current mirror path, no current flows through M4 and thus V_o roughly approaches zero. When difference between Vin and V_{ref} is small, M2 and M4 becomes saturated creating a high gain at the output. When V_{in} is much greater than V_{ref}, current through M1 increases. Due to mirror effect the drain current of M4 also increases and correspondingly current through M2 gradually drops to zero turning it off. This drives M4 into deep triode region resulting in Vo to approach VDD. However, to obtain a high swing at the output, the input common mode level must be kept as low as possible, i.e. $V_{GS1}+V_P$.
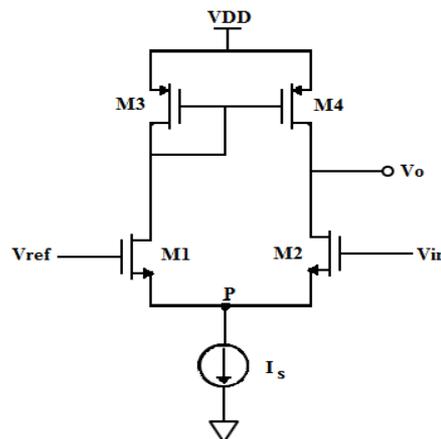

Fig.3. Single-ended Differential Amplifier

Thus the voltage gain of the partial differential amplifier stage can be evaluated to,

$$A_V \cong g_{m1,2}(r_{02} \| r_{o4}) \tag{3}$$

C. *Buffer:*

Stage 3 comprises of two buffer which in turn consists of two series connected inverters to generate rail-to-rail voltage swing at the output.

IV. **COMPLETE CIRCUIT VIEW OF PROPOSED CURRENT COMPARATOR**

Fig. 4 shows the full block diagram of the proposed current comparator. The input and reference current are first feed to the modified Wilson's current mirror. A local reference current I_b is used in this stage. Two separate Wilson's current mirror blocks generate two output voltage pertaining to two difference currents I_b-I_{ref} and I_b-I_{in}. The differential amplifier amplifies the difference and feeds the output to the buffer to regenerate the voltage logic at the output.
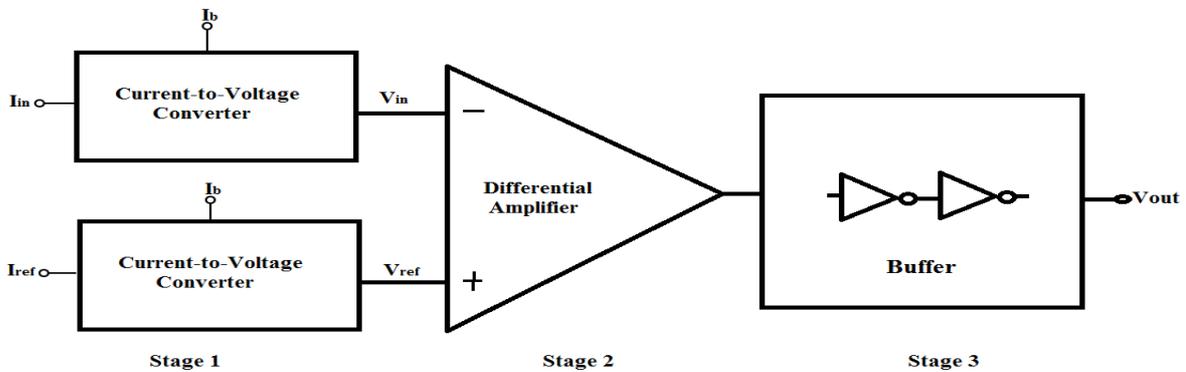
Fig.4. Block diagram of proposed current comparator

V. SIMULATION RESULTS

The proposed differential current comparator is designed in 180 nm CMOS technology using Cadence Virtuoso tool and simulated with Spectre. The frequency response of the differential amplifier is shown Fig. 5. The overall gain is found to be 28dB and bandwidth is 1.4 GHz. The phase cross over at 0dB is 75°. Fig. 6 shows the current inputs to the comparator and its computed voltage output at no-load condition. The comparator is subjected to an input frequency of 250 MHz and reference current of 4μA with a difference of 1μA at its input. Propagation delay of 0.76 ns is found including delay in the buffer stage. The overall average power dissipation at no-load condition is 226.8 μW. Fig. 7 and Fig. 8 shows the schematic design and layout of the comparator and it consumes an area of 945 um^2. A supply voltage of 1.8 V is applied for proper execution. For a high input switching frequency of 250 MHz the circuit shows good power-delay product as well as offset.

The proposed comparator works for a wide range of frequencies from 100 MHz to 1 GHz. Table I shows the change in power and delay reading for different input frequency at 1 μA input difference. It should be noted that the sensitivity degrades with increase in input sampling rate. The minimum offset recorded by the circuit is +10/-15 nA for 4 μA reference current at 100 MHz input frequency. From the simulated result it is visible that increasing input current difference decreases propagation delay. Chart 1 summarises delay for different process corners at frequency 250MHz. Chart 2 shows the dependency of power on temperature at frequency 250 MHz.

Comparison between the proposed and existing differential current comparator in [6] shows the power dissipation has reduced by approximately 63% and delay has reduced from 0.95 ns to 0.73 ns operating at a frequency of 500 MHz. Charts 3 and Chart 4 shows the comparison between the existing and proposed circuit in terms of power and delay.
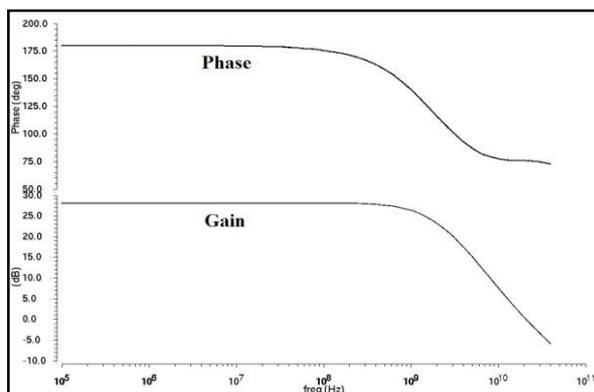

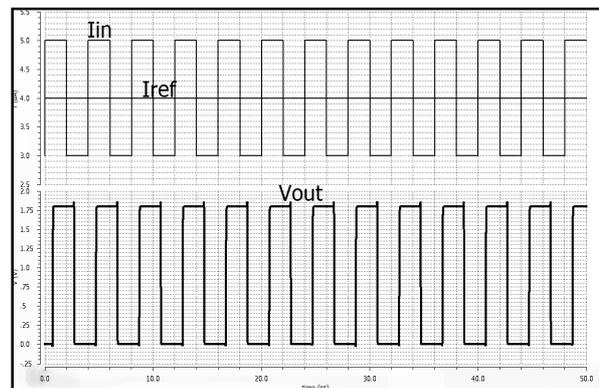Fig.5. Gain and phase curve of the pre-amplifier

Fig.6. Output response of the comparator for 1μA input difference and 250 MHz input frequency
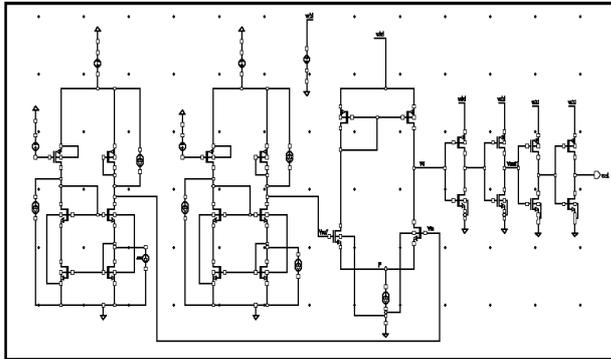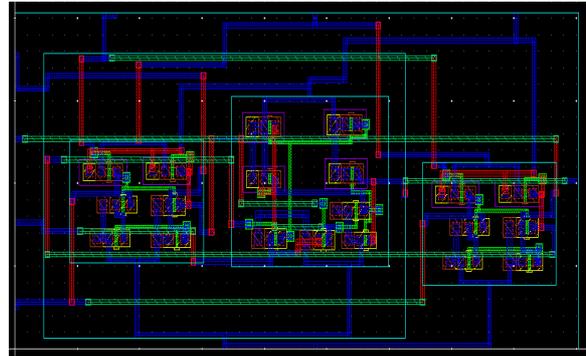
Fig.7. Schematic of proposed current comparator
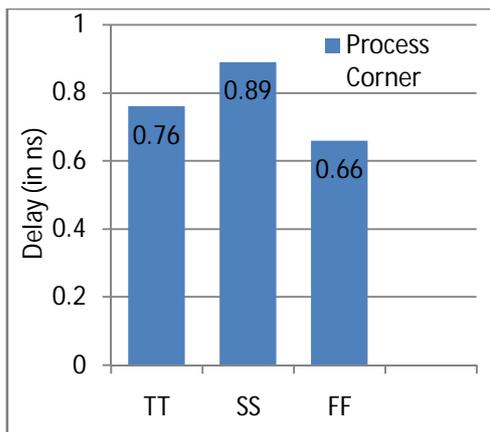

Fig.8. Layout of the proposed comparator
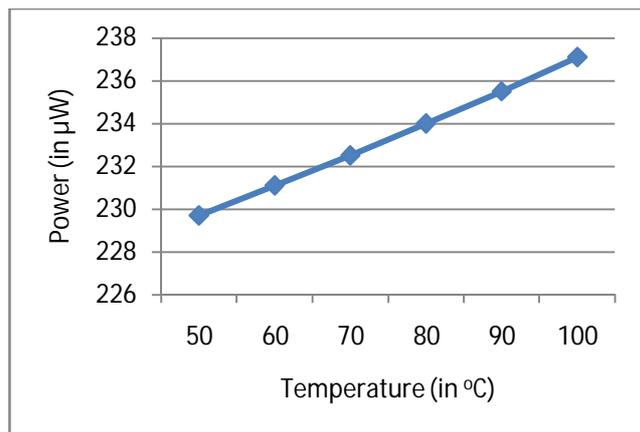

Chart 1: Delay variation with typical process corners

Chart 2: Dependency of power on temperature

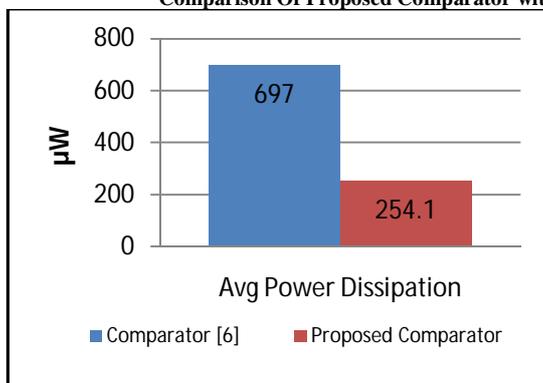**Comparison Of Proposed Comparator with existing Differential Current Comparator[6]**
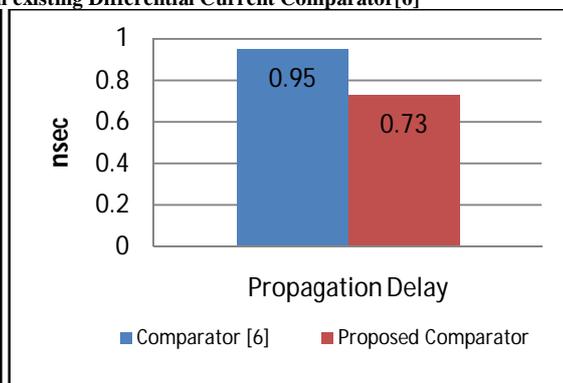

Chat 3: Average power dissipation comparison

Chart 4: Propagation Delay comparison

Table 1
Power and Delay variation with input current frequency

Input Frequency	Avg. Power Dissipation	Propagation Delay
100 MHz	209.6 µW	0.75 ns
200 MHz	220.9 µW	0.76 ns
250 MHz	226.8 µW	0.76 ns
500 MHz	254.1 µW	0.73 ns
1 GHz	301.8 µW	0.57 ns

VI. CONCLUSION AND FUTURE WORK

A simple differential current comparator is proposed for enhancing speed and reducing power dissipation. It is capable of detecting weak current for a large range of frequencies. Sensing a current as low as 15nA, with the input current changing at a speed of 100 MHz. The circuit utilizes Wilson's current mirror topology for current to voltage conversion, the outputs of which are feed to a single-ended active current mirror differential amplifier followed by a series of inverters to get a full swing at the output. The power and delay product is within reasonable range and can be used in circuits like current steering DACs where performance of the current comparison block is of utmost importance.

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BIOGRAPHY

Miss. Indrani Roy is a student pursuing Master of Technology in VLSI and Embedded System under School of Electronics Department at Kalinga Institute of Industrial Technology, Bhubneswar, India and would graduate in the year 2015. She has completed her B.Tech from IE&IT, Durgapur, affiliated to WBUT. Her research interest is in the field of analog electronics.

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