Multilevel Converter for Immunity in VSC HVDC Transmission

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ABSTRACT- Recent advances in technology have realized the diode clamped topology to have a considerable reduction in switching losses and the ability to control the harmonic content. Control methods based on selective harmonic elimination pulse-width modulation (SHE-PWM) techniques offer the lowest possible number of switching transitions. This feature also results in the lowest possible level of converter switching losses. For this reason, they are very attractive techniques for the voltage-source-converter-(VSC) based high-voltage dc (HVDC) power transmission systems. The paper discusses optimized modulation patterns which offer controlled harmonic immunity between the ac and dc side. The application focuses on the conventional two-level converter when its dc-link voltage contains a mix of low-frequency harmonic components. Simulation and experimental results are presented to confirm the validity of the proposed switching patterns. Finally a seven level Multilevel converter topology is applied for this application

Keywords-Amplitude modulation (AM), dc-ac power conversion, harmonic control, HVDC, insulated-gate bipolar transistor (IGBT), power electronics, power transmission system, pulse-width modulation, voltage-source converter (VSC).

I.INTRODUCTION

The continuous growth of electricity demand and ever increasing society awareness of climate change issues directly affect the development of the electricity grid infrastructure. The utility industry faces continuous pressure to transform the way the electricity grid is managed and operated. On one hand, the diversity of supply aims to increase the energy mix and accommodate more and various sustainable energy sources. On the other hand, there is a clear need to improve the efficiency, reliability, energy security, and quality of supply. With the breadth of benefits that the smart grid can deliver, the improvements in technology capabilities, and the reduction in technology cost, investing in smart grid Technologies has become a serious focus for utilities [1].

Advanced technologies, such as flexible alternating current transmission system (FACTS) and voltage-source converter (VSC)-based high-voltage dc (HVDC) power transmission systems, are essential for the restructuring of the power systems into more automated, electronically controlled smart grids. An overview of the recent advances of HVDC based on VSC technologies is offered in [2]. The most important control and modeling methods of VSC-based HVDC systems and the list of existing installations are also available in [2]
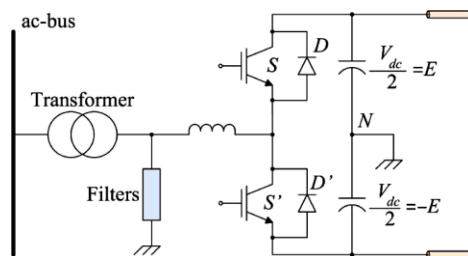.

Fig. 1. Phase of the two-level VSC for the HVDC power transmission system
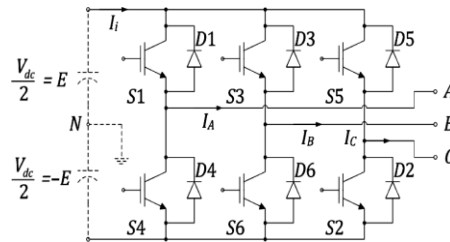
Fig. 2. Three-phase two-level VSC.

The first generation of utility power converters is based on current-source converter (CSC) topologies [3], [4]. Today, many projects still use CSCs due to their ultra-high power capabilities. With the invention of fully controlled power semiconductors, such as insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs) [5], the VSC topologies are more attractive due to their four-quadrant power-flow characteristics [6]. A typical configuration of the VSC-based HVDC power transmission system is shown in Fig. 1 as it is shown in [7] and [8].

With the continued increase of power and voltage levels, stress on cost effective solutions and stringent guidelines for power quality, multilevel converters have emerged as a technically viable solution for accomplishing acceptable standards. The term 'Multilevel' has been coined to emphasize the ability to increase the instantaneous voltage levels in steps, accomplished by addition of components in series. The basic topologies that have been studied so far are namely: Diode Clamped, Flying Capacitor, Cascaded H-bridge and the Modular Topology. Although the different topologies offer a variety of advantages, they however, also possess some limitations with further increase in voltage levels..

Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [5-11]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems voltage clamping requirement, circuit layout, and packaging constraints.

On the other hand, optimized modulation methods offer many advantages toward tight control of converter-generated harmonics [19]. A minimization method to find the complete set of solutions by solving the SHE-PWM equations for two-level inverters is discussed in [20]. In this paper, the dc-link voltage is assumed to be constant. In [10], a method is proposed to prevent the dc-link ripple voltage from creating low-order harmonics on the ac side of fixed and variable frequency inverters. However, only one of the multiple SHE-PWM sets [20] of solutions is reported.

An investigation of the harmonic interaction between the ac and dc side for STATCOM is presented in [21] including the so-called dynamic SHE-PWM scheme based on pre calculated angles for better THD. However, the dynamic SHE-PWM scheme is applied only for a three-level converter and can be applied only for known magnitude and frequency of the ripple. Another method for improving the harmonic performance of a two-level VSC with SHE-PWM is studied in [22]. However, only one set of SHE-PWM solutions is considered for the method of [22] which requires the exact values of magnitude, phase, and frequency of the ripple in order to be implemented.

Control strategies to compensate unbalances are reported in the literature. Mild imbalances caused by unbalanced loads of the ac side are regulated by using separate control loops for the positive- and negative-sequence components of the voltage as proposed in [23]. Efficient control of unbalanced compensator currents can be achieved by a control algorithm based on the D-STATCOM model [24]. D-STATCOM allows separate control of positive- and negative-sequence currents and decoupled current control of the d-q frame. An advanced strategy based on direct power control under unbalanced grid

voltage conditions has been recently presented for a doubly fed induction generator [25]. To take the full advantages of VSCs for HVDC power transmission systems, an auxiliary controller is added to the main controller which is conventionally implemented in the positive-sequence d-q frame [26]. To compensate for unbalanced ac-side loads, the auxiliary controller is implemented in the negative-sequence d-q frame.

The objective of this paper is to discuss the effectiveness of optimized modulation based on pre-calculated SHE-PWM in a two-level three-phase VSC to make the ac side immune from the fluctuations of the dc link without the use of passive components. However, since the VSC studied here does not include a closed-loop controller, strategies to compensate unbalances are not addressed in this paper.

This paper is organized in the following way. In Section II, a brief analysis of the VSC and the modulation method is provided. Section III contains the characteristics of the method on a VSC with dc-side ripple voltage. Section IV provides extensive experimental results to support the theoretical arguments. Conclusions are documented in Section V.

II. ANALYSIS OF THE PWM CONVERTER AND SHE-PWM

The optimized SHE-PWM technique is investigated on a two level three-phase VSC topology with IGBT technology, shown in Fig. 2. A typical periodic two-level SHE-PWM waveform is shown in Fig.3. The waveforms of the line-to-neutral voltages can be expressed as follows:

$$V_{LN} = \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = V_{dc} \begin{bmatrix} \sum_{n=1}^{\infty} A_n \sin n\omega_0 t \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t - \frac{2\pi}{3}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{2\pi}{3}\right) \end{bmatrix} \quad (1)$$

When ω_0 is the operating frequency of the ac, and
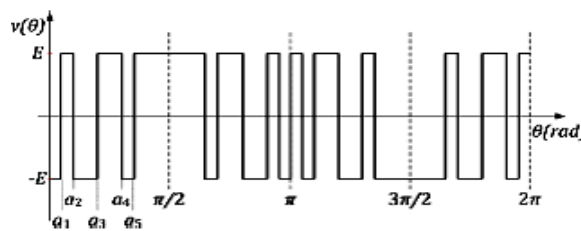V_{dc} is the dc-link voltage.

Fig. 3. Typical two-level PWM switching waveform with five angles per quarter cycle.
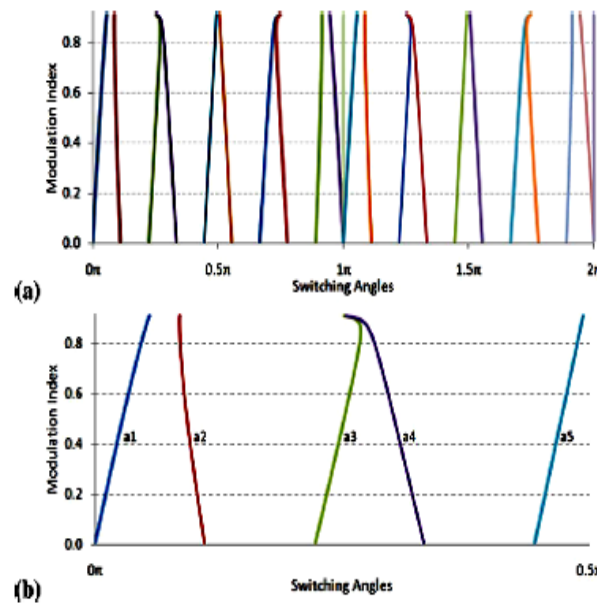
Fig. 4. Solution trajectories. (a) Per-unit modulation index over a complete periodic cycle. (b) Five angles in radians.

Thus, the line-to-line voltages are given by

$$V_{LL} = \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} \sqrt{3}.V_{dc} \begin{bmatrix} \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{\pi}{6}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t - \frac{\pi}{2}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{5\pi}{6}\right) \end{bmatrix} \quad (2)$$

The SHE-PWM method offers numerical solutions which are calculated through the Fourier series expansion [20] of the waveform

$$M = 1 + 2 \sum_{i=1,2,3.....}^{N+1} (-1)^i cos(\alpha_i)$$

$$O = 1 + 2 \sum_{i=1,2,3.....}^{N+1} (-1)^i cos(k\,\alpha_i) \quad (3)$$

Where N+1 are the angles that need to be found.

Using five switching angles per quarter-wave in (N=4)SHE-PWM, k= 5, 7, 11, 13 to eliminate the 5th, 7th, 11th,and 13th harmonics. During the case of a balanced load, the third and all other harmonics that are multiples of three are cancelled, due to the 120 symmetry of the switching function of the three-phase converter. The even harmonics are cancelled due to the half-wave quarter-wave symmetry of the angles, being constrained by

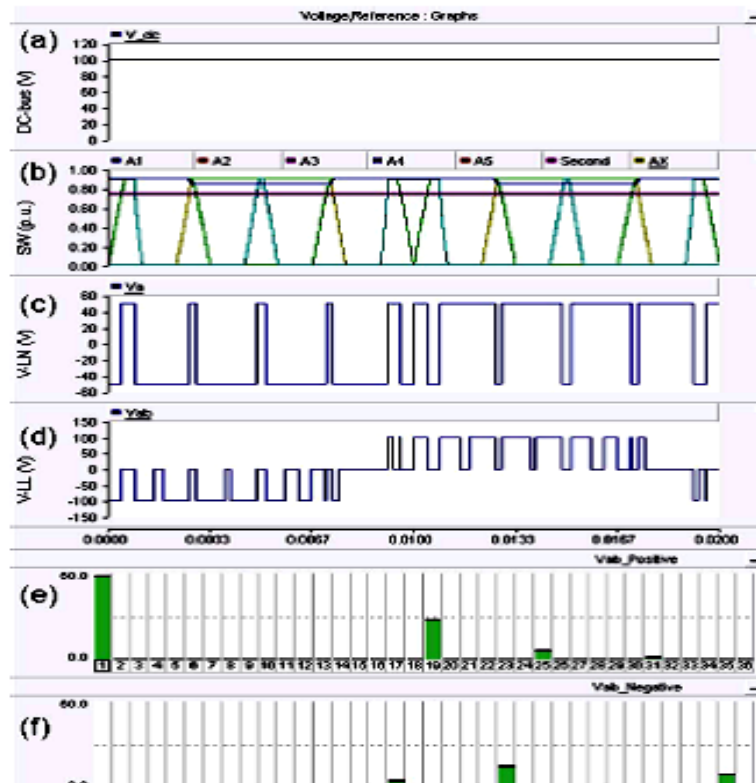$$0 < \alpha_1 < \alpha_2 ... . < \alpha_{N+1} < \pi/2$$

Fig. 5. Simulation results for SHE-PWM eliminating 5th, 7th, 11th, and 13th harmonics. (a) DC-link voltage. (b) Solution trajectories to eliminate harmonics and intersection points with the modulating signal (M=0.75). (c) Line-to-neutral voltage. (d) Line-to-line voltage. (e) and (f) Positive- and negative-sequence line-to-line voltage spectra, respectively.
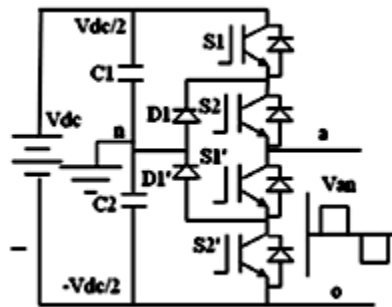
III. Diode Clamped Multilevel Converter

Fig. 6 Three level DCMLI

Fig.6 shows the circuit diagram of the 3-level Diode clamped multilevel inverter.

Switching States	Output Voltage
S_1, S_2	$V_{dc}/2$
S_2, S_1'	0
S_1', S_2'	$-V_{dc}/2$

Table I 3-LEVEL SWITCHING STATES

Table I shows the switching states of the 3-level Diode clamped multilevel inverter with the switching states of V_0, 0 and -V_{dc}
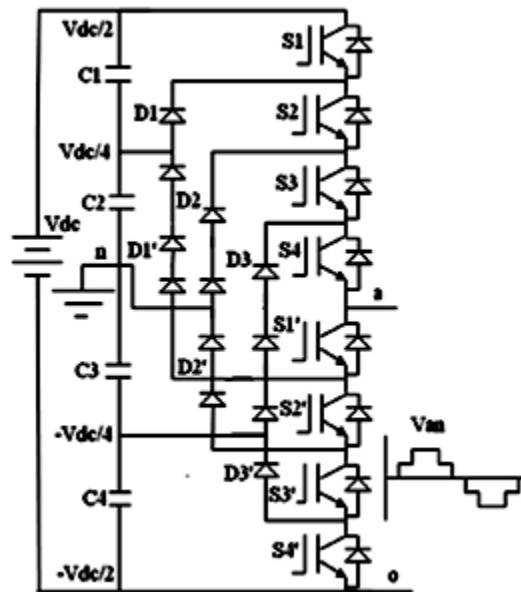

Fig.7 Five level DCMLI

Fig.7 shows the circuit diagram of the 5-level Diode clamped multilevel inverter

Switching States	Output Voltages
S1,S2,S3,S4	Vdc
S2,S3,S4,S1'	Vdc/2
S3,S4,S1',S2'	0
S4,S1',S2',S3'	-Vdc/2
S1',S2',S3',S4'	-Vdc

Table 2 SWITCHING STATES OF 5-LEVEL DCMLI

Table II shows the switching states of the Diode clamped multilevel inverter.

IV. SIMULATION RESULTS

Modeling of Diode Clamped Multilevel Converter

Fig.8 shows the Matlab/Simulink Model of three level Diode clamped multilevel converter.
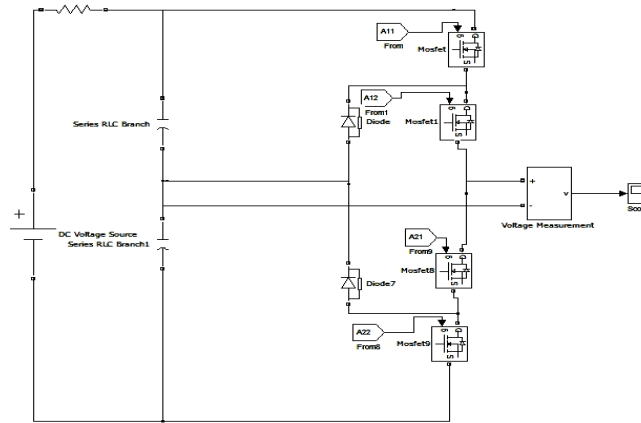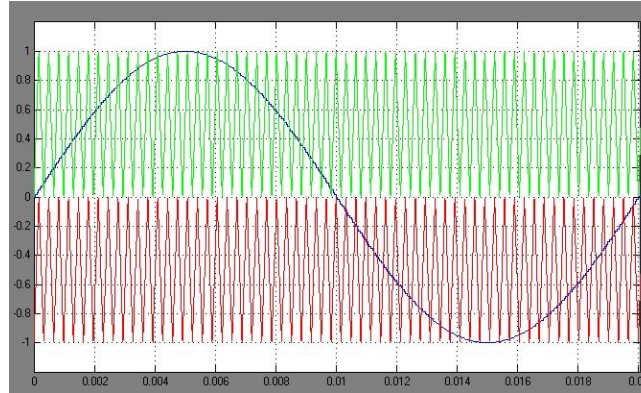

Fig.8 Simulink model three level DCMLI

Fig.9 Reference and carrier waveforms

Fig.9 shows the Level shifted Carrier PWM wave form. Here two carriers each are level shifted and are compared with sine wave.
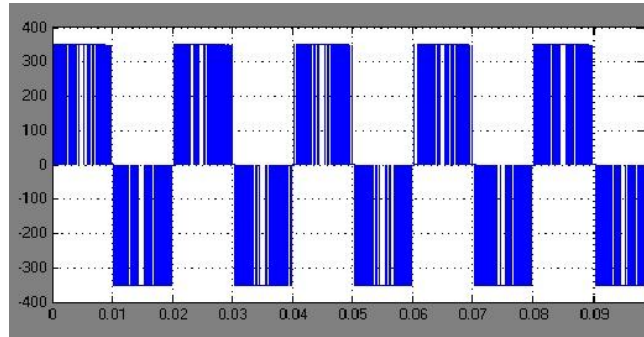
Fig.10. Output voltage

Fig.10 shows the three level output voltage waveform.
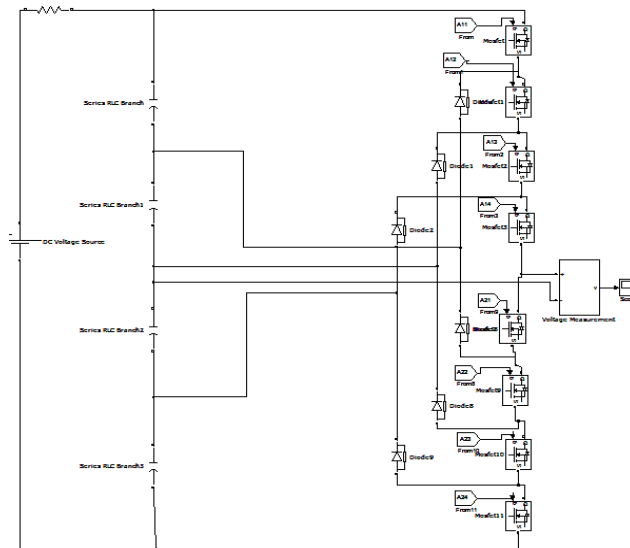
Case 2

Fig.11Simulink model of the 5-level DCMLI

Fig.11 shows the Matlab/Simulink Model of five level Diode clamped multilevel converter.
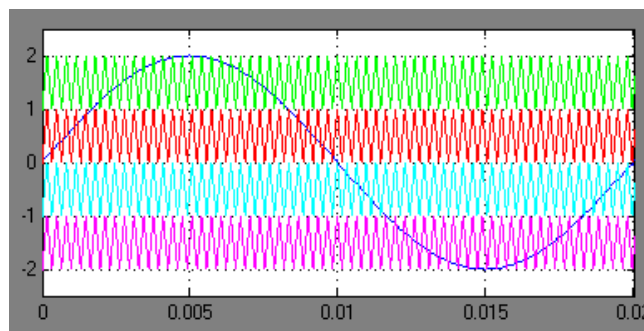

Fig.11 Reference and carrier waveforms

Fig.11 shows the Level shifted Carrier PWM wave form. Here four carriers each are level shifted and are compared with sine wave.
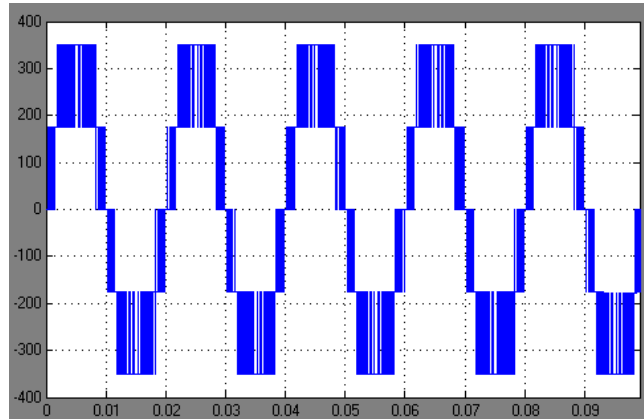

Fig.12. Output voltage

Fig.12 shows the five level output voltage waveform of the diode clamped multilevel inverter.
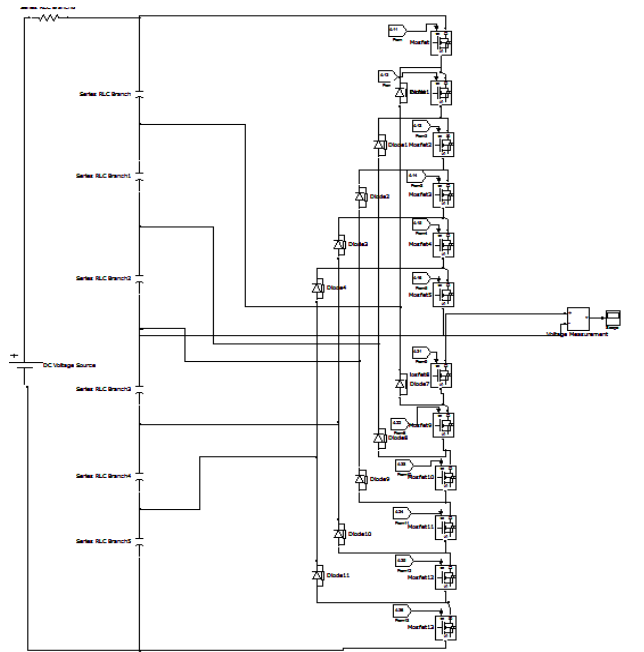

Fig.13 Simulink model of the DCMLI

Fig.13 shows the simulink model of the Seven level diode clamped multilevel inverter.
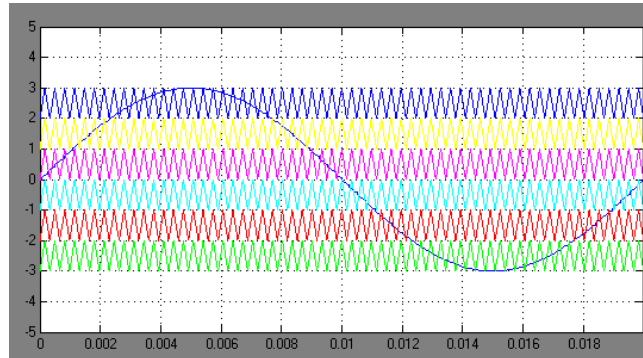
Fig.13 Reference and carrier waveforms

Fig.13 shows the Level shifted Carrier PWM wave form. Here four carriers each are level shifted and are compared with sine wave.
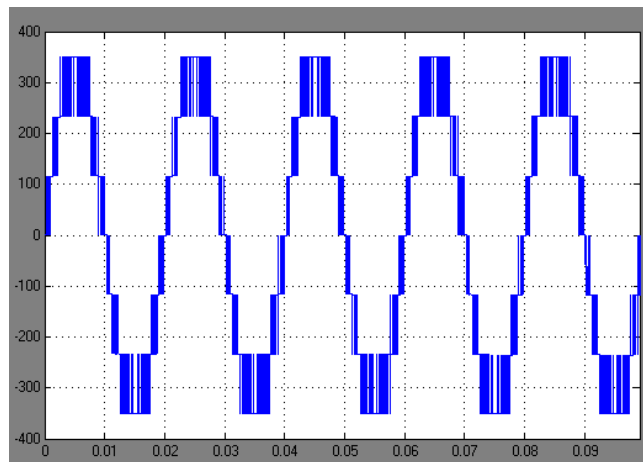

Fig.14. Output voltage

Fig.14 shows the five level output voltage waveform of the diode clamped multilevel inverter

V CONCLUSION

   This paper presents Diode Clamped multilevel converter. The three-level converter using the modular topology was simulated for the same voltage and power rating as the two-level converter. With higher levels, the use of PWM does not offer significant benefit as we have increased losses hence, SHE modulation strategy was utilized and the results were compared for increasing delay angles. For the same power and voltage rating, higher levels of the modular topology, were also simulated. Higher levels, implies the use of more number of submodules to generate intermediate steps in the instantaneous voltage wave to make it more sinusoidal. Finally a seven level single H-bridge is proposed. A SIMULINK based model is developed and Simulation results are presented.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 2, Issue 6, June 2013

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