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Ultra-Low Power Design of Digital CMOS Logic Circuits

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ABSTRACT: Power and area are the two major concerns in design of any digital circuit. At present scenario low power device design and its implementation have got a significant role in the field of nano electronics. However much research not has been done at ultra-low power with acceptable performance and high performance design with power. To achieve the ultra-low power requirement is to operate the digital logic gates in subthreshold region. This paper investigates the analysis of CMOS technology in 45 nm channel length where the relative study of average power dissipation of CMOS inverter. We analyze and compare CMOS Inverter and other logic gates in subthreshold region. The subthreshold current is found to be exponentially related to the gate voltage. Thus,this exponential relationship not only gives an exponential reduction in power consumption, but also an exponential increase in delay. The simulation results are taken at 45nm using CMOS technology with the help of Cadence tool**.** The simulation results show that the reduction in power outweighs the increase in propogation delay.

KEYWORDS: Ultra-low power, CMOS Inverter, subthreshold circuits.

I. INTRODUCTION

The power consumption is today the major issue in design of integrated circuits for portable devices. Also the heat dissipation is a problem for high performance integrated circuits.In the medium performance, medium power consumption design region, numerous optimization efforts have been made [1,2,3]. CMOS power dissipation has been increasing due to the increase in power density as shown in [8].From the last few decades the CMOS technology has emerged as a predominant technology in the field of nano electronics. As the technology has become compact there is rapid increase in demand of high performance and low power digital systems. The subthreshold circuits, the supply voltage is reduced well below the threshold voltage of transistor[4].The low power consumption of an integrated circuit can be achieved by running the digital circuits in subthreshold mode. In subthreshold MOSFET operation,current density is very low and the ratio of the transconductance to bias current of the device is (gm/Id) maximum [12].Static (leakage) power optimization can be exploited by using multiple thresholds, transistor stacking, etc [11].The other advantage of operating the circuit in subthreshold mode is that we are able to exploit the subthershold leakage current as the operating drive current.

II. RELATED WORK

The subthreshold current is exponentially related to the gate voltage .This exponential factor is expected to exponentially reduce the power consumption and at the same time brings an exponential increase in propagation delay .This paper focuses the analysis of CMOS technology in 45 nm channel length where we examine the average power dissipation of CMOS inverter. We analyze and compare CMOS Inverter and other logic gates in subthreshold region.In Section 3 we will discuss about the power minimization techniques. In section 4 we will do an analysis of subthreshold CMOS circuit. In section 5 Subthreshold CMOS Inverter is analysed with simulated results .In Section 6 shows the comparison results of subthreshold logic CMOS Inverter with other known low-power logic. The Section 7 concludes the paper.

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III. POWER MINIMIZATION TECHNIQUES

a) Voltage Scaling

Voltage scaling is perhaps most effective method of saving power due to the square law dependency of digital circuit active power on the supply voltage[6].The total power consumption can be represented by

$$P_{total} = \alpha C_{total} * Vdd^2 f_{clk} + Vdd * Ioff \ldots\ldots (1)$$

The first term in equation 1 represents dynamic or switching power , while the second term represents static power which happens due to the leakage in the design. Vdd scaling is the preferable method implemented for low power design but it decreases the speed of circuit as Vgs-Vt is reduced. Supply voltage scaling enhances the gate delays unless the threshold voltage of the transistors are also scaled down. If threshold voltage is being reduced more and more then there is a rise in the leakage current of transistors .

b) Reducing the physical Capacitance

Digital circuits have three types of capacitance: gate capacitance, diffusion capacitance an interconnect capacitance. If all the three components are scaled down as well by the same factor, then the net power dissipation is scaled down as well. Gate and diffusion capacitance are fixed during the cell design, whereas Intercell and global interconnect capacitances can be controlled by the CAD tools performing the global routing [7]. Physical capacitance mainly reduces by the transistor sizing [8].

c) Reducing The Switching Frequency

Reducing the number of “0”to „1” power dissipating transitions minimize the switching power dissipation of the gate .This can be achieved by lowering clock frequency and lower signal activity.Using half frequency on clock distribution network will save approximately half of the power consumption on the clock distribution network [9], [10].

IV. ANALYSIS OF SUBTHRESHOLD CMOS CIRCUIT

The CMOS logic operates in the subthreshold mode when the power supply voltage(vdd) is less than the transistor threshold voltage (Vt), this ensures that all the transistors are operating in subthreshold mode.In subthreshold region , when Vds >3kT/q then it is observed that Ids becomes independent of Vds. This provides an excellent current source span for almost the entire rail to rail voltage range in analog design, where this characteristic is used extensively. In digital design, this characteristic can be advantageous as we will be able to use more series connected transistors .We use 45 nm process technology for our circuit simulation with Vt of PMOS and NMOS transistor as - 0.1501V and +0.150047V respectively.418: The 3kT/q drop (about 78mV at T=300K) is practically negligible compared to the Vt drop in the normal strong inversion region[5].

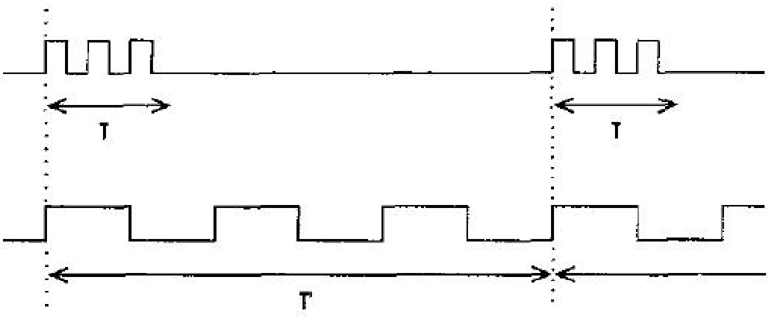

Fig.1 Subthreshold Circuit in Bursty Computation

Fig.1 it shows the Subthreshold Circuit in Bursty Computation,how it behaves with respect to time.

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At higher frequency , power consumption is linearly dependent with operation frequency .At same operating frequency subthreshold CMOS inverter consumes less power than strong inversion circuits. At lower frequency the power consumption becomes independent of operating frequency as the static power takes over .

V. SIMULATION AND RESULTS OF SUBTHRESHOLD CMOS INVERTER

The CMOS inverter is truly very important for all the digital designs. The electrical behaviour of complex circuits can be almost completely derived by deriving the results from inverters. Figure 2 shows the circuit diagram of a static CMOS inverter [1]. When Vin is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. A direct path exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. A path exists between Vdd and Vout , yielding a high output voltage.

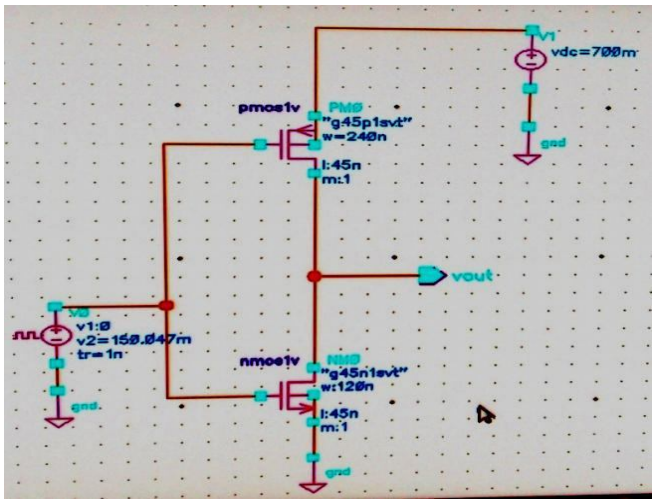

Fig .2 Static CMOS inverter

In the Fig 2.it shows the schematic diagram of Static CMOS inverter, which conists of one PMOS and one NMOS connected to the same input.

Table 1 Comparison of Delay, Avg. Power and PDP at different voltages at 27degrees

V_{DD}(V)	Delay	Average Power(P_{avg})
0.150047	$699.8e^{-3}$	$70.04e^{-12}$
0.14	$699.9\ e^{-3}$	$52.78e^{-12}$
0.13	$700\ e^{3}$	$39.18e^{-12}$
0.12	$700\ e^{-3}$	$30.93e^{-12}$
0.11	$700e^{-3}$	$22.58e^{-12}$

Table -1 shows delay and average power of static CMOS inverter at different voltages at 27 degrees temperature.

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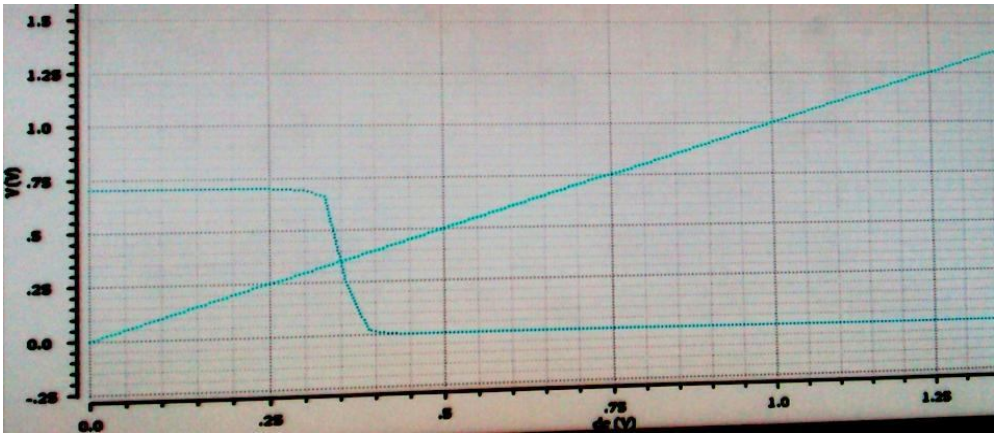

Fig .3 DC characteristics CMOS Inverter

The DC characteristics as obtained for CMOS inverter channel length 45nm shown below in Figure 3.The graph is between output voltage and input dc voltage.

VI. COMPARISION WITH OTHER DIGITAL LOGIC

Subthreshold circuits has lower PDP (power-delay product) because the reduction in power consumption outweighs the increase in delay by an order of magnitude.

Table -2 Comparision In Subthreshold Region(V_{DD}=0.150047V)

LOGIC	POWER(W)	DELAY(s)	PDP(J)
INVERTER	$70.04e^{-12}$	700	$490.28\ e^{-10}$
NAND	$311.8e^{-12}$	698.7	$2178.54\ e^{-10}$
NOR	$238.7e^{-12}$	696.2	$166.1829\ e^{-9}$

Table -3 Comparison In Strong Inversion Region(V_{DD}=0.3V)

LOGIC	POWER(W)	DELAY(s)	PDP(J)
INVERTER	$4.319e^{-9}$	700	$30.23\ e^{-7}$
NAND	$1.787e^{-9}$	698.7	$12.485e^{-7}$
NOR	$425.3e^{-12}$	696.2	$29.609\ e^{-8}$

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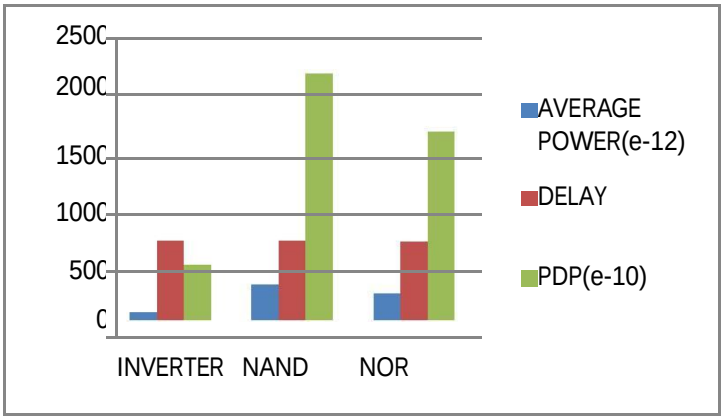
Table-2 and Table-3 show the comparison of CMOS inverter with 2 Input NAND and NOR logic gate in subthreshold region and in strong inversion.It table 3 and table 4 we can see that PDP of NAND gate is very high ,this is also one of the reason that why it is preferred.

Table-4 Performances of Different Logics



In Table-4 we can easily compare the average power , delay and PDP of inverter , NAND and NOR logic. Thus the comparative study of performances can be done .

VII. CONCLUSION

In this paper, we studied different characteristics of digital logic circuits operating in subthreshold region to achieve ultra-low power. The subthreshold logic can be easily implemented and derived from existing circuits by lowering the power supply voltage to be less than threshold voltage. The Subthreshold digital circuits are suitable for few applications which require very low power consumption.The few applications of this ultra low power digital logic circuit is seen in biomedical devices such as pace maker etc ,self-powered devices,wrist watch computation.and other different devices.Due to its slow performance, this subthreshold circuit is restricted to certain applications in which ultra-low power is mainly required.

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