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# 45 Nm MIGFET-Based ADC Design with Dithering

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**ABSTRACT**—In this paper, a multiple independent gate FET (MIGFET)-based flash type analog to digital converter (ADC) has been designed with dithering facility to improve the accuracy of the ADC. The comparators in the ADC have been realized using MIGFETs. The analog input signal is given to one gate of the MIGFET and the noise signal is given to another gate of the MIGFET. The functionality is verified in 45 nm technology node using TSPICE. The ADC performance metric, mean square difference (MSD) between the input signal and the output signal is studied for various mean values of the noise signal to get the optimum noise level.

# **KEYWORDS**— MIGFET, Dithering, MSD, ADC, TSPICE.

# I. INTRODUCTION

Dithering is an intentionally applied form of noise along with the input signal to reduce the quantization error. Most real-world signals are analog, whereas the analog to digital converter (ADC) output is digital. The ADC takes only discrete values at the output, all information in the intermediate value is lost. By adding small random noise signal at the input, it is possible to reduce the intermediate loss at output signal [1].

Scaling down of conventional bulk MOSFET leads to the short channel effects (SCE). To overcome these challenges quasi-planar multi-gate devices like FinFETs have emerged as a potential candidate. Double gate FinFET devices can be either simultaneously driven double gate (SDDG) devices where both the gates are biased simultaneously or independently driven double gate (IDDG) devices where the gates are biased independently. The IDDG devices can also be called as multiple independent gate field effect transistor (MIGFET) [2,3].

In this work, a 45 nm MIGFET-based flash ADC design has been presented. The functionality is verified using TSPICE. Since, the MIGFET has two independent gates one of the gates receives the analog signal to be

converted and the other gate is exploited for dithering i.e. to mix the noise signal to get the better accuracy. The rest of the paper is arranged as follows. Functionality of the MIGFET-based flash ADC with simulated results is discussed in section II. The Effect of dithering on MIGFET based ADC is discussed with simulation results in section III. Performance metric, mean square difference (MSD) between the real time random input and output signal are discussed in section IV. Finally section V gives the conclusion.

# II. SIMULATION METHODOLOGY

All the simulations in this study are performed using 45 nm MIGFET PTM model [4], in Tanner (TSPICE) circuit simulator. Figure 1 shows the 3 bit flash ADC circuit [5,6] used which consists of three major components namely resistive divider network, comparator and encoder. Generally, for an N bit converter the circuit employs 2<sup>N-1</sup> comparators. A resistive divider network provides reference voltage. The time varying voltage signal is given as input which is concurrently compared to the reference voltage levels provided by resistive divider network. The output of the comparator is a thermometer code which is given to encoder to get digital output signal. Table I gives the design specification of MIGFET based comparator. Figure 2 shows the MIGFET based comparator circuit used in flash ADC. The input transistors M1 and M2 are used in IDDG mode, and the remaining devices are used in SDDG mode in the below circuit.



Fig. 1 Three bit Flash ADC Circuit



Fig. 2 MIGFET -based Comparator Circuit used in Flash ADC

TABLE I DESIGN SPECIFICATION OF MIGFET BASED COMPARATOR

Parameter	Specification
Supply Voltage	$\pm 1 V$
Resolution	3-bit
CL	1.25fF
Cc	20fF
V <sub>out</sub> Range	±1V

The input sine wave signal is applied to the inverting terminal and a reference signal is given to the noninverting terminal in MIGFET based comparator (Fig. 2). Figure 3 shows the comparator output waveform.



The encoder circuit used for 3bit flash [5] ADC is shown in Fig.4 which converts the thermometer code to binary code. From the Table II by using K Map technique

below equations are derived.	
B0=A7A6+A6'A5+A4'A3+A2'A1	(1)
B1=A6+A4'A3+A3'A2	(2)



TABLE II TRUTH TABLE FOR ENCODER

Thermometer Code					Binary Code				
A7	A6	A5	A4	A3	A2	A1	B2	B1	B0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Fig. 6 shows the output waveforms of the ADC. Fig. 7 shows the DAC output waveform. The simplest way of describing the functionality of DAC is by its transfer function where B0 = LSB, B1 = Middle Bit, B2 = MSB.

$$DAC \_OUT = \{B0 + (B1 * 2) + (B2 * 4)\}$$
(4)

In 3 bit flash ADC, the input signal applied to the noninverting terminal is represented in Fig.6a. The reference voltage is given to inverting terminal. The output of the comparator is converted to binary code using encoder and then given to DAC. The corresponding DAC output is represented in Fig.7. An ideal DAC for 3-bit ADC will generate seven transitions.



Fig. 6 ADC output waveforms (a) input signal (b) MSB (c) Middle Bit (d) LSB



Fig. 7 DAC Output

 TABLE III

 Specification For MIGFET Based Flash Adc

Parameter	Specification
Technology	45nm
Resolution	3-bit
Power supply	1v
Input voltage range	0 to 1v
Frequency	10 MHz

## **III. DITHERING**

In this dithering technique, a real time signal (i.e. not a regular sine wave) (Fig. 9a) is given to gate1 and a noise signal is given to gate2 of MIGFET. Figure 9c depicts the output of DAC. The MIGFET based comparators (Fig. 8) offers the advantage that we can add noise to the transistor without disturbing the input signal. Due to dithering principle, the output effectively traces the input even below LSB level.



Fig. 8 Dithering in comparator





Fig. 9 Dithering (a) ADC input (b) Noise signal (c) DAC output

#### IV. RESULTS AND DISCUSSION

The mean square error (MSE) or Mean square difference (MSD) is one way to evaluate the difference between an estimator and the true value of the quantity being estimated. MSE measures the average of the square of the error, with the error being the amount by which the estimator differs from the quantity to be estimated.

$$MSE = \frac{1}{n} \sum_{i=1}^{n} (Input - Output)^2$$
<sup>(5)</sup>

Input= Input of ADC, Output= Output of DAC

The noise signals are generated in MATLAB using a function randn for a particular mean value, which was then exported to TSPICE and applied to the second gate of the MIGFET (M2) as shown in Fig.8. The simulations are repeated for noise signals generated with different mean values.

Mean of noise signal	Mean square difference
0	1.13879
0.1	1.103019
0.3	0.978414
0.5	1.105794
0.7	1.125771
1	1.133762

TABLE IV Performance Metric

Table IV shows the MSD between the real time input (input to ADC) and output of DAC along with noise signal of different mean values. Figure 10 shows the MSD as a function of noise mean values. It can be observed from Fig. 10 that a noise mean of 0.3 offers minimum MSD.



### V. CONCLUSION

In this paper, we designed a 45 nm MIGFET-based flash type ADC and investigated the effect of dithering in the designed ADC using TSPICE circuit simulator. A simple way to add the noise to get the performance enhancement using dithering has been demonstrated. The simulation results for various noise mean values confirms the dithering.

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#### REFERENCES

- M.F. Wagdy, "Effect of various dither forms on quantization errors of ideal A/D converters", IEEE Transactions on Instrumentation and Measurement, Vol. 38, NO. 4, pp. 850-855, August 1989.
- [2] Mayank Shrivastava, et al., "A Novel and Robust Approach for Common Mode Feedback using IDDG FinFET", IEEE Transactions on Electron Devices, vol.55, No.11, pp.3274-3282, 2008.
- [3] L.Mathew, et al., "CMOS Vertical Multiple Independent Gate Field Effect Transistor (MIGFET)" IEEE International SOI Conference, 2004.
- [4] Website http://ptm.asu.edu
- [5] Pradeep Kumar, Amit Kolhe "Design & Implementation of Low Power 3-bitFlash ADC in 0.18µm CMOS" International Journal of Soft Computing and Engineering (IJSCE)ISSN: 2231-2307, Volume-1, Issue-5, November 2011
- [6] Arunkumar. P. Chavan, G. Rekha, P.Narashimaraja"Design of a 1.5-V,4-bit Flash ADC using 90nm Technology" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-2, Issue-2, December 2012
- [7] M.F. Wagdy and W.M. Ng, "Validity of uniform quantization error model for sinusoidal signals without and with dither", IEEE Transactions on Instrumentation and Measurement, Vol. 38, pp. 718-722, June1989.
- [8] M.F. Wagdy, "Effect of various dither forms on quantization errors of ideal A/D converters", IEEE Transactions on Instrumentation and Measurement, Vol. 38,NO. 4, pp. 850-855, August 1989.
- [9] Mahmoud Fawzy Wagdy(1994), "Comparative ADC Performance Evaluation Using a New Emulation Model for Flash ADC Architectures" Circuits and Systems conference, pp. 1159-1163.
- [10] M.F. Wagdy and M. Goff, "Linearizing average transfer characteristics of ideal ADC's via analog and digital dither", IEEE Transactions on Instrumentation and Measurement, Vol. 43, No. 2, pp. 146-150, April 1994.