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55 Level Quasi Hybrid Cascaded Multilevel Inverter

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ABSTRACT: Multilevel Inverters (MLI) are suitable for high voltage and power applications because they can reduce voltage stresses and harmonic contents. Generally cascaded hybrid MLIs uses sinusoidal PWM strategies to generate multiple dc levels in the sinusoidal AC output for the reduced THD. In this paper 55 level Quasi Hybrid Cascaded Multilevel Inverter (QHCMLI) is developed with sinusoidal PWM strategy using simulink model. The obtained results are evaluated by the performance measures such as THD, root mean square, crest factor, form factor and distortion factor for various modulation index and shows that the performance QHCMLI using POD PWM scheme is satisfactory. QHCMLI is also designed with the proposed PWM strategy using reference signals generated by switching angle method and the simulated outputs are validated by comparing the performance with the conventional PWM strategy using the proposed PWM switching strategy the performance measure of PD, POD, and APOD is improved than the previous methods for high modulation index.

KEYWORDS: Cascaded MLI, PWM, PD, POD, APOD, THD, RMS.

I.INTRODUCTION

An effective and practical solution to reduce harmonics and to meet the increasing power demand is the multilevel inverter. The most common MLI topologies classified into three types are diode clamped MLI, flying capacitor MLI, and cascaded H-Bridge MLI. The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [5]. The 3-level diode clamped inverters, mostly a good solution for motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the diode clamped MLIs, when the level exceeds three. The Flying Capacitor-MLIs are based on balancing capacitors instead of diodes and generate multilevel output voltage waveform by capacitor clamping. To increase the number of output levels it requires more number of capacitor thus increasing the complexity of considering DC-link balancing. Among the three types of multilevel inverters, the cascade inverter has the least components for a given number of levels [3]. The cascade inverters also allow using various pulse width modulation (PWM) strategies to control the inverter accurately .A high magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced by connecting the number of DC levels using progressive methods. In this paper Quasi Hybrid Cascaded Multilevel Inverter (QHCMLI) is developed using various pulse width modulation (PWM) strategies.

II.RELATED WORK

Cascaded type of MLI has the least components for [9] the number of levels selected than the other types of MLI. H-bridges connected in series can be excited by several separate DC sources which may be fuel cell or PV cell. This leads to the applications of MLI in the interface of renewable energy sources and also in applications including inductions machine and motor drives, active rectifiers, filters, flexible AC transmission systems and static compensators. The cascaded MLI allows various pulse width modulation strategies [4] including selective harmonic elimination PWM (SHE-PWM), sinusoidal PWM (SPWM), space vector PWM (SVPWM) etc., The SPWM control method is very popular as it reduces the distortion harmonics by using several level shifting options on carrier signal. In SPWM a sinusoidal reference voltage waveform is compared with a triangular wave form to generate switching gate signals for

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the MLI [1]. The stepped sine PWM using several multicarrier signals [7] can also generate the pwm switching strategy for the harmonic reduction. The binary mode of selecting the dc supply for each H-bridge can be used by the MLI to increase the number of output levels to reduce the THD [6]. Binary type MLI with four H-bridges connected in series can generate ac sine output with thirty one levels whereas for the same 4 H-bridges using equal dc sources can output up to 9 levels. In this paper dc link sources for the four H-bridges connected in series use quasi method and it generates up to 55 levels of MLI output. The advantage of quasi method is the achievement of higher number of output levels without increasing the number of H-bridges.

III.QUASI HYBRID MLI

Fig. 1 shows the schematic of Quasi Hybrid Cascaded Multilevel Inverter (QHCMLI). QHCMLI consists of four

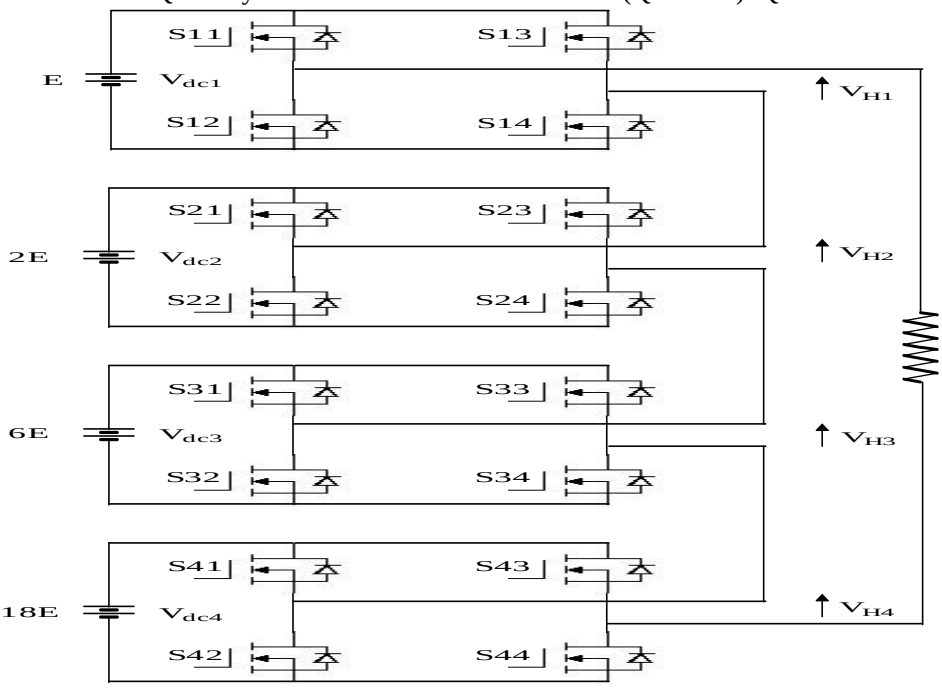

Fig. 1 Quasi hybrid cascaded multilevel inverter

H-bridges connected in series with separate dc sources. The ratio of dc sources selected for each H-bridge can be expressed as

$$V_{dci} = \begin{cases} E & i = 1 \\ 2 \times 3^{i-2} E & i \geq 2 \end{cases} \quad (1)$$

E is considered as the unit DC link voltage and V_{dci} represents the DC link voltage of the ith H-Bridges. In a four-HBs single phase

$$V_{dc1} = E \qquad V_{dc2} = 2E \qquad V_{dc3} = 6E \qquad V_{dc4} = 18E \quad (2)$$

It consists of 8 active switching states to make the output voltage depending on the switching condition of the switches. The output voltage of the ith H-Bridge is

$$V_{Hi} = F_i V_{dci} \quad (3)$$

F_i is the switching function. The value of F_i is 1 or -1 or 0. Table I shows the relationship of the F_i, V_{Hi} and states of switches. For the value 1, switches S_{i1} and S_{i4} are turned on and for zero, the switches S_{i1} and S_{i3} or S_{i2} and S_{i4} need to be turned on. Similarly for the value -1, switches S_{i2} and S_{i3} are turned on

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Table I Relationship of switching function output voltages and state of switches

F_i	V_{Hi}	S_{i1}	S_{i2}	S_{i3}	S_{i4}
1	V_{dci}	1	0	0	1
-1	$-V_{dci}$	0	1	1	0
0	0	1	0	1	0
0	0	0	1	0	1

IV.BIPOLAR MODULATION CONTROL SCHEMES

In general multicarrier based PWM strategies single bipolar with sinusoidal reference are used in MLI to produce switching patterns. The bipolar controlled sine signal is compared with fixed amplitude fixed/variable frequency triangular carrier signal. The number of carrier signals required to produce m level output is (m-1). The entire carriers having the fixed amplitude and fixed frequency are termed as (FAFF) and fixed amplitude and variable frequency as (FAVF). The reference signal is continuously compared with the carrier signal and whenever the reference signal is greater than carrier signal transient occurs from zero to one and otherwise one to zero is generated to form PWM.

$$m_f = \frac{f_c}{f_r} \tag{4}$$

The frequency modulation index is where m_f is the frequency modulation, f_c is the carrier signal and f_r is the reference signal. The amplitude modulation for Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) is

$$m_a = \frac{2A_r}{(m-1)*A_c} \tag{5}$$

Where m_a represents the amplitude modulation A_r is the reference amplitude and A_c is the carrier amplitude. The PWM strategies are developed using MATLAB/SIMULINK. In this paper hybrid cascaded type MLI using quasi mode for dc source selection is used to generate 55-level ac output.

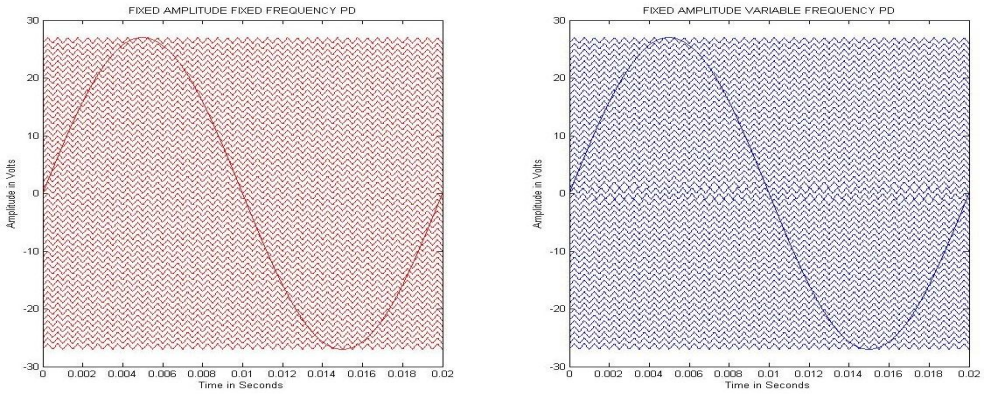

Fig. 2 Simulated Sine reference and multi-carrier signals for m_a = 1, m_f = 40 using FAFF PD PWM method and m_a = 1, m_f = 44 for lower switches and m_f = 40 for remaining switches using FAVF PD PWM method

The number of carrier signals used is 54 with 27 carriers on the positive side and 27 carriers on the negative side. A sinusoidal reference signals with different m_a is used to generate the switching patters for QHCMLI. Fig. 2 shows the generated reference signal with FAFF and FAVF 54 number of carriers arranged in-phase at different dc levels called as PD PWM method

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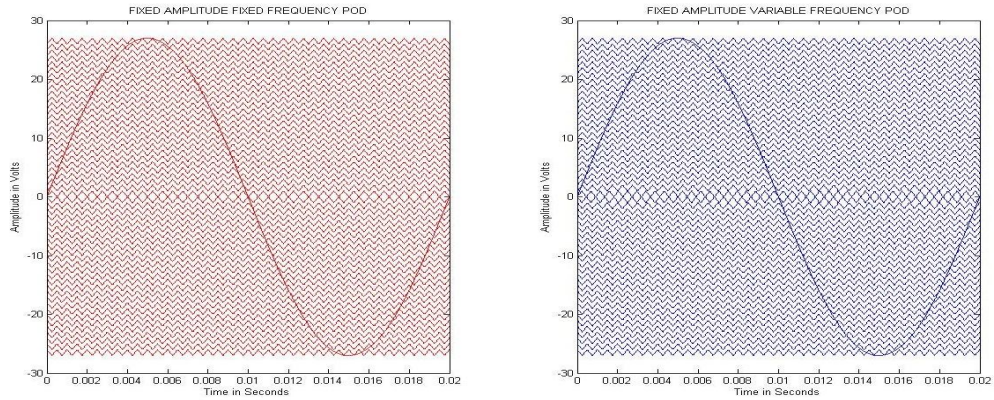

Fig. 3 Simulated Sine reference and multi-carrier signals for $m_a = 1$, $m_f = 40$ using FAFF POD PWM method and $m_a = 1$, $m_f = 44$ for lower switches and $m_f = 40$ for remaining switches using FAVF POD PWM method

Fig. 3 shows the phase opposition disposition (POD) PWM methods where the carriers are arranged in–phase and out of phase above and below the zero line.

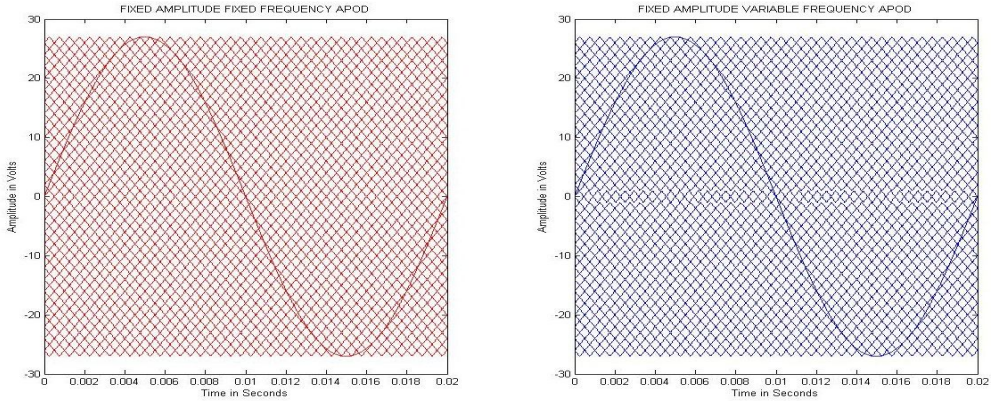

Fig. 4 Simulated Sine reference and multi-carrier signals for $m_a = 1$, $m_f = 40$ using FAFF APOD PWM method and $m_a = 1$, $m_f = 44$ for lower switches and $m_f = 40$ for remaining switches using FAVF APOD PWM method

Fig. 4 shows the APOD PWM method where the alternate carriers are in phase and adjacent carriers are out of phase. Sinusoidal reference is selected in the above Fig. 2, 3, & 4.

Proposed Bipolar Modulation Control Scheme

Stepped sine wave is used as reference instead of pure sine wave. Stepped angles to generate the proposed reference are calculated by switching angle method. There are different switching angle methods say Equal Phase method (EPM), Half Equal Phase Method (HWPM), Half Height Method (HHM) and Feed Forward Method (FFM).

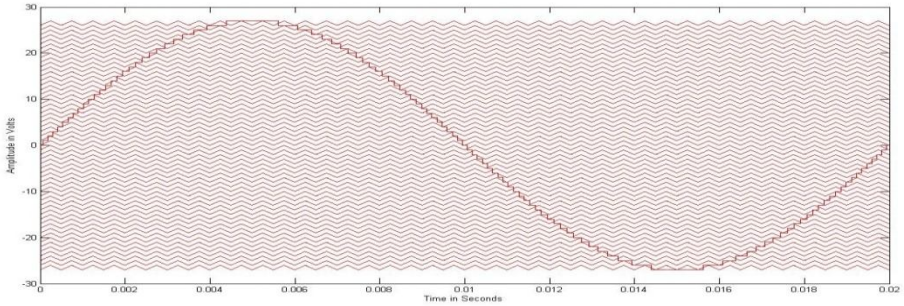

Fig. 5 Simulated Step reference and multi-carrier signals for $m_a = 1$, $m_f = 40$ using FAFF PD PWM method

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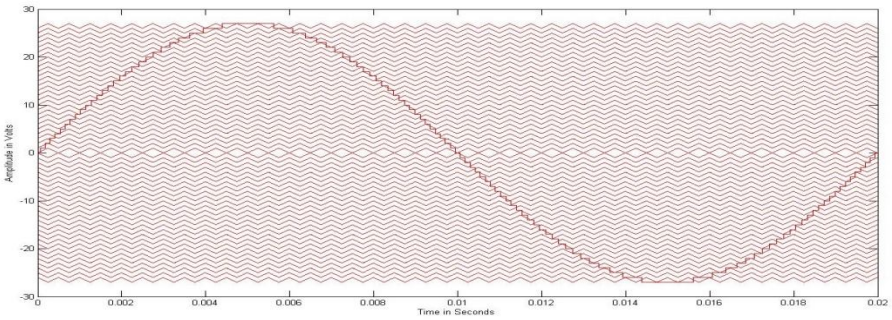

Fig. 6 Simulated Step reference and multi-carrier signals for $m_a = 1$, $m_f = 40$ using FAFF POD PWM method

Out of the above mentioned methods, half height method is selected for generating stepped sine reference because the other methods do not generate sine shaped reference. When the function value increases to the half-height of the level, the switch angle is set and thus better output waveform obtained. The main switching angles α_1, α_2..... α_m are determined where m represents the number of levels. Fig. 5, 6 & 7 shows the proposed stepped sine reference signal compared with multicarrier signal using FFFAPDPWM, FFFAPODPWM and FFFAAPODPWM strategies.

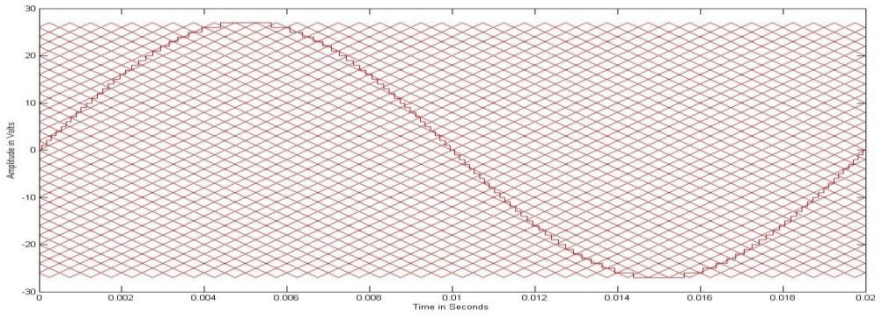

Fig. 7 Simulated Step reference and multi-carrier signals for $m_a = 1$, $m_f = 40$ using FAFF APOD PWM method

V. RESULT AND DISCUSSION

Fig. 8 shows the 55 level output of QHCMLI using FAFF and FAVF carrier signals and sine wave reference under PD,

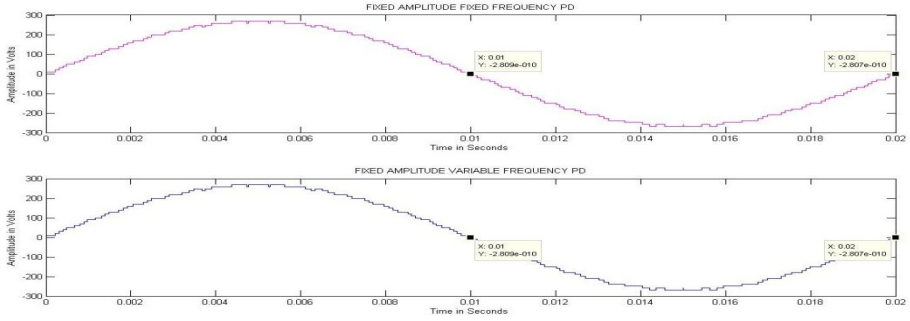

Fig (a)

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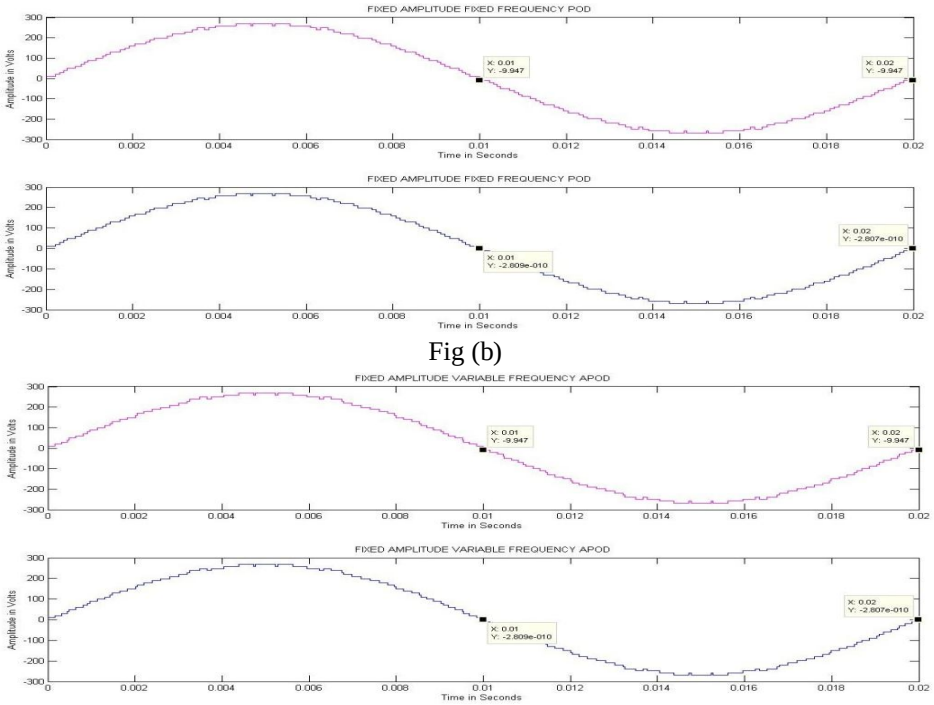

Fig (b)

Fig (c)

Fig. 8 One full cycle of 55 levels output voltage using FAFF and FAVF carrier signal and sine reference of QHCMLI (a) PD PWM (b) POD PWM (c) APOD PWM

POD and APOD PWM methods. In the Fig. 8 (b) and (c) the MLI output using FAFF carrier experiences zero shift error. Zero shift error is a non-zero amplitude value at t=0.01ms for a period of 0.02ms sine output. Zero shift error can be eliminated by using FAVF carrier signals. Zero shift error occurs in FAFF POD and APOD PWM method.

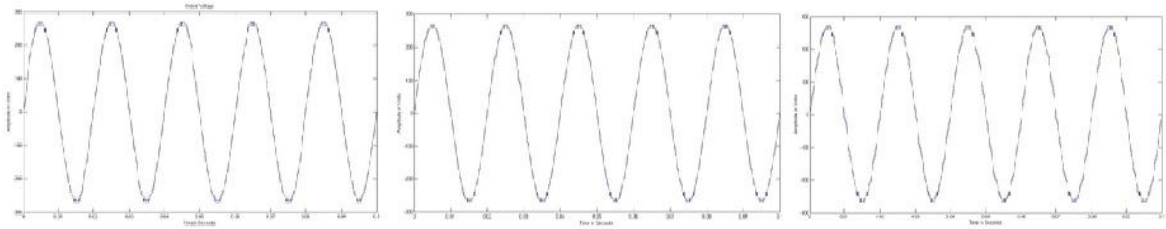

Fig. 9 Sine reference based 55 levels output voltage of QHCMLI PD, POD and APOD PWM

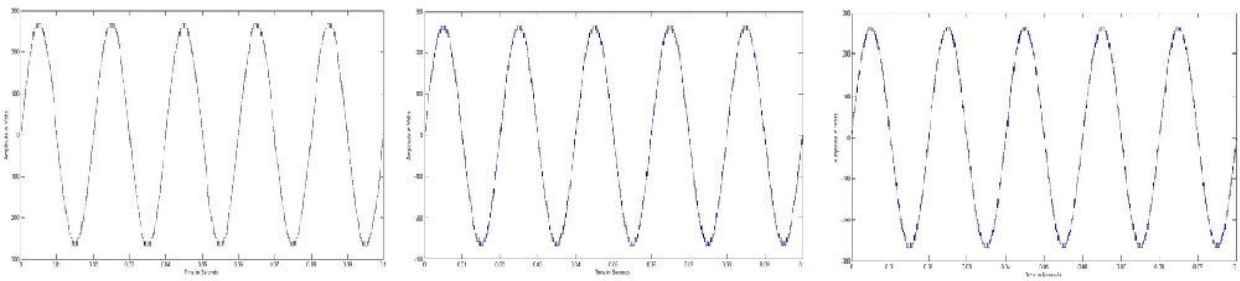

Fig. 10 Stepped sine reference based 55 levels output voltage of QHCMLI PD, POD and APOD PWM

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Fig. 9 & 10 shows the sine and stepped sine reference based 55 levels output voltage of QHCMLI PD, POD and APOD.

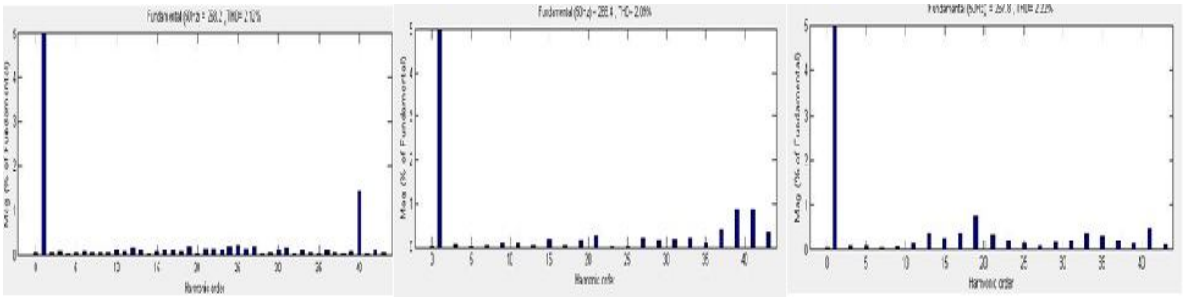

Fig. 11 FFT analysis of sine referenced 55 levels output voltage using FAVF PD, POD, and APOD PWM

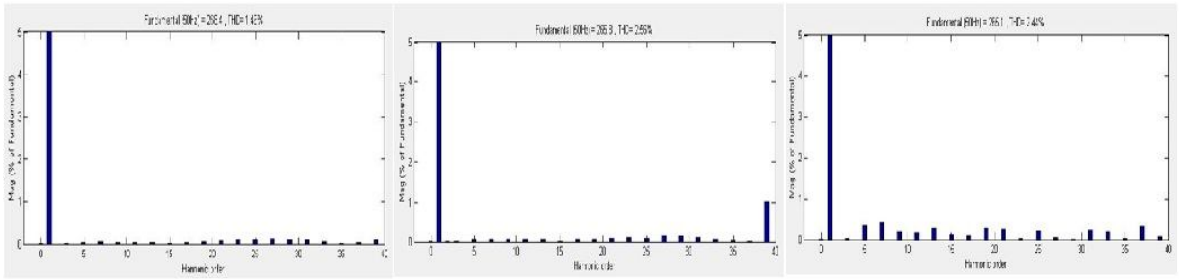

Fig. 12 FFT analysis of stepped sine referenced 55 levels output voltage using FAVF PD, POD, and APOD PWM

Fig. 11 & 12 represents the FFT analysis of sine and stepped sine reference based PD, POD and APOD.

Table II performance evaluation of 55 levels QHCMLI

PARAMETERS	Ma	Sine PWM Strategy						Proposed PWM strategy		
		FAFF [at 2000Hz]			FAVF [at 2200Hz]			FAFF [at 2000 Hz]		
		PD	POD	APOD	PD	POD	APOD	PD	POD	APOD
%THD	1	2.12	2.10	2.22	2.12	2.09	2.22	1.46	1.46	1.46
	0.99	2.18	2.19	2.16	2.17	2.19	2.16	2.43	2.56	2.44
	0.98	2.23	2.30	2.17	2.23	2.30	2.17	2.81	2.94	2.67
	0.97	2.23	2.19	2.15	2.22	2.19	2.14	2.80	2.88	2.58
V_{RMS}	1	189.7	189.8	189.3	189.7	189.8	189.3	189.8	189.8	189.8
	0.99	187.7	187.9	186.9	187.7	187.9	186.9	187.9	187.9	187.5
	0.98	186.2	186.1	185.7	186.2	186.1	185.7	186	186	185.4
	0.97	184.3	184	184	184.3	184	184	184.1	184.1	183.6
CREST FACTOR	1	1.4138	1.4141	1.4147	1.4138	1.4141	1.4147	1.4141	1.4141	1.4141
	0.99	1.4139	1.4141	1.4141	1.4139	1.4141	1.4141	1.4146	1.4146	1.4139
	0.98	1.4141	1.4142	1.4136	1.4141	1.4143	1.4136	1.4145	1.4145	1.4142
	0.97	1.4139	1.4141	1.4141	1.4139	1.4141	1.4141	1.4144	1.4144	1.4139
FORM FACTOR	1	3162	INF	INF	3794	INF	INF	INF	INF	INF
	0.99	2681	INF	INF	3128	INF	INF	INF	INF	INF
	0.98	4655	INF	INF	4655	INF	IBF	INF	INF	INF
	0.97	1843	INF	INF	1843	INF	INF	INF	INF	INF
DISTORTION FACTOR	1	1.3E-4	5.8E-5	1.1E-4	1.5E-4	5.8E-5	1.1E-4	2.3E-5	2.3E-5	2.3E-5
	0.99	3.2E-4	4.9E-5	2.5E-4	3.4E-4	4.7E-5	2.5E-4	3.4E-5	3.3E-5	1.6E-4
	0.98	1.0E-4	5.7E-5	1.6E-4	8.6E-5	5.7E-5	1.6E-4	4.9E-5	3.8E-5	2.8E-4
	0.97	2.0E-4	8.2E-5	1.1E-4	1.8E-4	8.2E-5	1.1E-4	4.2E-5	1.8E-5	1.7E-4

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Table II shows the analysis of 55 levels QHCMLI for reduction in harmonics and DC bus utilization using the performance indices say THD, V_{RMS}, crest factor, form factor, Distortion factor. The performance measures are carried out for different amplitude modulations ranging from 0.97 to 1.00 using different PWM methods. The performance evaluations are also carried out with carriers under FAFF and FAVF. Carriers with FAVF are designed to enhance exact zero crossing of the sinusoidal AC output at the middle value of the time period. Usage of FAVF carriers in POD and APOD shows good improvement in the symmetric property of the MLI output over the MLI outputs shown in Fig.8.Table II highlights the better performance of the proposed method for maximum m_a and the elimination of zero–crossing error with FAFF carriers in POD and APOD PWM methods.

Table III performance evaluation of 55 levels QHCMLI for $m_a = 1$

For Maximum amplitude modulation $m_a = 1$		% THD	V_{RMS}	CREST FACTOR	FORM FACTOR	DISTORTION FACTOR
FAFF using sine	PD	2.12	189.7	1.4138	3162	1.3E-4
	POD	2.10	189.8	1.4141	INF	5.8E-5
	APOD	2.22	189.3	1.4147	INF	1.1E-4
FAVF using sine	PD	2.12	189.7	1.4138	3794	1.5E-4
	POD	2.09	189.8	1.4141	INF	5.8E-5
	APOD	2.22	189.3	1.4147	INF	1.1E-4
FAFF using stepped sine	PD	1.46	189.8	1.4141	INF	2.3E-5
	POD	1.46	189.8	1.4141	INF	2.3E-5
	APOD	1.46	189.8	1.4141	INF	2.3E-5

Table III indicates the achievement of reduced THD by more than 65% with the proposed PWM strategy when compared with FAFF and FAVF carriers using sine referenced 55 levels QHCMLI. It also shows the high voltage output rms value say 189.8V for less THD value 1.46% hence satisfying the needs of applications requiring both the criteria of reduced THD and good DC bus utilisation.

VI. CONCLUSION

Table II and III shows that 55 level QHCMLI with $m_a = 1$ using the proposed switch patterns could perform satisfactorily for the applications requiring reduction of THD and good dc bus utilisation. The obtained results also show the achievement of higher number of output levels with less number of H-bridges. The increase in the number of output levels decreases the THD.

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BIOGRAPHY

K.Muthukumar was born in 1976 in cuddalore. He has obtained B.E [Electronics and Instrumentation] and M.E [process control and Instrumentation] degrees in 2003 and 2010 respectively from Annamalai University. He is currently assistant professor in the Department of Instrumentation Engineering at Annamalai University, Chidamabram, India and has put in 8 years of service. His research interests include Renewable sources, Power electronics converters and its control techniques.

T.S.Anandhi was born in 1974 in chidambaram. She has obtained B.E [Electronics and Instrumentation] and M.E [process control and Instrumentation] degrees in 1996 and 1998 respectively and then Ph.D in power electronics in 2008 from Annamalai University. She is currently Associate professor in the Department of Instrumentation Engineering at Annamalai University, chidamabram, India and has put in 15 years of service. She has produced one Ph.D and guiding 6 Ph.D scholars. Her research interests are in power converters, control techniques for multiple connected power converters, embedded controllers for power converters, renewable energy based power converters. She is a life member of Indian society for technical education.

S.P.Natarajan was born in 1955 in chidambaram. He has obtained B.E [Electrical and Electronics] and M.E [Power Systems] degrees in 1978 and 1984 respectively from Annamalai University securing distinction and then Ph.D in Power Electronics from Anna University, Chennai in 2003. He is currently Professor and Head of Instrumentation Engineering Department at Annamalai University where he has put in 33 years of service. He produced eight Ph.Ds and presently guiding eight Ph.D Scholars and so far guided eighty M.E students. His research papers 75 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 20 publications in national journals and 55 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of permanent magnet brushless DC motor, embedded control for multilevel inverters and matrix converters etc.