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A Comparative Study Of Ballistic SOI DG NMOS For .8nm Gate-Length With Mixed Gate-Oxide Over Single Gate-Oxide By DC And RF Analysis

Mukesh Kumar Suman, Sandeep Kumar, Brinda Bhowmick

Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, India

Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, India

Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, India

ABSTRACT— Over the last decade Multi Gate SOI MOSFET devices have seen a lot of potential improvements. As per the ITRS predictions, the 10nm node technology must be adopted in these devices within the year 2021 for satisfying the increasing needs of high performance logic, low operating power as well as standby power. In this paper, we report 3 different arrangements of Gate oxide for ultrathin SOI MOSFET along with their influence on electrical as well as capacitive behavior in low frequency range. Furthermore, we also analyzed the RF behavior of this device under consideration by successful variation in the scattering parameters. For, this purpose two-dimensional self-consistent Schrodinger–Poisson solver with Neumann boundary condition is used to capture the quantum mechanical nature of carrier transport along with a non-equilibrium Green's function (NEGF) approach. We also investigated the effect of different gate oxide arrangements on f_T, f_{max}, current gain, maximum available gain, maximum stable gain, stern stability factor.

KEYWORDS— f_T, f_{max}, Green's function, Schrodinger-Poisson solver, Silicon-on-Insulator(SOI) Double-Gate(DG) MOSFET, RF, S-Parameter, Technology Computer-Aided Design (TCAD).

I. INTRODUCTION

Over the past 40 years, the growth of the semiconductor industry has been governed by the continuous performance improvement of MOSFETs via aggressive device scaling. It has been widely acknowledged that the scaling capability of the silicon-on-insulator (SOI)-based classical or non-classical MOS technology is more superior to that of the conventional bulk technology which led to the introduction of several SOI structures such as the partially depleted SOI (PDSOI [1]–[3]) fully depleted SOI (FDSOI [4]–[6]), double-gate SOI (DGSOI [7], [8]), multiple-gate MOSFETs (MuGFET or FinFET [9]–[13]) etc.

In this paper, we tried to perform quantum level simulation using Technology Computer aided design (TCAD). In an attempt to accomplish a 17% annual reduction of the high-performance transistor's intrinsic switching delay (CV/I), the International Technology Roadmap of Semiconductors (ITRS) [14] imposes aggressive scaling trends for the gate length and equivalent gate oxide thickness (EOT).The need to limit the tunneling gate leakage current is pushing us towards the introduction of new gate dielectrics with high relative permittivity (high-*k*) [15], allowing thicker physical thickness for given EOT. The introduction of high-k dielectrics turned out to be a quite difficult task as they introduce parasitic effects that degrade the transistor's performance because large physical thickness leads to enhanced fringing fields that degrade short-channel effects [16] and high permittivity materials introduce additional polar phonons thus degrading the effective mobility in the channel through remote polar-phonon scattering [17].

In this paper, we investigate the DC characteristic of Double-Gate MOSFET with different materials as gate oxide viz. SiO_2, Sapphire and a mix combination of SiO_2 and Sapphire. As reported by Pedram Razavi *et al.* [18] that mixed oxide improve the SCE (Short Channel Effect). Moreover, the RF behavior of the Double-Gate MOSFET has been analyzed thoroughly through extraction of the high frequency (HF) parameters of the ultrathin Double-Gate MOSFET with Gate length of 9.8nm. We also portray capacitive behavior of this device at low frequency using a non-equilibrium Green's function (NEGF) method.

The device structure is presented in Section II, followed by results along with related discussions in Section III which include DC and High frequency RF characteristics of this device .Finally, a conclusion is drawn in Section IV.

II. Device Structure

The device under consideration consist a 5nm thick SiO_2 layer above which another SiO_2 layer having thickness 3nm is present. It is then followed by a 4nm undoped Si film, above which another 3nm SiO_2 layer and a 5nm SiO_2 passivation layer is grown. The schematic of device under consideration is portrayed in Fig.1a. A 2nm separation between Drain-Gate and Source-Drain is kept intentionally to avoid unwanted tunneling of electrons to Gate from drain and source sides.

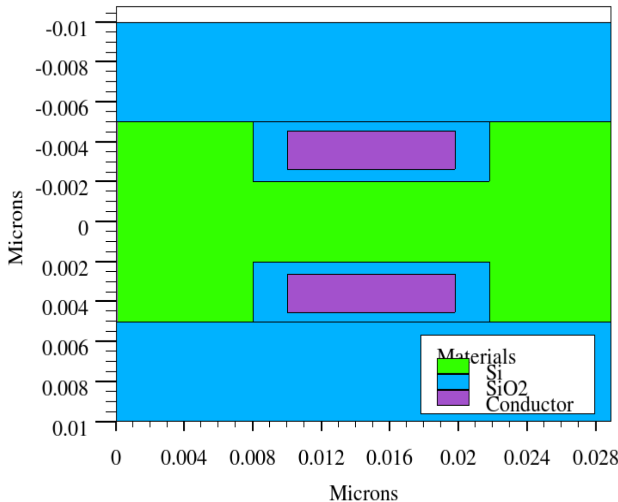

Fig. 1a Schematic view of the SOI DG nMOS for L_g=9.8nm

First of all we used SiO_2 as Gate-oxide having thickness 0.59nm. Then we replace SiO_2 with Sapphire with EOT 0.59nm. At the Last, we use a combination of SiO_2 and Sapphire in the form of Gate oxide. The schematic view of device structure of mix combination of SiO_2 and Sapphire (k=12) as gate-Oxide shown in Fig. 1b.

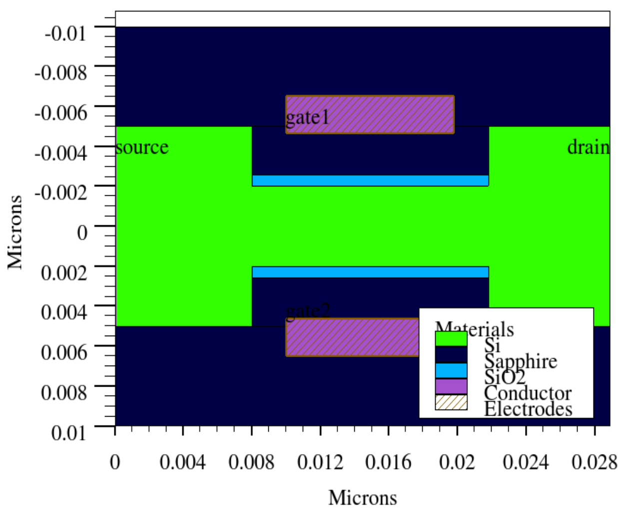

Fig. 1b Schematic view of the SOI DG nMOS for L_g=9.8nm with mix combination of SiO_2 and Sapphire as a Gate-Oxide

III. Experimental Results and Discussion

A. DC Characteristics

In Fig.2 we extracted the threshold voltage for SiO_2 (EOT=0.59nm), Sapphire (EOT=0.59nm) and combination of SiO_2 and Sapphire which is followed by capacitive analysis for the three mentioned combinations in Fig. 3.

According to ITRS for Gate length 9.8nm EOT is 0.59nm. When we used SiO_2 as Gate-Oxide the device shows a very high Gate leakage of 0.48mA/µm but when we replaced SiO_2 with Sapphire then leakage current improved to 13nA/µm. From, Fig. 3 it can be also seen that the total Gate capacitance increased from 0.925×10^{-15}F/µm in former case to1.3×10^{-15}F/µm in later case resulting in a 40% increment in strong inversion. When we tried a proper combination of SiO_2 with Sapphire so that in strong inversion the total Gate capacitance approach the capacitance due to SiO_2 with EOT 0.59nm. Hence Gate leakage current as well as total Gate capacitance both showed improvement.

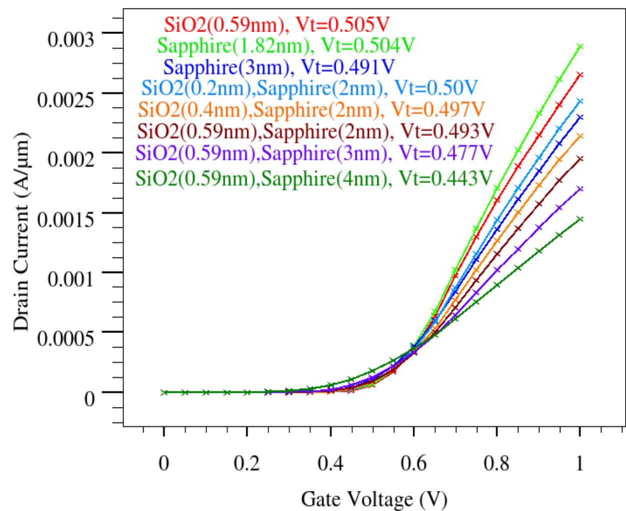

Fig. 2 I_d – Vgs curve atV_{ds}=0.1V, and L_g=9.8nm for 0.59nm SiO_2, 1.82nm Sapphire(EOT=0.56nm) and SiO_2(0.59nm)-Sapphire(2nm)

Here we used SiO_2 with thickness 0.59nm and another layer of Sapphire with thickness slightly greater than the EOT of SiO_2. For this arrangement, we registered Gate-leakage current of 0.5nA/µm and total Gate capacitance also of 0.5F/ µm in strong inversion as shown in Fig. 3. Hence, Gate-leakage current improved by 96.15% with respect to single dielectric Sapphire. Also improved threshold voltage as shown in Fig. 2.

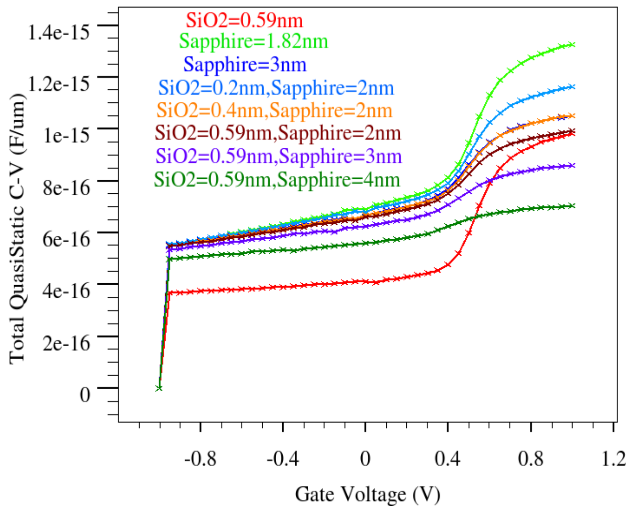

Fig. 3 Total Gate capacitance at L_g=9.8nm for 0.59nm SiO_2, 1.82nm Sapphire(EOT=0.59nm) and SiO_2(0.59nm)-Sapphire(2nm)

For this combination of Gate oxide we also achieved low transverse and longitudinal electric fields as can be seen in Fig. 4 and Fig. 5 leading to low surface scattering and DIBL which led to improvement of mobility.

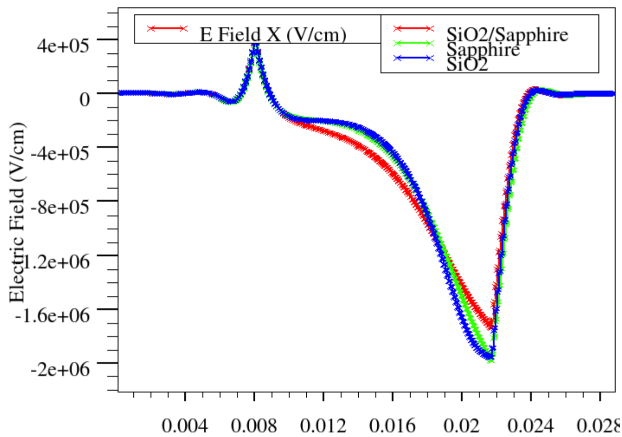

Fig. 4 Longitudinal E-Field at V_{gs}=0.7V and V_{ds}=1V, for L_g=9.8nm

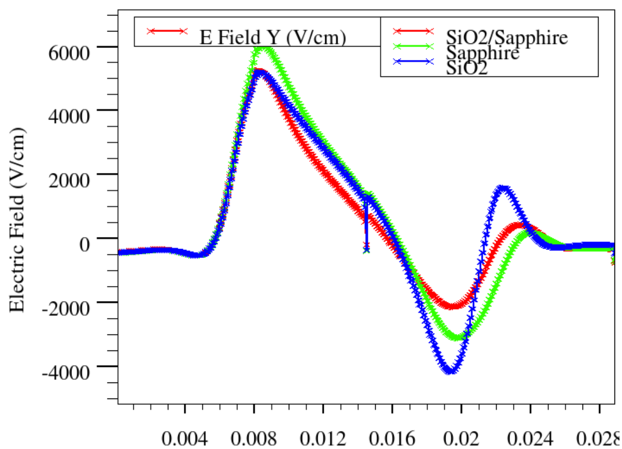

Fig. 5 Transvers E-Field at V_{gs}=0.7V and V_{ds}=1V, for L_g=9.8nm

We also registered improvement in conduction band and valence band profile as depicted in Fig. 6 resulting in an easy passage for electrons can easily flow from Source to Drain.

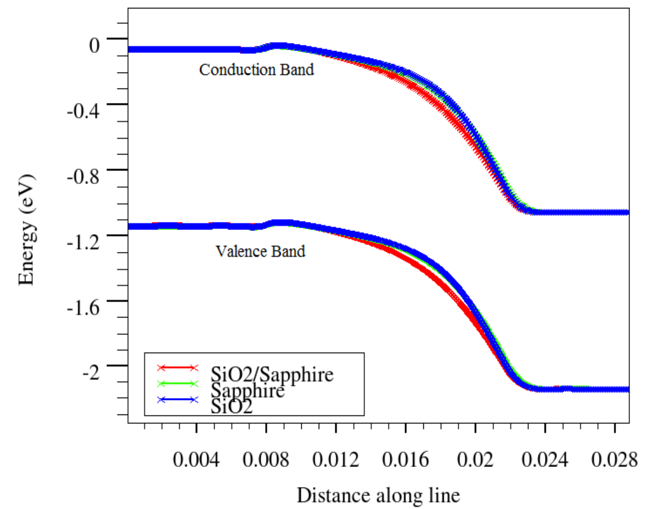

Fig. 6 Energy Band at V_{gs}=0.7V and V_{ds}=1V, for L_g=9.8nm

Intrinsic time delay for NMOS [14] devices, given by

$$\tau = (C_{g.total} \times V_{dd}) / I_{d.sat}$$

(1)

Where $C_{g\ total}$, V_{dd}, and $I_{d.sat}$ are the total Gate capacitance per micron device width in inversion (this is the sum of $C_{g.ideal}$ and the Gate fringing capacitance), nominal power supply voltage, and saturation drive current (i.e. NMOSFET Drain current per micron device width). For the above three arrangements extracted intrinsic time delay is 0.255ps (SiO_2), 0 .336ps (Sapphire) and 0.331ps (SiO_2& Sapphire) respectively.

The delay produced by SiO_2 is less but it can't be used for mass production because of high Gate leakage. Hence, it is better to use mixed Gate-Oxide keeping intrinsic time delay point in mind.

The dynamic power of NMOS [14] devices, given by

$$P_{dynamic} = CV^2 = C_{g.total} \times V_{dd}^2 \qquad (2)$$

Where $C_{g\ total}$ and V_{dd} are the total Gate capacitance per micron device width in inversion (this is the sum of $C_{g.ideal}$ and the Gate fringing capacitance) and nominal power supply voltage. The extracted dynamic power for three arrangements is 0.42875fJ/μm (SiO_2), 0.588fJ/μm (Sapphire), and 0.441fJ/μm 331ps (SiO_2& Sapphire) respectively. Hence, from dynamic power points of view also it is better to used mixed combination of Gate dielectric.

Both the calculations of intrinsic time delay and dynamic power were carried at V_{dd} equal to 0.7V.

One more and important advantage to used mixed Gate-Oxide is that we can achieve smooth interface between Si and SiO_2 rather than the high-k dielectric materials.

B. RF Characterization

In this section, we focus on the RF performances of device. For RF measurement, S-parameter characterisations were performed up to 100THz. The two important RF parameters i.e. cut-off frequency f_T and the maximum frequency of oscillation f_{max} are two important were carefully analyzed for finding the high frequency performance potential of the device.

The cutoff frequency f_T [19] is the frequency when the current gain is unity, whereas f_{max} is the frequency when the power gain/MAG/MSG is unity. The approximate values of f_T and f_{max} are shown in the following equations:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{g_m}{2\pi C_{gg}} \quad (3)$$

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s+R_i+R_g)(g_{ds}+g_m\frac{C_{gd}}{C_{gs}})}} \quad (4)$$

Where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances, respectively. g_m and g_{ds} are the transconductance and the output conductance, respectively; C_{gg} is the total gate capacitance; and R_g, R_s, and R_i are the gate, source, and channel resistances. Thus, it is obvious that both figures-of-merit are greatly influenced by these geometrical parameters.

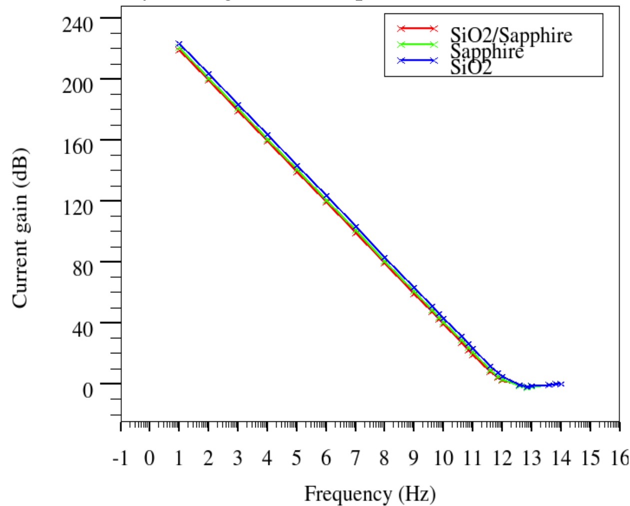

Fig. 7 The comparison of cut-off frequency (f_T) for SiO_2, Sapphire, and mix combination of SiO_2& Sapphire.Frequency on logarithmic scale

Kai Lu *et al.* [20], reported f_T and f_{max} is 94.6 and 132.8 GHz for PD SOI nMOSFET. Also Kun-Ming Chen *et l* [21] reported f_T and f_{max} of WD device are 5.3 and 18 GHz. From Fig. 7 we extracted the value of f_T is equal to 3THz for the SiO_2, and Sapphire and for mix combination of SiO_2 & Sapphire is equal to 2THz. For SiO_2 we achieved slightly greater value then Sapphire and mix combination of SiO_2 & Sapphire.

From Fig. 8 and Fig. 9 we extracted the f_{max} also which is almost same for all three arrangement of gate-Oxide and is equal to 40THz.

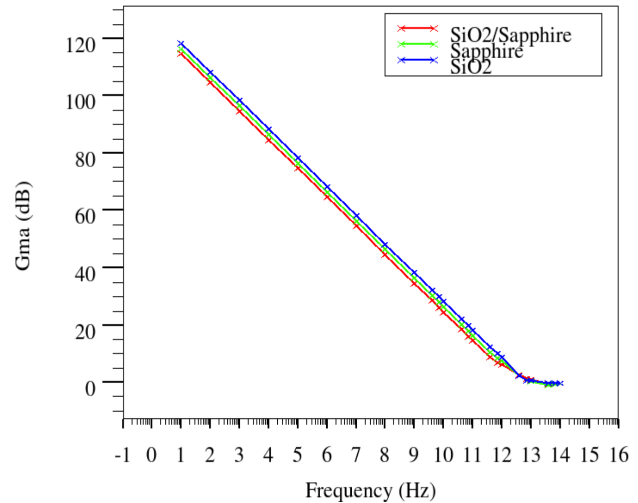

Fig. 8 The comparison of MAG for SiO_2, Sapphire, and mix combination of SiO_2& Sapphire. Frequency on logarithmic scale

For an amplifier to have considerable stability G_{ms} or maximum stable gain is considered to be an important criterion. From, Fig. 9 it can be seen that the device shows a best G_{ms} of 118 dB for dielectric as SiO2 followed by Sapphire as dielectric alone and lastly by the combination of Sapphire/SiO2.

The variation in scattering parameters for the device under consideration is shown in Fig 10 and 11 respectively.

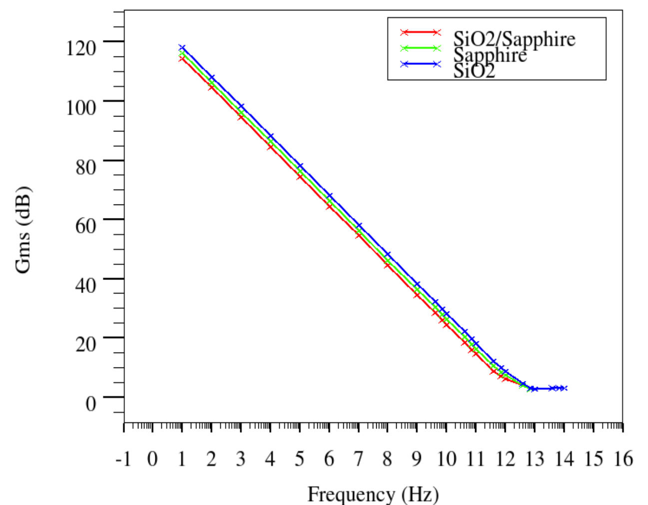

Fig. 9 The comparison of MSG for SiO_2, Sapphire, and mix combination of SiO_2 & Sapphire. Frequency on logarithmic scale

From the smith chart in Fig. 10 It is that the input reflection coefficient S11 =1 at 1Hz. It represents the maximum reflection of signal at the input port and the device behaves as open circuit. As frequency increases towards 100 THz, the S11 follows the constant R circle with decreasing value of capacitance as shown in the Smith chart, in a clockwise direction and approaches closer to the matching point (i.e. centre of the bigger circle), where no reflections occur due to proper impedance matching. In higher frequency range for S_{11} red curve correspond to SiO_2 is more closer towards to the perfect matching point, but it can not be used due to high leakage current. Then followed by the blue curve

correspond to mix combination of oxide and green curve correspond Sapphire. In similar way S_{22} is also has better for mix combination of oxide.

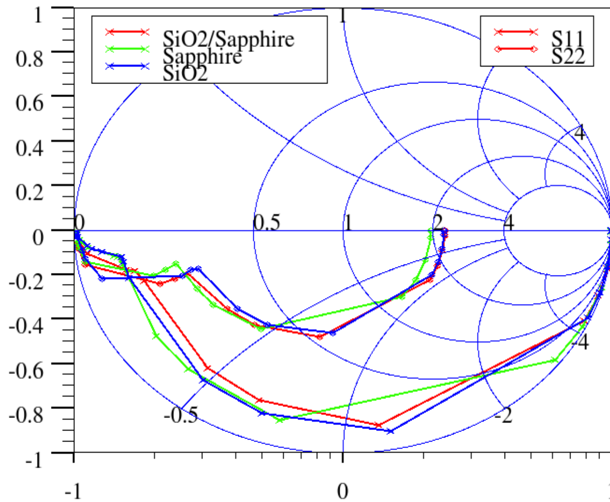

Fig. 10 Smith chart for S11 and S22 parameter for SiO_2, Sapphire, and mix combination of SiO_2& Sapphire

The input impedance of the device is found to be of capacitive in nature because S_{11} lies in the lower half of the smith chart as evident from Fig. 10 for all the three combinations of Gate dielectrics.

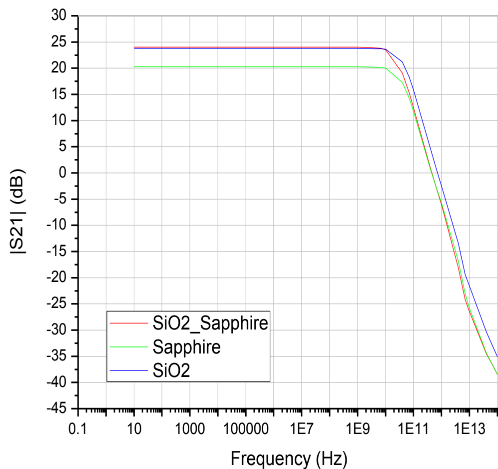

Fig. 11. Magnitude plot for S21 parameter for SiO_2, Sapphire, and mix combination of SiO_2& Sapphire

From Fig. 11 forward voltage gain is maximum for mix combination of oxide as well as SiO_2 and minimum for Sapphire (EOT=0.59nm). For mix combination of oxide gives forward voltage gain more than one up to 0.8THz whereas SiO_2 and Sapphire up to 0.5THz.

Reverse voltage gain was found to be very less and is almost the same for all the five combination (Fig. 12).

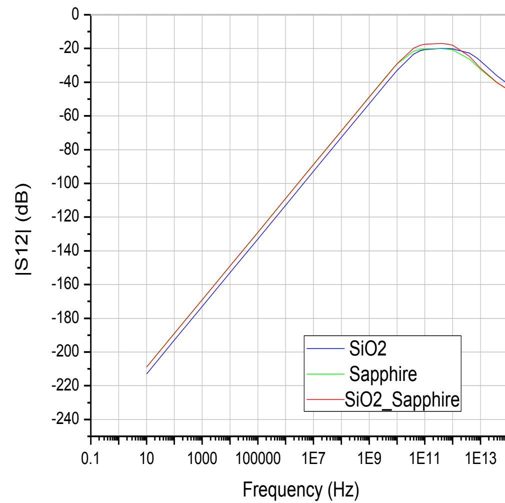

Fig. 12 Magnitude plot of S12 with respect to frequency for different arrangement of Gate oxide

Finally, from Fig. 13 we can see the variation of Stern stability factor (k) for different combinations of Gate dielectrics for the device under consideration. It shows that for all the different combinations of Gate dielectric the device behaves as an oscillator up to a frequency range of 4 THz (k<1) and then it starts behaving as a RF amplifier with suitable stability (K>1). It can be also be seen from the Fig. 13 that the best RF behavior is shown by Sapphire as Gate dielectric followed by the combination of SiO_2/Sapphire and finally SiO_2 alone.

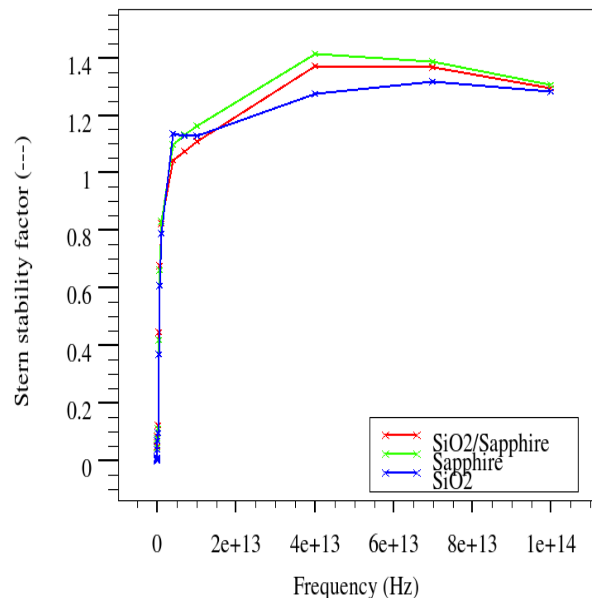

Fig. 13 Stern stability factor for SiO_2, Sapphire, and mix combination of SiO_2&Sapphire

IV. CONCLUSIONS

We performed rigorous experiments and analyzed that mix combination of Gate-Oxide gives better result than the single Gate-Oxide either high-k material or SiO_2. We also got very high cut-off frequency as well as frequency of oscillation for such a ultrathin SOI DG MOSFET.

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