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# A High Power Factor DC Drive for Universal Input Voltage Applications

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**ABSTRACT:** This paper proposes a high power factor DC drive for the speed control of DC motor. In electric power system, load with low power factor draws more current which leads to energy wastage and higher electricity charges. A new configuration of SEPIC converter is used in this paper to improve power factor. Low switch voltage and high static gain of the converter is achieved by employing voltage multiplier method. Simple regenerative snubber is used in order to reduce losses associated with diode reverse recovery current and to achieve ZCS. Operational analysis, design procedure and simulation results for a 5HP, 500V, 1720 RPM DC motor is presented. The system show enhanced dynamic response to sudden change in speed reference, input voltage and load fluctuations.

KEYWORDS: SEPIC converter, DC motor, voltage multiplier, ZCS

### I. INTRODUCTION

In ac-dc conversion system, the current drawn from the ac side has huge amount of third harmonics, so the power quality problems introduced on the ac grid is severe. Many methods are adopted to solve the low power factor and high THD. In power system, load with low power factor draws more current, so energy is wasted. Because of wasted energy, electrical utilities will charge a higher cost to customers with low power factor. The most common method used is boost type power factor correction. But there are many disadvantages such as it is not applicable for universal input voltage applications and it has low efficiency, which affect the thermal design of heat sink. Also its static gain is not enough and has high switching losses. In boost converter, voltage multiplier technique [1] is used to increase the static gain with low switching losses. A modified high power factor SEPIC [2] is used to obtain high static gain at low voltage. Due to the operation with high input current and high output voltage, the step up stage is a critical point for design of high efficiency converter [3]. Some single phase high power factor rectifiers are presented in [4-5]. High static gain and low switch voltage topology, to improve the efficiency are given in [6-7].

DC-DC converters are widely used in DC motor drive applications. The input to the converter is DC voltage obtained by rectifying the grid voltage, but for its application high step up static gain and high efficiency is required. SEPIC Converter is a DC-DC converter, which is suitable for both step up and step down operation. Its input current is not pulsating and has same polarity for both buck and boost operation. Fig. 1 shows a conventional SEPIC Converter.

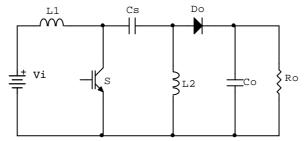


Fig. 1 Conventional SEPIC converter

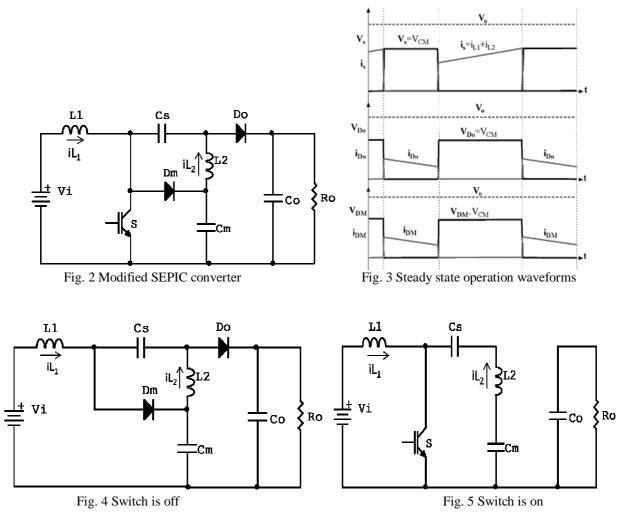


(An ISO 3297: 2007 Certified Organization)

Vol. 3, Special Issue 5, December 2014

#### **II. MODES OF OPERATION AND WAVEFORMS**

The selected converter is Modified SEPIC Converter [2] which has many advantages than that of conventional SEPIC such as low switching voltages and high static gain. In conventional converter, the switching voltage is the sum of input and output voltage, so it has high switch voltage and low static gain and is not applicable for universal voltage applications. For avoiding these problems, diode  $D_M$  and capacitor  $C_M$  is used. Fig. 2 shows the modified SEPIC Converter. Due to the charging of the capacitor  $C_M$  to the output voltage, the voltage across the inductor will be very high and so increasing the static gain.



Mode 1: Switch is off

The energy stored in the inductor during the turn on is transferred to the output. The switching voltage during this period is low and is equal to the capacitor voltage. In this case both diodes are forward biased and current through it decreases due to the charging of capacitor.

### Mode 2: Switch is on

During this period both inductors store energy. Inductor  $L_1$  stores energy from input voltage and inductor  $L_2$  stores energy from  $V_{CS}-V_{CM}$  ( $V_{CM} > V_{CS}$ ). The diode  $D_0$  is reverse biased as  $V_0 > V_{CS}$  and diode  $D_M$  is reverse biased due to the voltage  $V_{CM}$ .

The modified SEPIC converter has lowest duty cycle values in all range of input voltage than conventional converter. Lower duty cycle results in lower switch conduction interval. As the t<sub>on</sub> period is low, a lower current ripple



(An ISO 3297: 2007 Certified Organization)

### Vol. 3, Special Issue 5, December 2014

is obtained in the input inductor  $L_1$ . The switch voltage is lower than output voltage in all input voltage range, which will increase the converter efficiency and reduce the cost

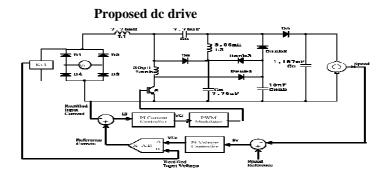


Fig. 6 Implemented DC drive

Fig.6 shows the proposed DC drive along with the ratings of the components used. The speed of the DC motor is measured and is used for controlling the switch. L<sub>snb</sub> is used to limit the di/dt and to provide ZCS and it will also eliminate turn on commutational losses. C<sub>snb</sub> is used to eliminate the dv/dt of power switch voltage. Speed of the DC motor is compared with the reference speed. The error is applied to the PI controller. The result obtained is multiplied with the input voltage and the resultant obtained is reference waveform for current control loop. The reference current is made in phase with the input voltage by multiplying the unit input voltage waveform with the output of PI controller. Then it is compared with the rectified input current, so that the actual current follows the reference current. Hence power factor will be improved. The output obtained is applied to PWM, which generate control signal to power switch.

#### **III. ANALYSIS AND DESIGN**

The design of the 5 HP (3728.5W), 500V, 1720 RPM DC motor is presented in this section. The input voltage is varied between  $V_i = 100-240V$ .

Output current = 
$$\frac{\text{Output power}}{\text{Output voltage}} = \frac{3728.5}{500} = 7.457\text{A}$$

The input current is different for different input voltage and is maximum for minimum value of input voltage. So maximum value of input current can be calculated.

Α. Static Gain

It is defined as the ratio of output voltage to input voltage, which is the ability of the circuit to increase the power from the input to output. It can be obtained by considering the average value of inductor voltage as zero. Fig 7 shows the voltage across the inductor  $L_1$  and  $L_2$ 

From Fig. /  

$$V_i t_{ON} = (V_{CM} - V_i) t_{OFF}$$

$$V_i D = (V_{CM} - V_i) (1 - D)$$

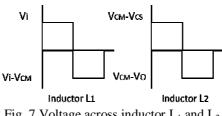


Fig. 7 Voltage across inductor  $L_1$  and  $L_2$ 

By rearranging,



(An ISO 3297: 2007 Certified Organization)

### Vol. 3, Special Issue 5, December 2014

$$\frac{V_{CM}}{V_i} = \frac{1}{1 - D}$$

When power switch is on  $D_O$  and  $D_{CM}$  are in conduction stage, output voltage is the sum of voltage across capacitor  $C_S$  and  $C_M$ 

$$V_{O} = V_{CS} + V_{CM}$$
  
From Fig.7  
 $(V_{CM} - V_{CS})t_{ON} = (V_{O} - V_{CM})t_{OFF}$   
 $(V_{CM} - V_{CS})D = (V_{O} - V_{CM})(1 - D)$   
 $V_{CS} = V_{O} - V_{CM}$   
 $\frac{V_{O}}{V_{i}} = \frac{1 + D}{1 - D}$   
 $\frac{V_{O}}{V_{i}} = \frac{1 + D}{1 - D} = \frac{500}{100} = 5$ 

Maximum Input current = (output current)  $\times \left(\frac{1+D}{1-D}\right) = 7.457 \times 5 = 37.285A$ 

For Analysis select duty ratio as .5 D = .5

$$\frac{V_o}{V_i} = \frac{1+D}{1-D} = 3$$
$$V_i = \frac{V_o}{3} = \frac{500}{3} = 166.67$$

Input current = (output current)  $\times \left(\frac{1+D}{1-D}\right) = 7.457 \times 3 = 22.37A$ 

V

### B. $L_1$ and $L_2$ Inductors

The value of input impedance is obtained as a function of maximum input current ripple. The current ripple is assumed as 1% of the input current. The input voltage is 166.67 and duty cycle is equal to .5 with supply frequency 50 Hz and switching frequency 48 kHz.

$$\Delta I_L = i_{inpeak} \times \frac{1}{100} = 22.37 \times .01 = .2237A$$
$$L_1 = \frac{V_i \times D}{\Delta I_L \times f} = \frac{166.67 \times .5}{.2237 \times 48000} = 7.761H$$

The volume of the inductor  $L_2$  is less than that of inductor  $L_1$  as the average input current is higher than average output current and is assumed as its half of  $L_1$ .

$$L_2 = \frac{L_1}{2} = \frac{7.761}{2} = 3.88mH$$

#### C. Series capacitor $C_S$ and multiple capacitor $C_M$

During turn on period, the current in the series capacitor  $C_S$  and the multiple capacitor  $C_M$  is same as the inductor current  $L_2$ . The capacitor charge variation

$$\Delta Q = i_{L2}DT$$
$$\Delta V_c = \frac{\Delta Q}{C} = \frac{i_{L2} \times D \times T}{C}$$

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### Vol. 3, Special Issue 5, December 2014

$$C_s = C_m = \frac{i_{L2} \times D}{\Delta V_c \times f}$$

The capacitors are designed for a ripple of 2% of output voltage

$$C_{s} = C_{m} = \frac{i_{L2} \times D}{\Delta V_{c} \times f} = \frac{7.457 \times .5}{10 \times 48000} = 7.76 \,\mu F$$

#### D. Output Capacitor

The output capacitor is a function of output power  $P_0$ , grid frequency  $F_G$ , and voltage ripple. The output capacitor is designed for a ripple of 2% of output voltage.

$$C = \frac{P_0}{2\Pi f_G 2V_o \Delta V_o} = \frac{3728.5}{2 \times 3.14 \times 50 \times 2 \times 500 \times 10} = 1.187 mF$$

#### IV. SIMULATION RESULTS

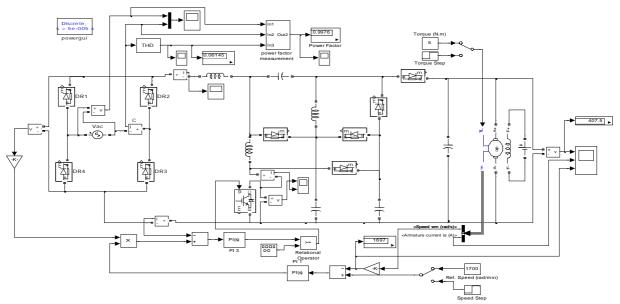


Fig. 8 Simulink model of DC drive

Fig. 8 shows the simulink model of the proposed dc drive. Power factor of the system measured by using the equation

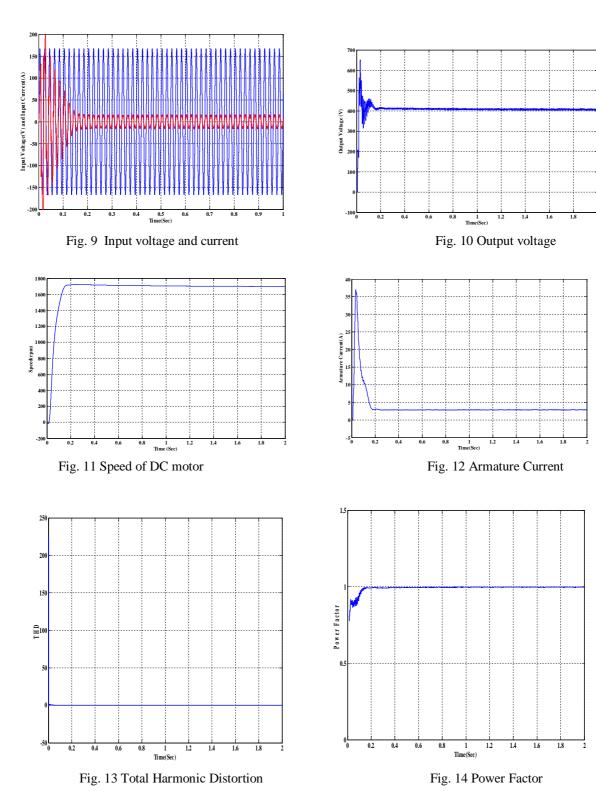
$$powerfactor = \frac{P}{\sqrt{P^2 + Q^2}\sqrt{1 + THD^2}}$$

Fig 9-14 are the output waveforms obtained during simulation. Fig. 9 shows the input voltage and current of the converter. The current is in phase with the voltage which is one of the primary aim. Fig.10, 11 and 12 shows the steady state output voltage, speed of the DC motor and armature current respectively have a fast transient response with a settling time of 0.1 sec. Fig.13 shows THD, which is obtained as .06145. Fig 14 shows the power factor which is obtained as .9976.



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Vol. 3, Special Issue 5, December 2014

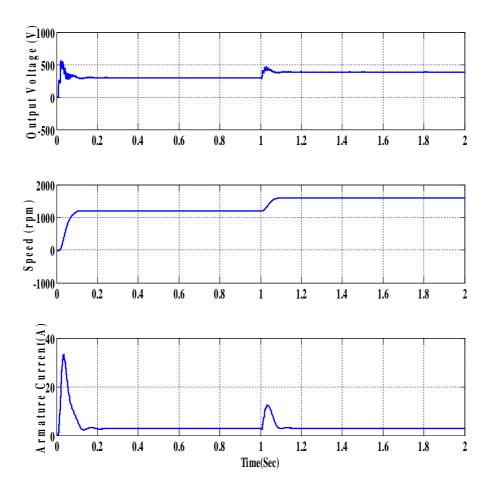


Fig. 15 Response of the system to the sudden change in speed Reference

Fig. 15 shows the response of the system to sudden change in the reference voltage. When speed changes, there will be a corresponding change in the output voltage, but the armature current remains the same. Fig. 16 shows the response of the system to load fluctuations. When there is a load fluctuation, there will be corresponding change in armature current, but the control loop keep the output voltage and the speed as same. Fig. 17 shows the response of the system to the change in input voltage. As it is used for universal input voltage applications, even if there is change in the input voltage, the output voltage, speed and armature current remains same.



(An ISO 3297: 2007 Certified Organization)

Vol. 3, Special Issue 5, December 2014

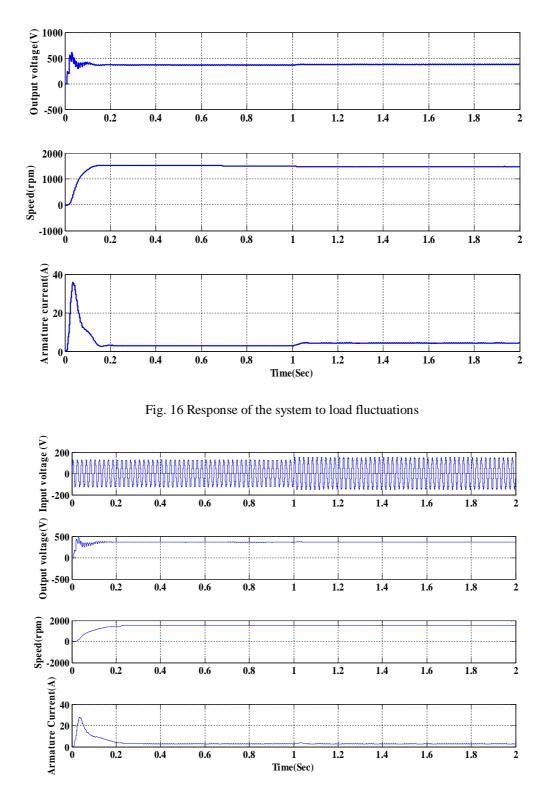


Fig. 17 Response of the system to change in input voltage



(An ISO 3297: 2007 Certified Organization)

#### Vol. 3, Special Issue 5, December 2014

#### V. CONCLUSION

Speed control of the DC motor is proposed for universal input voltage applications. The closed loop converter model is simulated on MATLAB simulink. PI controller is used for controlling the speed of the proposed converter. In spite of high circuit complexity the system provide many advantages like high power factor, low total harmonic distortion, and have low diode reverse recovery current. The simulation results of a 5 HP, 500V, 1720 rpm DC motor is evaluated and concluded that the proposed system is suitable for universal input voltage applications and sudden load fluctuations.

The main demerits of the proposed converter is that it has higher circuit complexity than the basic converter, also have high switch current stress. It also has high settling time.

Stability analysis of system can be done. The system can be modified to control the speed of AC motor by incorporating an additional inverter. It can also be used for variable input voltage application like PV and wind energy system

#### REFERENCES

[1] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. R. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar.*2008.

[2] P. F.Melo, R.Gules, E. F. R. Romaneli, and R. C.Annunziato, "A modified SEPIC converter for high-power-factor rectifier and universal input voltage applications," *IEEE Trans. Power Electron., vol. 25, no. 2, pp. 310–321*, Feb. 2010.

[3] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC- DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[4] J. Qian, F. C. Lee, "A high efficient single stage single switch high power factor ac/dc converter with universal input", IEEE Trans. Power Electron., Vol. 13, No. 4, pp. 699–705, 1998.

[5] C. Qiao, K. M. Smelley, "A topology survey of single-stage power factor corrector with a boost type input current-shaper", IEEE Trans. Power Electron., Vol. 16, No. 3, pp. 360–368, 2001.

[6] Q. Zhao, F. C. Lee, "High-efficiency, high step-up DC–DC converters", IEEE Trans. Power Electron., Vol. 18, No. 1, pp. 65–73, 2003.

[7] R.J. Wai, R.Y. Duan, "High-efficiency power conversion for low power fuel cell generation system", IEEE Trans. Power Electron., Vol. 20, No. 4, pp. 847–856, 2005.