



A Modification of Concurrent Dual Band Radio Receiver Architecture

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ABSTRACT: Channels linking information sources and receivers are one of the fundamental blocks of all communication system. The size of the dust particle present in space, those of snows and rain drops are known to affect communication due to their diffracting and scattering effects. A concurrent dual band radio receiver architecture that can operate at both 900MHz and 1800MHz is proposed. The architecture is found to be feasible with additional advantages of low power consumption, light and small chip area. This result implies that, the problem of channel condition can be reduced if this architecture is adopted at both transmission and reception points.

KEYWORDS: Concurrency, Dual Band Filter, Dual Band Amplifier, Dual Detection, Frequency Multiplier

I. INTRODUCTION

The common radio transmission and reception activities are accomplished through modulation at single carrier frequency. When the communication channel vary by the presence of dust particles, raindrops or snows the scattering and diffracting abilities of these tiny masses, cause detrimental effects to the smooth propagation of these radio carrier waves and thus spoil the communication activities.

Solution to this effect could be achieved, by increasing the signal strength of the radio signal or by changing the carrier frequency which has direct link to these effects, since they are wavelength dependent. The latter solution is more economical and technically feasible. It was suggested by Wu,S and Razavi,B, Fong, k and Ryyananen,J.

In this work, we wish to present an architecture that would provide concurrency in the dual transmission and reception of the modulated carrier above, with additional modification of the previous works on the detection section.

Most of today's wireless receivers use any of these general architectures: heterodyne, homodyne, low-IF, and image-rejection receivers such as the ones originally proposed by D. K. Weaver. Similarly, all these architectures have been employed in the multi-band receivers for various applications.

Direct conversion receiver represents a less complicated design by having a reduced number of circuit blocks, number of stages; provide a wide tuning range and high selectivity. There is however several drawbacks such as two high frequency conversion stages in parallel, local oscillator signal may cause leakage to the antenna. The reduce circuit complexity generally reduced performance; problem of image in this architecture is form when the size of noise or any interference is closed to or above the size of signal.

That problem of image with direct conversion can be overcome using superheterodyne receiver. This is the traditional radio receiver architecture for wireless communication. The solution is to place a filter before the mixer to remove the image. A very high quality band pass filter is needed, to provide the desired performance. To achieve good selectivity by down-converting the received RF signal in multiple steps. In multi-band heterodyne radio architecture, there will be higher power consumption, and a higher overall cost for the system, translation. Also at the end, the received signal information, though of high quality, is usually weak.

To solve the problem of weak signal in super heterodyne architecture,[18] suggested parallel dual detection. When the final output is added, the signal is obtained. This architecture increases the signal strength. The weaver solution is restricted to the signal already received by the radio. If the signal suffered in the channel before reaching the receiver, the weaver solution is ineffective.[17] proposed a modification in which the transmission and reception are going to be done at two different frequencies.

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The problem of power consumption of the above architecture was considered by [6], and led them to a circuit with a dual band low noise amplifier using single wide band amplifier and dual band filter for the two carrier frequencies. However this architecture needs two local oscillators for detection of F_1 and F_2 .

In this work we proposed the use of a single LO with a frequency multiplier instead of double oscillators in the Hossein. H and Hajimiri, A.

II. CONCURRENT DUAL BAND RADIO RECEIVER

In the [6], two distinct oscillators were used. In this work, we intend to use a single oscillator with a doubler circuit during detection. This may reduce the cost of the final circuit. The proposed architecture is illustrated in figure 1.

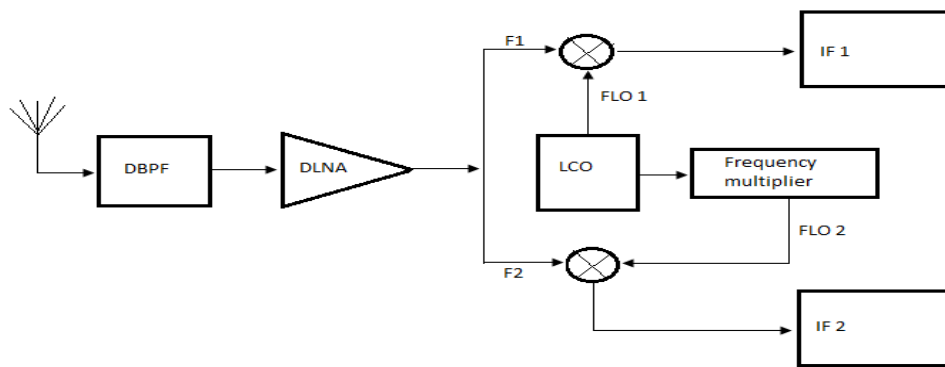


Figure 1: Block diagram of concurrent dual band receiver

The circuit block includes an antenna, which received modulated signals of the same information at different frequencies. The modulated signals passed through a dual band-band pass filter (BPF), to select the desired frequencies F_1 and F_2 and reject or block the undesired ones. These signals are then amplified by a very wideband amplifier with turning at f_1 and f_2 concurrently. The last stage is dual detection, where modulated frequency F_1 is mixed with carrier frequency F_{C1} of LO to produce intermediate frequency (IF_1). Also the signal F_1 from the LO is doubled in the multiplier, and mixed with modulated frequency F_2 to produce intermediate frequency (IF_2). The designs of these three circuits; the dual band filter, the amplifier and the frequency multiplier are presented below.

III. FILTER DESIGN

The design architecture of the filter used in this work was the one proposed by [13] and follow chebyshev configuration. It is simple and has the advantage of using identical conductor throughout the filter sections beside its excellent design flexibility and high performance.

For dual band filters, the architecture proposed by [12] and [1] modified by [11] is used in which the architecture dual band filter is achieved by inserting a narrow band top filter into a broadband filter to create the dual band characteristics. It is presented in fig 2

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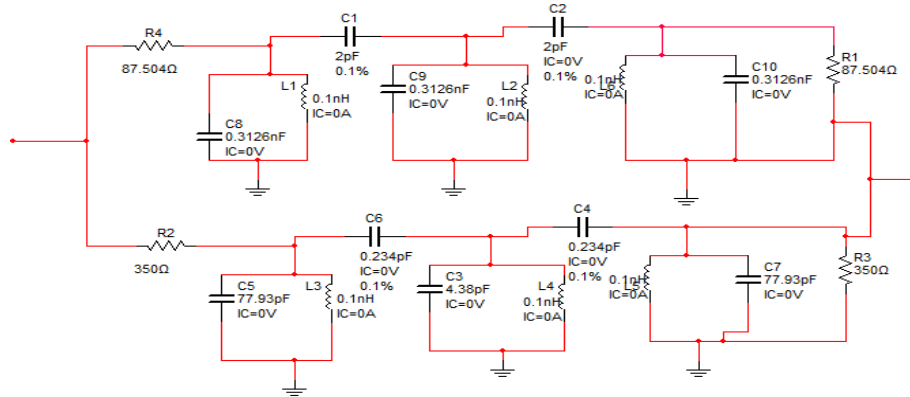


Fig. 3: Dual band filter

The figure above shows three stages of two single band filters, to select f_1 and f_2 connected in parallel, with input from the left and output at the right side of the circuit.

To design such filter, it requires Center frequency (f_0), bandwidth (BW), pass-band ripple (rp), input and output impedances (Z_i and Z_o), number of stages (ns) and the shunt inductor value (L) to be used. Using these parameters, the capacitance and Q factor values were computed.

Center Frequency, (900MHz and 1800MHz) Bandwidth (Hz) BW=25MHz (G.S.M Band) Pass band Ripple = 1 dB [16]
Inductance, L=0.1nH

$$R_s = \omega L Q_1 = 2\pi f L Q_1 \quad 1$$

where R_s is Source Impedance (Ohms), $\omega = 2\pi f$, L= inductance and Q_1 = quality factor

$$\text{Load Impedance (Ohms): } R_L = \omega L Q_1 = 2\pi f L Q_1 \quad 2$$

Based on the above specification; $Q_1 = 1.0316 = Q_3$ and $k_{12} = k_{23} = 0.9192$ [16]

$$Q_{bp} = \frac{f_0}{BW} \quad 3$$

$$C_{node} = \frac{1}{\omega^2 L} \quad 4$$

$$C_{12} = C_{node} k_{12} \quad 5$$

$$\text{Similarly, } C_{23} = C_{12} \quad 6$$

$$C_1 = C_{node} - C_{12} \quad 7$$

$$C_2 = C_{node} - C_{12} - C_{23} \quad 8$$

$$C_3 = C_{node} - C_{23} \quad 9$$

Where C_1 , C_2 and C_3 are the resonance capacitors at center frequency

C_{12} and C_{23} are coupling capacitors

C_{node} is the nodal capacitor

IV. DUAL BAND FILTER DESIGN

Recent researches on the design of dual-band BPFs have been presented [1]. One of simplest methods to design the dual-band BPF is by connecting two different pass band BPFs in parallel to obtain the dual-band characteristics. Another approach is to insert a narrowband band stop filter into the broadband BPF to create the dual-band characteristics. [11]. Because two different filters are used, the sizes of these dual-band BPF are comparatively large.

$$C_3 = C_s + C_p \quad 10 [16]$$

Where

$$C_p = \frac{CS(Z-RP)}{RP} \quad 11$$

$$C_s = \frac{1}{(\omega^2 Z(R_p - Z))} \quad 12$$

The output and input impedance to be connected in series is given with

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$R_p=211.6\Omega$ Impedance $Z=50\Omega$

Therefore single band BPF of f_1 & f_2 designed above can form a dual band BPF with two signals by connecting the two single bands in parallel. The fig. 3 above shows the circuit diagram of dual band BPF.

V. DUAL BAND AMPLIFIER

In conventional dual-band amplifier, either one of the two single-band amplifier is selected [14][5], or two single-band amplifier are designed to work in parallel using two separate resonant loads, resulting in a high implementation cost due to the large chip area [17]. The former approach is non-concurrent, while the latter consumes twice as much power. In a wideband LNA, strong unwanted blockers are amplified together with the desired frequency bands and significantly degrade the receiver sensitivity. In this work, concurrent multiband amplifier was proposed as an alternative to alleviate these problems, using bipolar junction transistor (BJT) for wide band operation.

Dual band amplifier is achieved by using a wave band amplifier and tuning within its pass band, the two desired frequencies F_1 and F_2 .

VI. AMPLIFIER DESIGN

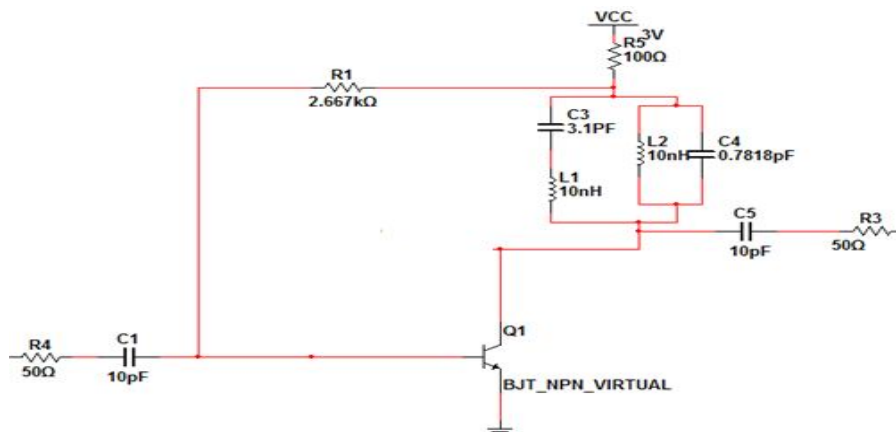


Figure 4: wide band amplifier

The figure above shows main function of concurrency. An amplifier built around transistor, NPN RF Input Power of SiGe:C Bipolar Transistor BFR740L3RH, with Common source configuration. Contains input and output impedances, series resonance circuit and parallel resonance at the output, which turn to amplify f_1 and f_2 at the output

The circuit design starts with data sheet. [10] silicon configurations were used

$$I_{cq}=15 \text{ mA } V_{cc}= 3\text{V } V_{be}=0.7\text{V}$$

$$V_{R5} = \frac{1}{2} \text{ of } V_{CC} \quad 13$$

$$R_5 = \frac{V_{R5}}{I_{CQ}} \quad 14$$

$$V_C = V_{be} + V_{R1} \quad 15$$

$$I_b = \frac{I_C}{\beta} \quad 16$$

Where $I_b = 2\%$ of I_C [15]

$$R_e = \frac{25\text{mv}}{I_E} \text{ or } \frac{50\text{mv}}{I_E} = R_{in} \text{ (constant)}$$

$$X_{C1} \ll R_{in} \text{ and } I_E = I_C \quad 17$$

The capacitor is chosen with reference to the lower frequency f_1 with impedance so that any frequency above f_1 with lower impedance will be amplified.

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VII. SERIES RESONANCE CIRCUIT

To excite a crystal for operation in series resonant mode, it may be connected as a series element in feedback path. At the series resonant frequency of the crystal, its impedance is smallest and the amount of positive feedback is largest.

At series resonant frequency f_1 , inductor $L_1=10\text{nH}$ (assumed)

$$C_1 = \frac{1}{4\pi^2 f_1^2 L_1} \quad 18$$

VIII. PARALLEL RESONANCE CIRCUIT

Since the parallel resonant impedance of a crystal is a maximum in shunt. At the parallel resonance operating frequency, a crystal appears as an inductive reactance of largest value.

At parallel resonant frequency f_2 , inductor $L_1=10\text{nH}$

$$C_2 = \frac{1}{4\pi^2 f_2^2 L_1} \quad 19$$

The output impedance must be far greater than the input impedance of the next stage, assume $Z=50\Omega$

$$C_3 = \frac{Z}{2\pi f_1} \quad 20$$

IX. AMPLIFIER DESIGN ANALYSIS

This aspect expressed the general amplifier analysis to transfer function of an amplifier gain. The equivalent model of the circuit is given in the figure below;

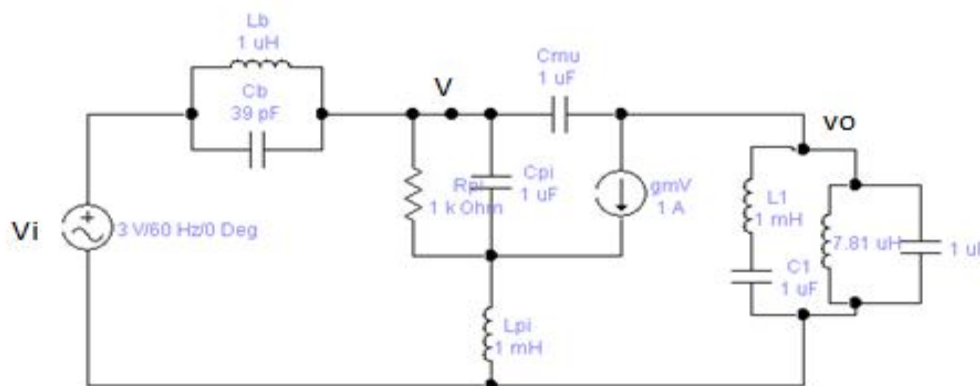


Figure 5;Equivalent circuit (hybrid π modal)

The figure above indicates the equivalent circuit of figure 4 using hybrid π model. This figure used to determine the the transfer function of an amplifier by using nodal analysis.

$$\frac{V^I - V_i}{z_b} + \frac{V^I}{z_\pi + X_{L\pi}} + \frac{V^I - V_o}{X_{C_\mu}} = 0 \quad 21$$

$$\frac{V_o - V^I}{X_{C_\mu}} + gmV + \frac{V_o}{Z_{LC}} = 0 \quad 22$$

The input loop can be expressed as;

$$V_i = iZ_b + iZ_\pi + (1 + \beta)iX_{L\pi} \quad 23$$

Where

V_i is the input voltage, V_o is the output voltage, V^I is the nodal point, Z_b is the input impedance resonating at f_1 , Z_π is the impedance at r_π and C_π ,

Z_{LC} is the output resistance resonating at both series (f_1) and parallel resonator (f_2)

gm is the transconductance of the transistor (see data sheet), L_b is the base inductor,

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C_b is the base capacitor; C_μ is the capacitor operating at high frequency, L_π is the tuning inductor, X_{lb}, X_{cb} and X_π are the impedance at l_b, c_b and C_π respectively. L_1 and C_1 is inductor and capacitor in series resonator. L_2 and C_2 are inductor and capacitor in parallel resonator

The transfer function of the amplifier is given by the following expression,

$$A_v = \frac{Z_{LC} X_\mu Z_b}{(z_b + Z_\pi + (1+\beta)X_{L_\pi})} \frac{gm Z_\pi (Z_b X_\mu + (X_\mu + Z_b)(Z_\pi + X_{L_\pi}) - (Z_\pi + X_{L_\pi})(z_b + z_\pi + (1+\beta)X_{L_\pi}))}{[Z_{LC} Z_b (Z_\pi + X_{L_\pi}) - X_\mu (Z_b X_\mu + (Z_\pi + X_{L_\pi})(Z_b + X_\mu))]} \quad 24$$

By simplification and substituting all component values, the transfer function expressed in the polynomial form given as;

$$A_v = \frac{-1.02e-127s^{13} + 7.5e-117s^{12} - 1.12e105s^{11} + 2.56e94s^{10} + 1.04e83s^9 + 2.75e-72s^8 + 2.35e-63s^7 + 5.26e-52s^6 + 1.5e-43s^5 + 2.56e-32s^4 + 2.7e-24s^3 + 3.7s^2}{2.14e-142s^{14} + 7.93e-132s^{13} + 9.7e-118s^{12} - 1.08e-104s^{11} - 7.01e-78s^{10} - 6.10e-84s^9 - 1.51e-57s^8 - 8.79e-48s^7 - 4.24e-38s^6 - 2.43e-44s^5 - 1.06e-35s^4 - 6.84e-25s^3 - 3.89e-15s^2 - 1.65e-15s} \quad \dots\dots\dots 25$$

X. DUAL DETECTION

In this case a single oscillator is used to generate 900MHz of carrier signal. An interesting effect that results from choice of the single LO Frequencies is in-band leakage to the antenna. That is, if $f_{LO1} = 900\text{MHz}$ is mixed with $f_{LO2} = 1800\text{MHz}$, both 900MHz and 1.8GHz components are generated at the receiver output, f_{LO2} is generated using frequency multiplier circuit. At the output of the multiplier a single stage filter is designed, to filter 1800MHz. This will help to further smooth the doubling output. . Fig. 6 below show the frequency doubling circuit

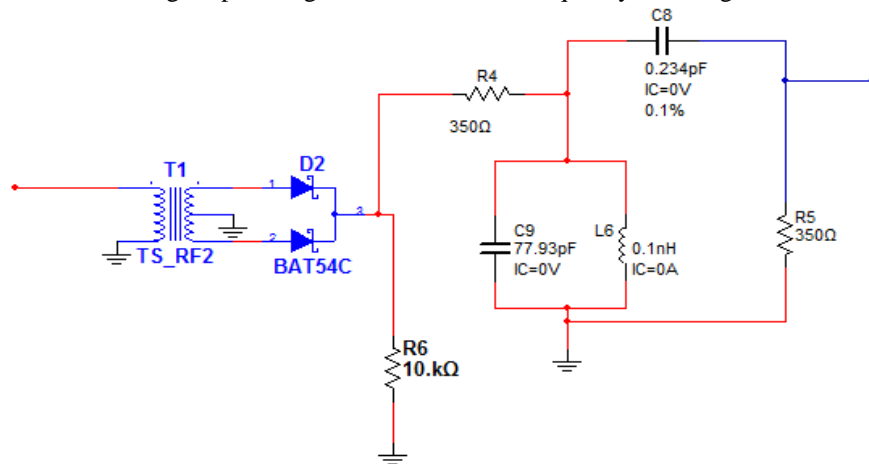


Figure 6: Frequency multiplier circuit of 900MHz to generate 1800 MHz carrier frequency of LO.

In the above circuit full wave rectifier is used to double the given frequency, with RF centered tape transformer and BAT54C_schottky diode [15].

The Schottky diode possesses two unique features as compared to an ordinary P-N junction diode. It is unipolar device because it has electrons as the majority carrier on both side of the junction. An ordinary P-N junction diode is a bipolar device because it has both electrons and hole as the majority carriers. Since no holes are available in metals, there is depletion layer or stored charged to worry about. Hence, schottky diode can switch off faster than bipolar diode. Because of these qualities, schottky diode can easily rectify signal of frequency exceeding 300MHz. [15]

Frequency multiplication can also be done using bridge rectifier with a capacitor and an ordinary diode, but the above method is better. Resistors in (kΩ) were used across the output to obtain large voltage drop. At the receiving end, the same information can be received at different frequencies.

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XI. RESULTS

The output of Dual Band-band pass filter is obtained below;

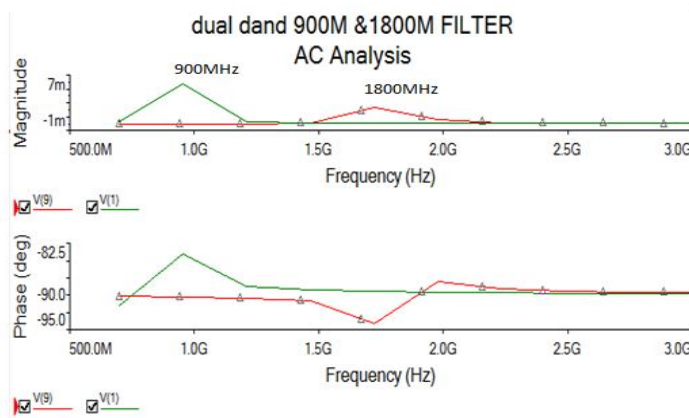


Figure 7: Dual Band-band pass filter of 900MHz and 1800MHz

The model was simulated using sinusoidal input signal. When dual signal of f_1 at centre frequency of 900MHz and 1800MHz is received, the signal will pass through a dual band-band pass filter (BPF) to select the desired frequency and block the others.

The two filters were arranged in parallel to obtain dual band characteristics as can be seen in the fig. 7 above.

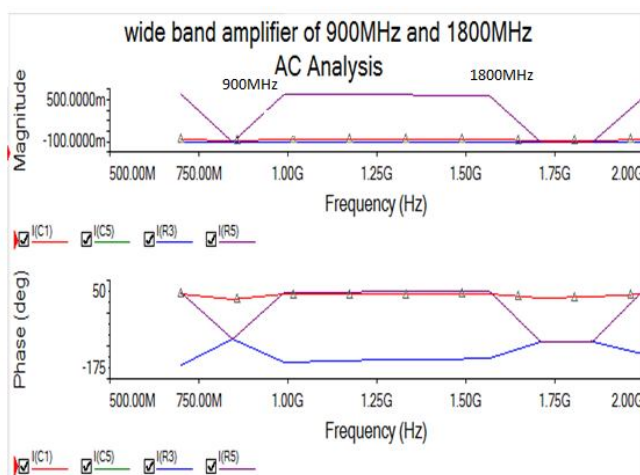


Figure 8; A wide band amplifier

The transfer function of the amplifier is further simplified to obtained poles of frequencies, which are used to plot a graph with a peak at 900MHz and 1800MHz. By turning the inductor L_r . The Figure 9 below shows the transfer function curves.

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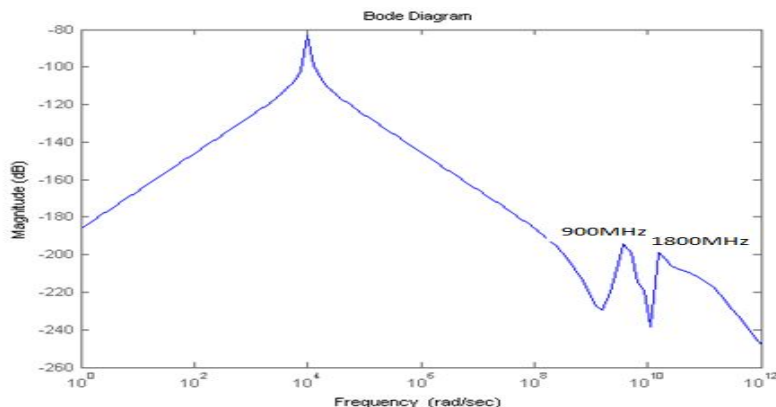


Figure 9; a wide band amplifier transfer function curve

The figure above show the transfer function curved. A peak at 900MHz and 1800MHz.this implies that at all poles; it amplified only at desired frequencies using LC resonance circuit at the output of the amplifier.

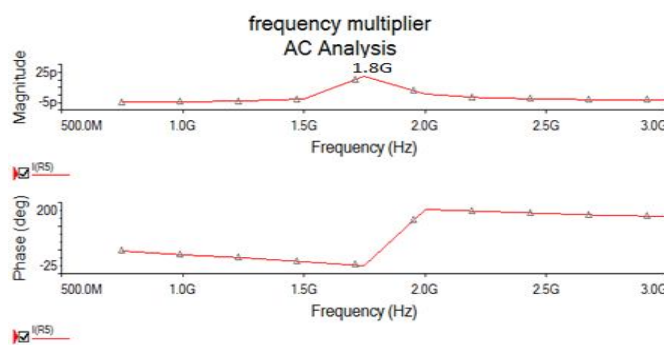


Figure 10; The output ac analysis of multiplier circuit

The above figure indicates the magnitude of frequency doubling at 900MHz to 1.8G.

XII. CONCLUSIONS

We are able to demonstrate that the replacement of two oscillators with a single one is feasible in the detection section of the Hajimiri architecture. The architecture is found to be feasible with additional advantages of low power consumption, light and small chip area. This result implies that, the problem of channel condition can be reduced if this architecture is adopted at both transmission and receptions points.

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