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Department of ECE, Aarupadai Veedu Institute of Technology, Vinayaka Missions University,

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A Novel Approach in Pipeline Architecture for 64-Point FFT Processor without ROM

A.Manimaran, Dr.S.K.Sudheer, Manu.K.Harshan

Associate Professor, Department of ECE, Karpaga Vinayaga College of Engineering and Technology Chennai, India

Assistant professor, Department of ECE, University of Kerala, India

M.E. Embedded System Technologies, Department of ECE, Karpaga Vinayaga College of Engineering and Technology , Chennai, India

Abstract – FFT processor is an important unit in modern wireless communication system. So more research and developments take place in this field. The paper reports low power efficient implementation of FFT processor. Proposed architecture in the design is single-path delay feedback (SDF) pipeline architecture. The requirement of memory and utilization of multipliers is comparatively less in this architecture so that this architecture is very efficient for low power and smaller area FFT designs that is mainly using in portable DSP devices. Proposed architecture completely eliminates the use of ROM by using a reconfigurable complex multiplier and bit-parallel multipliers. Symmetric property of twiddle factor is also used in the proposed multiplier to get low power.

I.INTRODUCTION

In digital signal processing (DSP) discrete fourier transform (DFT) is a very important technique. For telecommunication, particularly for orthogonal division multiplexing (OFDM)[2] systems fast fourier transform is a critical block. Time complexity ($O(N^2)$) and computational difficulty of DFT increase the FFT. FFT is an efficient method to reduce the time complexity to $O(N \log_2 N)$ which was proposed by Cooley and Turkey[5], Here N denotes FFT size.

Implementation of hardware in various papers[6]-[10] is mainly classified into memory based and pipeline architecture style. Mainly memory based and pipeline architecture is adopted to design FFT processor . Design method composed of a main single processing element (PE) and several memory units. The hardware cost and power consumption of this kind of architecture style is lower. But its disadvantage is long latency, long throughput and it cannot be parallelized. Pipeline architecture can get rid off the disadvantage of the above architecture.

In pipeline architecture each stage of FFT using separate arithmetic unit. This approach increase the throughput by a factor of $\log_2 N$ when different units are pipelined. This architecture is also known as cascade FFT architecture and will be used in our proposed design.

Pipeline FFT processors have two popular design types. One uses asingle-path delay feedback (SDF) pipeline architecture[6]-[7], and the other uses a multiple-path delay commutator (MDC) pipeline architecture.The single-path delay feedback (SDF) pipeline FFT is good in its requiring less memory space (about *N*-1 delay elements) and its multiplication computation utilization being less than 50%, as well as its control unit being easy to design. Such implementations are advantageous to low-power design, especially for applications in portable DSP devices. Because of these reasons SDF pipeline architecture is adopted in our design.

FFT computation need to multiply input signals with different twiddle factors, which result in more hardware cost because large size ROM is required and it also increase the area. Designing a FFT processor without ROM we can increase the performance and also can reduce the area. Commonly using word length complex multipliers increase the cost so we are using complex multiplier realized with shift and add operation. The architecture design also use of the symmetric property of twiddle factor[1][3].

The rest of this paper is organized as follows. Abrief review of the fast Fourier transform is described in Section II. In Section III presents our proposed FFT

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architecture. In section IV simulation and result. In section V concluding remarks has given.

II.FFT ALGORITHM

The DFTof an *N*-pointdiscrete-time signal is defined by:

$$X(K) = \sum_{n=0}^{N-1} x(n)\, W_N^{nk}, \qquad 0 \le k \le N-1 \quad (1)$$

Wherethe coefficientW_N^{nk}(alsocalledthe twiddlefactor) isacomplexnumber given by,

$$W_N^{nk} = e^{-j2\pi \frac{nk}{N}} \quad (2)$$

Straight implementation of this algorithm is impractical because large number of multipliers is required for its implementation. So FFT algorithm is required for its efficient implementation and to reduce the hardware cost.Generally, FFT analyses an input signal sequence by using a decimation-in-frequency (DIF) or decimation-in-time (DIT) decomposition to construct an efficiently computational signal-flow graph (SFG).
Decimation in Frequency algorithm Thisalgorithm decomposesevenandodd-indexedfrequencysamples as shown mathematically in equation sets (3) & (4).

$$X(2k) = \sum_{n=0}^{N-1}[x(n)\, W_N^{2nk}]$$

$$= \sum_{n=0}^{N/2-1}[(x(n) + x\left(n+\tfrac{N}{2}\right))\, W_{N/2}^{kn}]$$

$$= \mathrm{DFT}_{N/2}[x(n) + x\left(n+\tfrac{N}{2}\right)] \quad (3)$$

$$X(2k+1) = \sum_{n=0}^{N-1}[x(n)\, W_N^{(2k+1)n}]$$

$$= \mathrm{DFT}_{N/2}[(x(n) - x\left(n+\tfrac{N}{2}\right))W_N^n] \quad (4)$$

An example of radix-2 DIF FFT SFG for *N* = 8 is shown in Fig. 1.

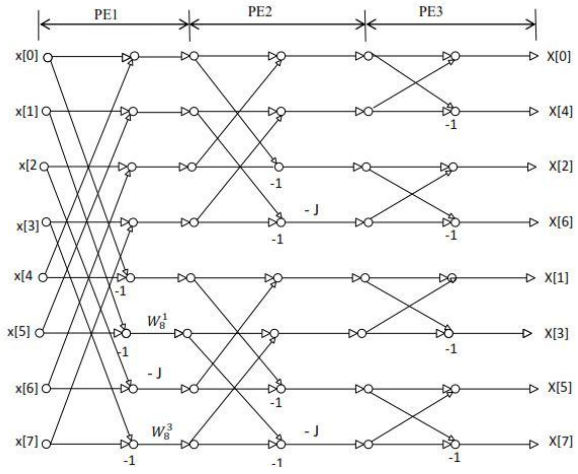

Fig.1 Radix-2 DIF FFT signal-flow graph of length 8

From figure we can analyse that some complex multiplication can be simplified to reduce the chip area and to avoid ROM. Input signal multiplied by w_8^1 in fig can be expressed as:

$$(a+jb)w_8^1 = [(a+b)+j(b-a)]/\sqrt{2} \quad (5)$$

Where $(a+jb)$ denote discrete-time signal in complex form. In similar manner complex multiplication of w_8^3 is given by:

$$(a+jb)w_8^3 = [(b-a)-j(a+b)]/\sqrt{2} \quad (6)$$

Both these equations are required for hardware implementation. Multiplication by $1/\sqrt{2}$ can be obtained easily by using the bit-parallel multiplier explained in the later section.

III. PROPOSED ARCHITECTURE

By considering symmetry of twiddle factors we can reduce the complexity of complex multiplication. Complex multiplication in an FFT must be one of the type given below:

$$W_N^k.(a+jb) = W_N^{k-\left(\frac{N}{4}\right)}.(b-ja), \quad \frac{N}{4} < k < N/2 \quad (7)$$

$$W_N^k.(a+jb) = -W_N^{k-\left(\frac{N}{2}\right)}.(a+jb), \quad \frac{N}{2} < k < 3N/4 \quad (8)$$

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$$W_N^k.(a+jb) = -W_N^{k-\left(\frac{3N}{4}\right)}.(b-ja), \quad \frac{3N}{4} < k < N \quad (9)$$

$$W_N^k.(a+jb) = [W_N^{\left(\frac{N}{4}\right)-k}.(b+ja)]^*, \quad 1 < k < N/4 \quad (10)$$

$$W_N^k.(a+jb) = -j.[W_N^{\left(\frac{N}{2}\right)-k}.(b+ja)]^*, \frac{N}{4} < k < N/2 \quad (11)$$

Twiddle factors are generating using cosine and sine functions. Therefore using all the values of sine and cosine function coming between 0-π/4 the complex multiplication with twiddle factors can be done.

The proposed architecture is composed of three different types of processing elements (PEs), a complex constant multiplier,delay-line (DL) buffers (as shown by a rectangle with a number inside).The proposed architecture uses single path delay feedback. A reconfigurable complex constant multiplier is used to eliminate the twiddle factor ROM. Thus the new multiplication structure becomes the important component in reducing the area and hardware cost. The proposed architecture is shown in Fig. 2

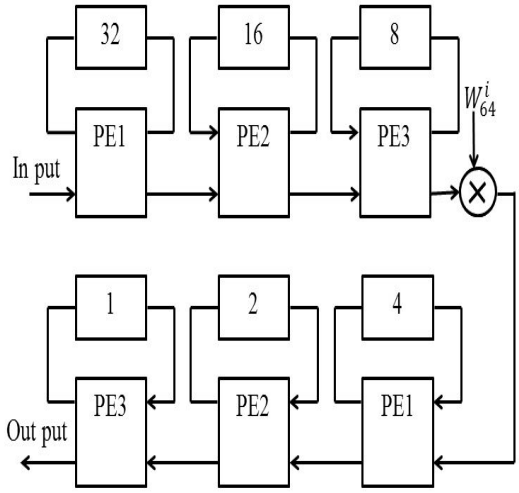

Fig. 2 Proposed radix-2 64-point pipeline FFT processor.

PE3 stage is used to implement a simple radix-2 butterfly structure only, and serves as the submodules of the PE2 and PE1 stages.In the figure, *Iin*and *Iout*are the real parts of the input and output data, respectively. *Qin* and *Qout*denote the image parts of the input and output data, respectively. Similarly, *DL_Iin*and *DL_Iout*stand for the real parts of input and output of the DL buffers,and*DL_Qin*and *DL_Qout*are for the image parts, respectively.The working of processing element 3 (PE3) is as follows and illustrated in Fig.3. When So =0, DL_Iin = Iin ,Iout=DL_Iout ,When So=1 , DL_Iin = DL_Iout + (Iin), Iout=Iin+(-DL_Iout).In PE2 stage,we need toperform the multiplication by -1. In PE2 stage, it is required to compute the multiplication by –*j* or 1. Note that the multiplication by-1 in Fig. 4 is practically to take the 2's complement of its input value.

In the PE1 stage, the calculation is more complex than the PE2 stage, which is responsible for computing the multiplications by $-j$,$W_N^{N/8}$and $W_N^{3N/8}$. But we have seen $W_N^{3N/8} = -jW_N^{N/8}$it can be given by either the multiplication by $W_N^{N/8}$ first and then multiplication by $-j$ or the reverse of the previous calculation. Hence, the designed hardware utilizes this kind of cascaded calculation and multiplexers to realize all the necessary calculations of the PE1 stage. This manner can also save a bit-parallel
multiplier for computing, which further forms a low-cost hardware.

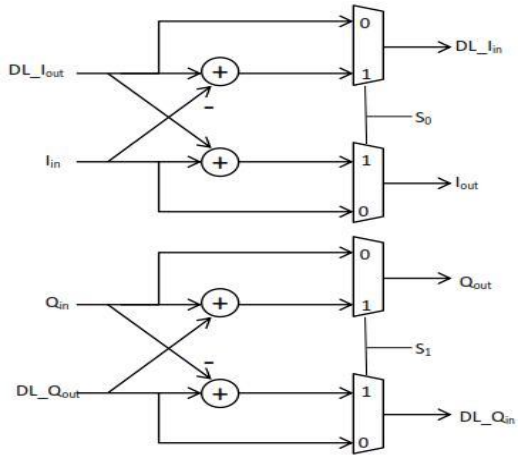

Fig.3 PE3 circuit diagram

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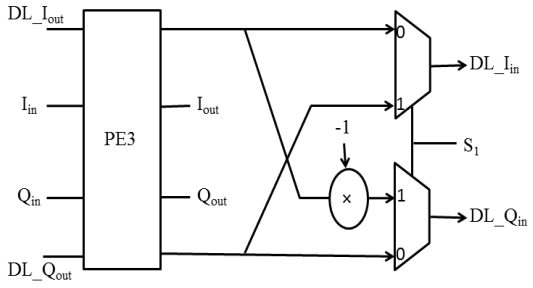

Fig.4 PE2 circuit diagram

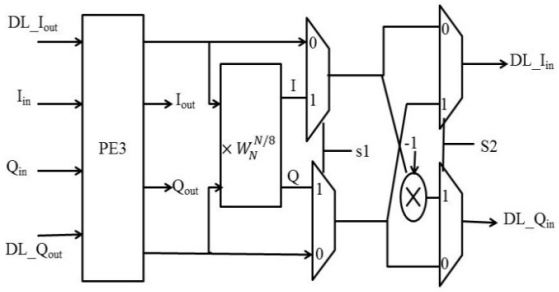

Fig.5 PE1 circuit diagram

In section-II multiplication by $1/\sqrt{2}$ can be employ by bit-parallel multiplier.The bit-parallel operation in terms of power of 2 is given by

$$output = in \times \frac{1}{\sqrt{2}} = in(2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} + 2^{-8} + 2^{-14}) \quad (12)$$

If a straightforward implementation for the above equation is adopted, it will introduce a poor precision due to the truncation error, and will spend more hardware cost. Therefore, to improve the precision and hardware cost, Eq.(12) can be rewrite as:

$$output = in \times \frac{1}{\sqrt{2}} = [1 + (1 + 2^{-2})(2^{-14} + 2^{-6} - 2^{-1})] \quad (13)$$

the circuit diagram of bit-parallel multiplication is illustrated in the fig.6,The complex multiplication by $w_N^{N/8}$ is realised as shown in fig.7 respectively.

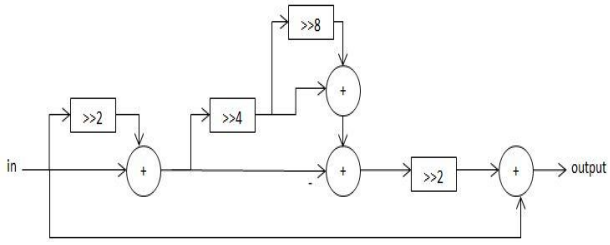

Fig. 6 Circuit diagram of the bit-parallel multiplication by $\frac{1}{\sqrt{2}}$

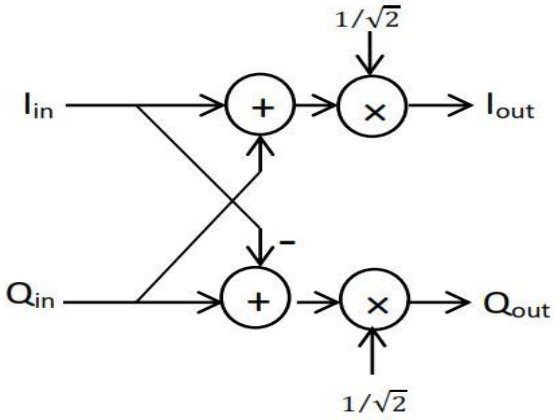

Fig.7 Circuit diagram of the multiplication by $w_N^{N/8}$

Multiplication by w_{64}^{i} is done by a reconfigurable complex constant multiplier. Structure of this complex multiplier also adopts a cascaded scheme to achieve low-cost hardware. Structure is as illustrated in the figure. Circuit in fig.8 is responsible for the multiplication of W_{64}^{i} in the proposed architecture that is shown in the fig. 2

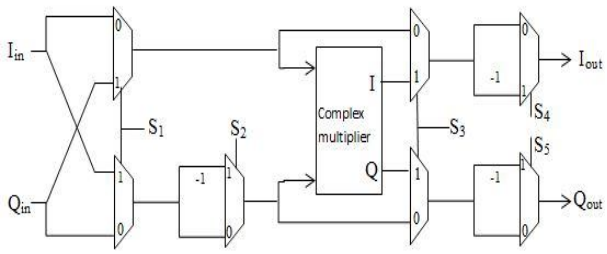

Fig. 8 Proposed reconfigurable complex constant multiplier.

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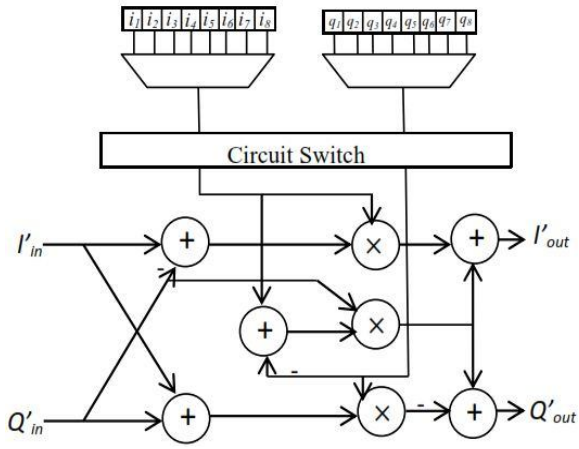

Fig. 9 Complex multiplier used in Fig. 8.

The multiplier in fig.9 is responsible for the twiddle factor complex multiplication in the reconfigurable complex multiplier shown in fig.8. The coefficient values i_1-i_8 and q_1 - q_8 are listed in table I. The twiddle factors in our proposed design is generating using the values in the table.

TABLE I
COEFFICIENT VALUES USED IN FIG.9

Coefficient	value	Coefficient	value
i_1	0.7071	q_1	0.7071
i_2	0.7730	q_2	0.6343
i_3	0.8314	q_3	0.5555
i_4	0.8819	q_4	0.4713
i_5	0.9238	q_5	0.3826
i_6	0.9569	q_6	0.2902
i_7	0.9807	q_7	0.1950
i_8	0.9951	q_8	0.0980

IV.SIMULATION RESULTS

Simulation of 64-point FFT was described in VHDL and Simulation was done in modelsim and the code was functionally verified to be correct.

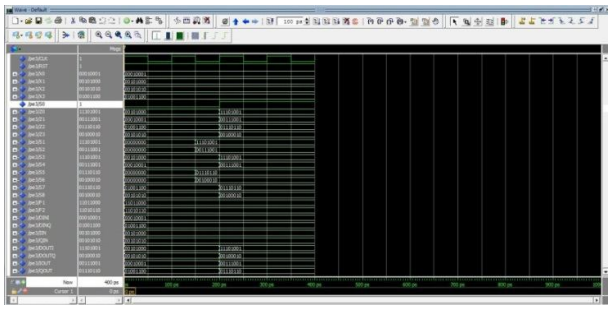

Fig.10 PE3 simulation result

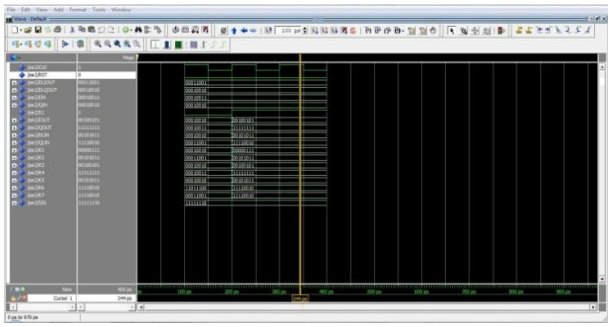

Fig.11 PE2 simulation result

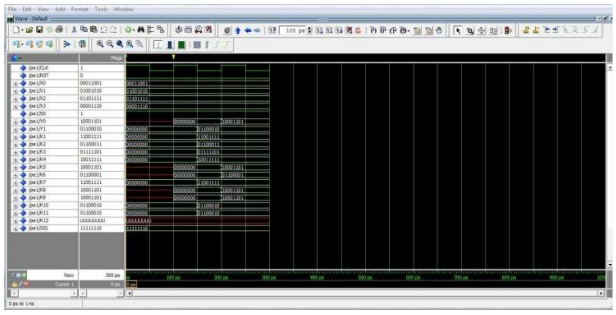

Fig.12 PE1 simulation result

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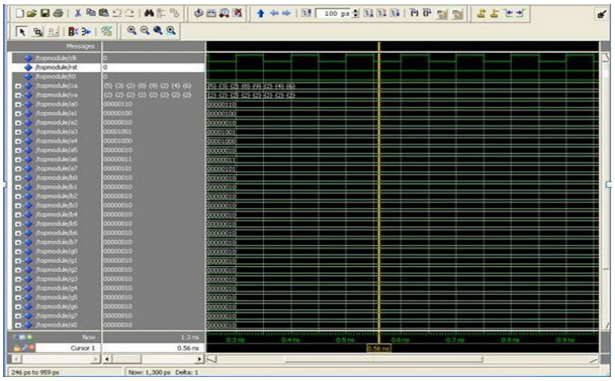

Fig.13 FFT simulation result

From the synthesised power report the following result is obtained. The total dynamic power only 2.1875mW and cell leakage power only 43.6134uW.

V.CONCLUSION

This approach using without ROM and low-power pipeline FFT for OFDM applications have been described in this paper. Considering the symmetric property of twiddle factors in FFT, we have designed a reconfigurable complex constant multiplier such that the size of twiddle factor ROM is significantly shrunk, especially no ROM is needed in our work. By using proposed structure there should be significant reduction in area and hence power. So the proposed architecture can be used in portable DSP devises.

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