A Novel SB-MOSFET with Record Switching Characteristic

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ABSTRACT—This paper presents a novel 65 nm n-channel SB-MOSFET(Schottky barrier MOSFET) based Tunnel Field Effect transistor using Non-Local Band-to-Band tunneling model that shows the good switching characteristic.Stacks of Erbium silicide and Cobalt silicide is used as source/drain because of low schottky barrier height of Erbium silicide and high schottky barrier height of Cobalt silicide. TCAD Simulation is made which shows the result with the record high I_{on}/I_{off} ratio of $4.08{\times}10^9$and the steepest pointsub threshold swing of 77.12mV/decade.

KEYWORDS—SB-MOSFET; rare earth(RE) metals; silicide source/drain; High-K materials; Sub threshold Swing; Band-to-Band Tunneling Model.

I. INTRODUCTION

Recently MOSFET with Schottky source and drain hasbeen considered an important candidate for VLSI because of its ultra-shallow junctions to minimize short-channel effects, low source and drain series resistances, simplified processes, and the elimination of minority carrier injection into the substrate[1].Schottky Barrier MOSFETs(SB-MOSFETs)can be used as an alternative to conventional MOSFETs.SB-MOSFETshave their source/drain regions replaced with metal, typically silicides such as Titanium silicide,Nickel silicide,Platinum silicide, Erbium silicide etc. as opposed to highly doped silicon regions in conventional devices .The main advantage are low parasitic ,superior scaling properties ease of fabrication and low thermal budget.SB-MOSFETs have also been shown to offer immunity to latch-up by essentially eliminating parasitic bipolar actions.An excellent scalability of SB-MOSFETs to sub-10nm gate lengths is feasible due to the low resistance of the silicide regions and atomically abrupt silicide/silicon junctions. silicides are typically at temperature below 973.15 kelvin which makes them compatible for integration with high-K dielectrics and metal gate stacks used in a conventionally sub-65nm CMOS process flow [1]-[5].

II. STRUCTURE & PHYSICS OF THE DEVICE

Fig.1 shows SB-MOSFET with gate length of 65 nm with supply voltage of 0.5 Vand metal as gate material. The source & channel regions are of   p-type and drain and gate regions are of n-type material.In all the simulations, pocket source doped with a concentration of $1{\times}10^{21}$ (n type atoms/cm^3), channel is doped with concentration of $1{\times}10^{20}$ (p type atoms/cm^3) andpocket drain doped with a concentration of $1{\times}10^{21}$ (n type atoms/cm^3). A high-k material HfO$_2$ which is used as the dielectric and Aluminum gate are placed over the channelwith work function of 4.03 eV. Leakage current through the gate oxide should be minimum for the desired reliability and this will achieve when the gate oxide resist with the high electric field. Here, stacks of silicides is used as source/drain in which top material(i.e, Erbium silicide) possess low barrier height(0.28ev) is to provide high on-state current and bottom material(i.e,Cobaltsilicide) possess high barrier height is to provide low off-state current [5]. Non-localBand-to-Band Tunneling model is used which presents the non-local generation rate of electrons and holes caused by phonon-assisted Band-to-Band Tunneling as available in TCAD Synopsys[9],[13].

Let's start the mechanism of SB-MOSFETs from schottky contacts , as we know that for n-type semiconductor with $\Phi_M>\Phi_S$,its equation of current(thermionic emission current , J) in which electron is flowing from metal to semiconductor is

$$J = Aexp(-\frac{q\Phi}{kT})$$

where A is the effective Richardson's constant is the temperature ,$k$is the Boltzmann constant, q is the charge and $\Phi$is the schottky barrier height .But The total current density across a Schottky barrier consists not only of the thermionic emission component but also of a field assisted (thermionic) tunneling component [3].

Higher barrier height reduces thermionic emission and electron tunneling .Firstly thermionic emission takes place , as temperature is decreasing tunneling current start to takes place[13],[12].
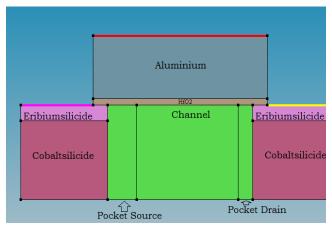

Fig.1. Device Structure of SB-MOSFET

TABLE 1
Description about 65nm gate length SB-MOSFET

Item	Thickness (nm)	Length (nm)
Channel	30	50
Pocket Source	30	10
Pocket Drain	30	5
Erbiumsilicide	5	30
Cobaltsilicide	25	30
Aluminium	20	75
HfO$_2$	0.02	75

A. TUNNELING MECHANISM

TFET is a semiconductor device in which the gate controls the source-drain current through the modulation of Band-to-Band tunneling. BTBT is the quantum mechanical phenomenon in which electrons tunnel from the valance band to condition band (or vice-versa) through the forbidden energy band gap.The important factors of BTBT models are
a) Band structure
b) Dimensionality of the device
c) Local vs. Non-local.

Two different processes for BTBT are direct and phonon assisted BTBT. There are two direct tunneling models are local and non-local model. In local model, electron and holes generation profiles are the same whereas in non-local model holes are generated at the beginning and the electrons at the end of the tunneling path. To understand the nature of the BTBT it is important to understand the approximation made in various simulation models which is also useful for optimizing the design parameter of TFET. To find the optimal solution

for improving the tunnel devices TCAD simulation can be an additional gadget [6, 7].

There are different models which are accepted by the device society to simulate the BTBT such as Non-local BTBT model [8, 9], Schenk BTBT model [11], Hurkx BTBT model [12], Simple (E1) BTBT model [9] etc.Schenk and Hurkx are the local models and as the name says non-local BTBT is non-local model.

Local models means the maximum or average electric field is constant throughout the tunneling. In non-local models the electric field at each point in the tunneling path is dynamically changing that means the tunneling current depends on the band edge profile along the entire path between the points connected by tunneling.Fig 2 shows the 1-D view of BTBT for local and non-local tunneling model. In local model, valance electrons tunnel from position M to N, and the tunnel distance can be obtained by electric field. But in the case of non-local, valance electrons tunnel from position M to N' and the electric field is changing continuously so the tunnel distance is not found.
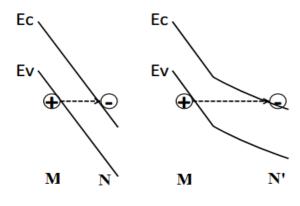

Fig.2.The local and non-local BTBT model.

A non-local BTBT is model in which the conduction and valance band are multi-dimensionally traced to get tunnel paths. The nonlocal electric field is used in famous Kane and Keldysh's formula of BTBT generation rates. The non-local electric field E_{nonl} is defined as the average electric field along the traced tunnel path. Fig.3shows the non-local electric field using band diagram. Here, L is the tunnel length which is obtained by tracing the conduction and valance band to find the same energy level and E_G is the energy band gap [13].
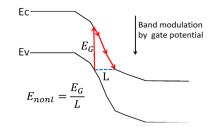

Fig. 3.Non-local electric field using band diagram.

In TFETs, at the source gate overlap region band to band tunneling occurs where the electric field is strongly bended by gate, source and drain voltages. In our device,

this reason is sufficient to use the non-local band to band tunneling model.

A non-local model is the non-local generation of electron and holes caused by direct or phonon assisted band-to-band tunneling process. Phonon assisted band-to-band tunneling process is dominant in indirect semiconductors such as Si and Ge. The BTBT expression is given by[9]

$$R_{net}^P = |\nabla E_V(0)|C_P exp\left(-2\int_0^{x_0}\kappa_V dx\right.$$
$$\left. -2\int_{x_0}^{l}\kappa_C dx\right)\left[\left(exp\left[\frac{\varepsilon - E_{F,n}(l)}{kT(l)}\right]\right.\right.$$
$$\left.+1\right)^{-1}-\left(exp\left[\frac{\varepsilon - E_{F,p}(0)}{kT(0)}\right]+1\right)^{-1}\right]$$

With

$$C_P = \int_0^1\frac{g(1+2N_{op})D_{op}^2}{2^6\pi^2\rho\varepsilon_{op}E_{g,tun}}\sqrt{\frac{m_V m_C}{hl\sqrt{2m_r E_{g,tun}}}}dx\left(\int_0^{x_0}\frac{dx}{\kappa_V}\right)^{-1}\left(\int_{x_0}^l\frac{dx}{\kappa_C}\right)^{-1}$$
$$\left[1-exp\left(-k_{Vm}^2\int_0^{x_0}\frac{dx}{\kappa_V}\right)\right]\left[1-exp\left(-k_{cm}^2\int_{x_0}^l\frac{dx}{\kappa_C}\right)\right]$$

D_{op}, ε_{op} and $N_{op} = \left[exp(\varepsilon_{op}/kT)-1\right]^{-1}$ are deformation potential, energy and number of optical phonons respectively, ρ is the mass density and $\kappa_V\&\kappa_C$ are the magnitudes of the imaginary wave vectors from the Keldysh dispersion relation:

$$\kappa_V = \frac{1}{\hbar}\sqrt{2m_V|\varepsilon - E_V|}\ \Theta(\varepsilon - E_V)$$

$$\kappa_C = \frac{1}{\hbar}\sqrt{2m_C|E_C + \Delta_C - \varepsilon|}\ \Theta(E_C + \Delta_C - \varepsilon)$$

andx_0 is the location where $\kappa_V = \kappa_C$,R_{net}^P is the net hole recombination rate due to the phonon-assisted band-to-band tunneling process.

III. Result & Discussions

We have calculated drain current Vs gate voltage , Ion/Off ratio and sub threshold swing at different gate lengths and gate lengths Vs threshold voltage on Synopsys TCAD [10]. All resuts are based on simulation .Fig.4 shows the drain current versus gate voltage for three different gate Lengths.
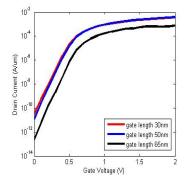

Fig. 4.$I_d$vs.V_{gs} curve for different gate lengths.

Here, we can see that the gate length of 65nm shows the highest I_{on}/I_{off} ratio in comparison to other gate lengths.

Gate Length	Ion/Ioff	Subthreshold (mV/decade)
30nm	7.91×10^7	82.141
50nm	3.23×10^8	79.624
65nm	4.08×10^9	77.129

TABLE.2.
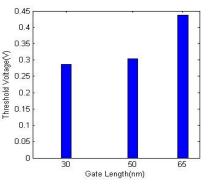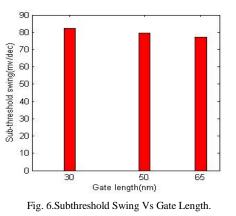Ion/Off ratio and sub threshold swing at different gate lengths

Fig. 5.Gate Length Vs Threshold voltage .

With increase in gate length ,threshold voltage also increase because of DIBL(Drain induced barrier lowering) as shown in Fig.5. One of the important requirements regarding switching characteristic of the Tunnel FET is the subthreshold swing.Fig.Fig.6 shows the pointsub threshold swing (SS) decreases with increase in gate length and it show good result at 65nm gate length.

Fig. 6.Subthreshold Swing Vs Gate Length.

IV. Conclusion

This work presents a novel 65 nm n-channel SB-MOSFET with stack of Erbiumsilicide and Cobaltsilicide as the source/drain, Aluminium as the gate, p-type material as the substrate and HfO_2 dielectric constant as oxide.TCAD Simulation is made which shows the result with the record high I_{on}/I_{off} ratio of $4.08\times10^9$and the sub threshold swing of 77.12 mV/decade. This is the highest I_{on}/I_{off} ratio recorded for the SB-MOSFET.

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