ISSN (Online) : 2319 - 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

Volume 3, Special Issue 3, March 2014

2014 International Conference on Innovations in Engineering and Technology (ICIET'14)
On 21st & 22nd March Organized by

K.L.N. College of Engineering, Madurai, Tamil Nadu, India

A Novel Single Phase Cascaded H-Bridge Inverter with Reduced Power Electronics Switches

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ABSTRACT— This project presents single-phase cascaded H-Bridge Inverter with minimum number of power electronics devices. The proposed Inverter consists of 4 unidirectional switches and single bidirectional switch in each cell. Single carrier and multicarrier PWM method is used to generate the multilevel output. The proposed multilevel Inverter is compared with conventional symmetrical CHB, Asymmetrical CHB with binary and trinary configurations. The comparison will be made on the basis of number of components, number of DC sources, number of Balancing capacitors, Switching and conduction losses. The proposed Cascaded H-Bridge Inverter will be simulated using MATLAB/SIMULINK and will be implemented in hardware also using SPARTAN3A DSP.

KEYWORDS - Bi-directional Switches, Cascaded H-bridge Inverter, DC to DC Boost Converter, Multi carrier PWM, PV array.

I. INTRODUCTION

Over the past few years, technological advances in power electronics and increasing demand for energy have contributed to rapid development of power generation based on renewable energy sources as like the Photovoltaic (PV), Wind and Fuel cell (FC) based renewable energy technologies [3].

One of the problems focused in the research is the constraint of power electronic switches. If the power electronic devices which can prolong high voltage are used in the inverter, their switching frequency is restricted. Hence, the device voltage must be reduced to use high-speed switching devices. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. Further, increase in number of isolated DC sources in order to increase the number of output voltage levels leads to additional system complexity especially in PV and FC fed inverter topologies. In single-phase multi-level inverters, the most widely used techniques are cascaded H-bridge (CHB), diode-clamped and capacitor-clamped types [7-9]. In addition, many other techniques also exist. In particular, among these techniques, CHB single phase inverters have drawn attention because of their modularized circuit layout and simplicity. A variety of modulation techniques can be applied to CHB inverters. By increasing the number of cascaded H-bridges, the number of levels in CHB inverters increases. Generally if the number of output voltage levels is increased, then the number of power electronic devices and the number of isolated DC sources is also increased. This makes a CHB inverter further complex.

In this paper, a novel multilevel inverter with minimum number of power electronic switching devices is proposed which is a modified version of the multilevel inverter using series/parallel conversion of DC sources. In the proposed Multilevel Inverter three similar Cascaded H-Bridges are used, each Bridge carries an auxiliary switch which will be Bi-directional in nature. However, three isolated dc sources are needed to generate the same number of output levels as compared to the conventional Cascaded H-Bridge Inverters. The number of switching devices used and the harmonics of the output voltage waveform for the proposed inverter are reduced as well. The proposed multilevel inverter topology can be extended for the application of grid connected photo voltaic systems, hybrid electric vehicles, etc.

Furthermore, theoretical analysis, numerical simulations and experimental results are also presented to demonstrate the validity of the proposed single phase cascaded multilevel inverter.

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The term Multilevel began with the three-level converter. The concept of multilevel converters has been introduced since 1975 [1]. The cascade multilevel inverter was first proposed in 1975. In recent years multi level inverters are used high power and high voltage applications. Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multi level inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor [2-3].There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM. Among these PWM methods SPWM is the most used for the multilevel inverter, because it has very simple and easy to implemented [7]. This proposed work is implemented with another major advantage of using the supply as the Renewable energy sources (PV Cells). The individual PV string feds the power to each H bridges. The output from the PV string will be very small in value hence, the output voltage can be boosted up by the use of boost converter. The boost converter is used for two purposes. (i) Boost converter acts as a DC-DC step up transformer, to boost up the voltage required to drive the inverter. (ii) Boost converters are used for balancing the input capacitor voltages. The output from the boost converter feds the power to the inverter structure which drives the load connected across its terminals. The Overall Block Diagram for the Proposed Inverter is shown in Fig 1.1.

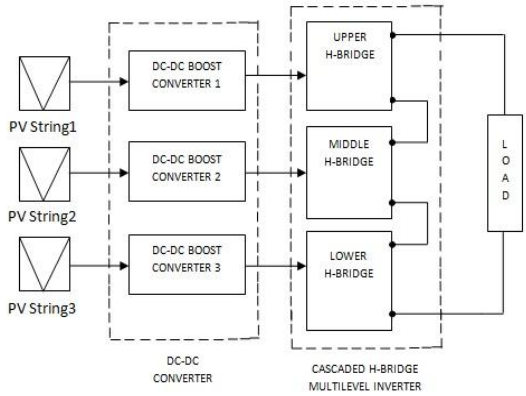

Fig. 1.1 Overall Block Diagram

II. PROPOSED INVERTER CONFIGURATION

A. INTRODUCTION

Fig. 2. shows the circuit configuration of the proposed cascaded H bridge multilevel inverter with three H-Bridge inverters connected in cascade (Upper , Middle and Lower H-bridge inverters). As shown in Fig. 2, in the lower H bridge, an auxiliary circuit comprising of four diodes and a switch is placed between two DC sources.

This cascaded multilevel inverter made up of series connected single full bridge inverter each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources, which is obtained from solar photo voltaic cells. This type of converter does not need any transformer or clamping diodes or flying capacitors. Each level can generate five different voltage outputs $+V_{dc}$, $+1/2v_{dc}$, 0 ,$–V_{dc}$ and $–1/2v_{dc}$ by connecting the dc sources to the ac output side by different combinations of the five switches.

The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Further, each switching device always conducts for 180˚ (or half cycle). This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work.

B. OPERATION

The circuit diagram of proposed method of multilevel cascaded inverter as shown in Figure 2. It consists of three full-bridge cells, capacitor voltage divider, three auxillary switches. The inverter produces output voltage in thirteen levels: $0.5V_{dc}$, V_{dc}, $1.5V_{dc}$, $2V_{dc}$, $2.5V_{dc}$, $3\ V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$, $-2V_{dc}$, $-2.5V_{dc}$, $-3\ V_{dc}$. The advantages of the inverter topology are: Improved output voltage quality, Smaller filter size, Lower Electromagnetic interferences, Lower total harmonics distortion compared with conventional fifteen level pulse

width modulation with reduced number of switches compared to the conventional CHB inverter.

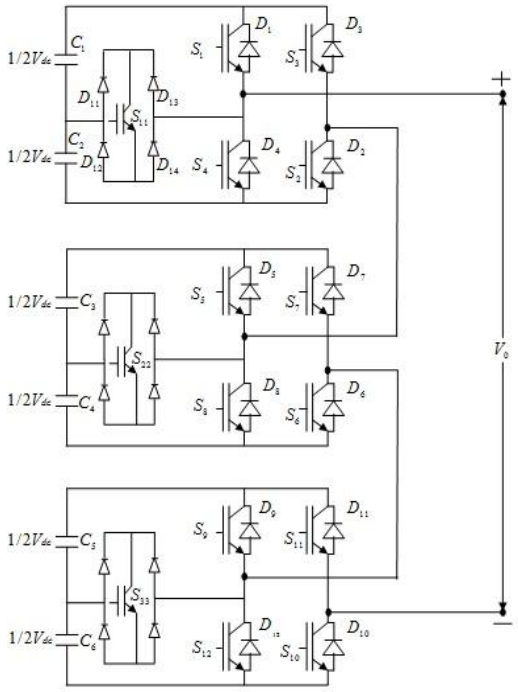

Fig. 2.1 Cell Configuration for the Proposed Inverter.

The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to two capacitors 0.5Vdc. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, The system consists of 15 switches which can be used to produce those thirteen different output voltage levels such as, 0, 0.5 V_{dc}, 1 V_{dc}, 1.5 V_{dc}, 2 V_{dc}, 2.5 V_{dc}, 3 V_{dc}, -0.5 V_{dc}, -1 V_{dc}, -1.5 V_{dc}, -2 V_{dc}, -2.5 V_{dc}, -3 $V_{dc.}$ The switching strategy for various output voltages in the proposed 3 cell configuration is clearly shown in Table I.

TABLE I
THIRTEEN-LEVEL CASCADED H-BRIDGE INVERTER OUTPUT VOLTAGE

UPPER INVERTER	MIDDLE INVERTER	LOWER INVERTER	TOTAL OUTPUT VOLTAGE
S1,S2	S5,S6	S9,S10	$3V_{dc}$
S1,S2	A2,S6	S9,S10	$2.5V_{dc}$
S1,S3	S5,S6	S9,S10	$2V_{dc}$
A1,S2	S5,S7	S9,S10	$1.5V_{dc}$
S1,S3	S5,S7	S9,S10	V_{dc}
A1,S2	S6,S8	S10,S12	$0.5V_{dc}$
S1,S3	S5,S7	S9,S11	0
S1,S3	A2,S7	S9,S11	$-0.5V_{dc}$
S2,S4	S6,S8	S11,S12	$-V_{dc}$
A1,S3	S6,S8	S11,S12	$-1.5V_{dc}$
S1,S3	S7,S8	S11,S12	$-2V_{dc}$
S3,S4	A2,S7	S11,S12	$-2.5V_{dc}$
S3,S4	S7,S8	S11,S12	$-3V_{dc}$

When a switch S2 and S4 of one particular H-bridge inverter are closed, the output voltage is 0 .When a switch S2, A5, are closed, the output voltage is $+0.5V_{dc}$. When a switch S1, S2, S6, S8, S10, S12 are closed, the output voltage is $+V_{dc}$.. When a switch A1, S2, S5, S6, S10, S12 of one particular H-bridge inverter are closed, the output voltage is $+1.5V_{dc}$. When a switch S1, S2, S5, S6, S10, S12 are closed, the output voltage is $+2V_{dc}$. When a switch S1, S2, S5, S6, A3, S10 are closed, the output voltage is $+2.5V_{dc}$. When a switch S1, S2, S5, S6, S9, S10 are closed, the output voltage is $+3V_{dc}$. Similarly for the negative voltages the switching sequences appears. Therefore totally, thirteen levels of output voltage appears on the load side.

C. COMPARISION BETWEEN DIFFERENT TOPOLOGIES

The proposed topology is compared with conventional symmetrical CHB inverters, asymmetrical CHB inverter with 1:3 configuration , asymmetrical CHB inverter with 1:2:4 configuration and asymmetrical CHB inverter with 1:3:9 configuration. The comparison is done on the basis of number of components and rating of the devices [8].
As per the comparison, In the symmetrical CHB - to produce a 5 level output, eight switches are required in the ratio of 1:1 configuration. Similarly for a 7 level output, same eight switches are required in the ratio of 1:1:1 configuration. Further, to increase the levels the voltage ratios must be increased, $V_{dcn}/V_{dco = n,}$ that depends upon the number of output voltage level required.

TABLE II
COMPONENT LEVEL COMPARISION OF DIFFERENT TOPOLOGIES OF MLI

S. No	TYPE OF INVERTER	Primary Devices	OUTPUT LEVEL
1	Diode Clamped Multi-level Inverter	PD_{11}=14 for 13 levels $PD_N=PD_{(N-4)}+3$ Where N=levels	N=13
2	MLISPC	PD_{11}=14 for 13 levels $PD_N=PD_{(N-4)}+3$ Where N=levels	N=13
3	Conventional CHB	PD_{11}=13 for 13 levels $PD_N=PD_{(N-4)}+4$ Where N=levels	N=13
4.	Proposed Inverter	PD_{11}=13 for 13 levels $PD_N=PD_{(N-4)}+4$	N=13

III. PWM MODULATION STRATEGY

The modulation index *M* of the proposed multilevel inverter is defined by

$$M = \frac{1}{2}\frac{V_{ref}}{V_{cr}} \quad (1)$$

Where, V_{ref} is the amplitude of the voltage reference and V_{cr} is the amplitude of the carrier signal.

Multicarrier phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals. The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of cells, the carrier phase shift for each cell $\theta Cr,n$ can be obtained from,

$$\theta_{cr,n} = \frac{2\pi(n-1)}{N_c}, n = 1,2,..... n_c \quad (2)$$

The references, *v*ref1 and *v*ref2 are derived from a full-wave voltage reference, *V*ref defined by

$$V_{ref} = M \sin \omega t \quad (3)$$

$$V_{ref1} = |V_{ref}| \quad (4)$$

$$V_{ref2} = V_{ref1} - \frac{1}{2} \quad (5)$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is 1/2. When the voltage reference is between $0 < v_{ref} \leq (1/2)$, v_{ref1} is compared with the triangular carrier and alternately switches *S*1 and *S*3 while maintaining *S*5 in the ON state to produce either $(1/2)v_{dc}$ or 0. Whereas, when the reference is between $(1/2) < v_{ref} \leq 1$, v_{ref2} is used and alternately switches *S*1 and *S*2 while maintaining *S*5 I n the ON state to produce either $(1/2)v_{dc}$ or v_{dc}. As for the reference between $-(1/2) < v_{ref} \leq 0$, *v*ref1 is used for comparison which alternately switches *S*1 and *S*2 while maintaining *S*4 in the ON state to produce either $-(1/2)v_{dc}$ or 0. For a voltage reference between $-1 < v_{ref} \leq -(1/2)$, v_{ref2} is compared with the carrier to produce either $-(1/2)v_{dc}$ or $-v_{dc}$ alternately switches *S*1 and *S*3, maintaining *S*4 in the ON state. It is noted that two switches, *S*4 and *S*5, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency.

The various output voltage for the each cells (ie., Upper, Middle, Lower) is obtained. And the combination of these voltage levels is the total output voltage for the proposed Inverter.

The separate reference waves are developed by using a Interpreted MATLAB function, and hence the developed signal is shown in Fig. 3.1. and Similarly for the Middle and Lower level Bridges in Fig. 3.2 and Fig. 3.3.

The Generated Gate pulses are fed to the relevant Inveter Bridges and hence the desired output for each and every bridge is obtained, the number of output levels generated are combined to get the actual number (ie., thirteen level output) of output levels are generated.

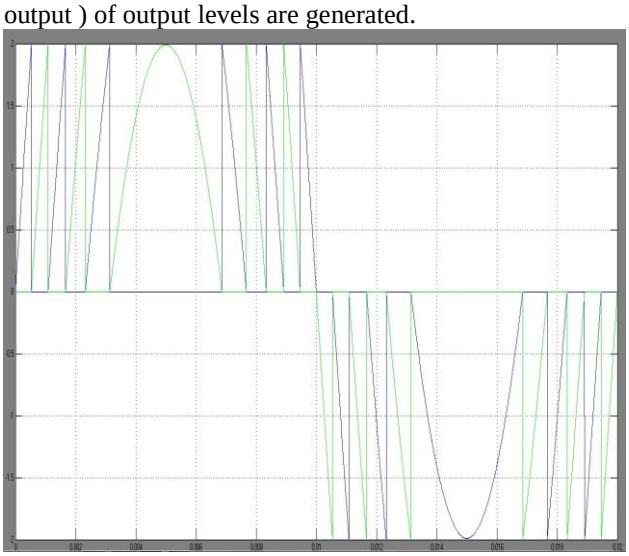

Fig. 3.1. Reference Wave Signal Generation for the Upper Bridge Inverter.

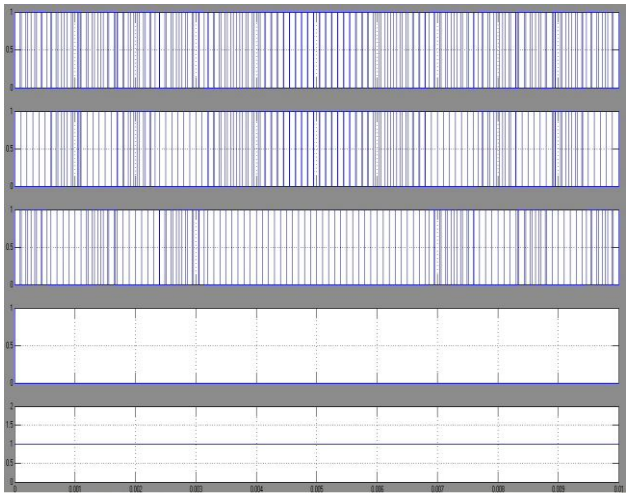

Fig. 3.2. Generated Gate Pulses for Upper Bridge Switches.

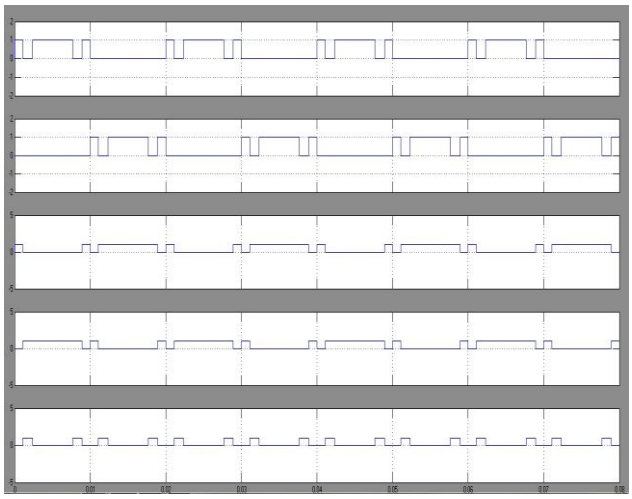

Fig. 3.3 Generated Gate Pulses for Middle and Lower Bridge Switches.

IV. SIMULATION RESULTS

The Above Cascaded Multi-level Inverter is Simulated by using MATLAB/SIMULINK software tools for generating the 13 Level output voltage.

This simulation is carried out for each cells in the proposed Inverter and the combined result is taken as the total output voltage. To validate the proposed inverter topology simulation has been carried out for the proposed inverter in Matlab/Simulink. The PWM modulation strategy discussed in section III was implemented in the simulation upto 13 levels and the same can be extended to any required level. Table I gives the different switching strategies for each and every cells in the proposed inverter. The upper inverter is operated at high switching frequency that is equivalent to the carrier frequency. The output voltages for the each cells are shown in Fig. 4.3.

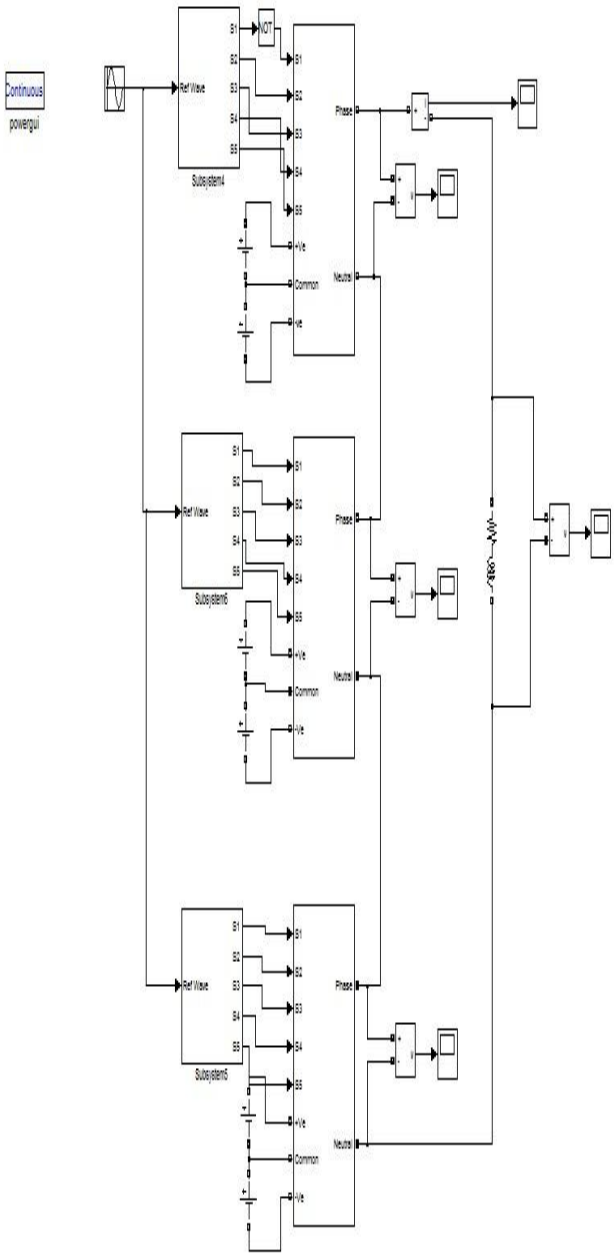

Fig. 4.1. MATLAB/SIMULATION Diagram- Proposed Cascaded H-Bridge Multi-Level Inverter

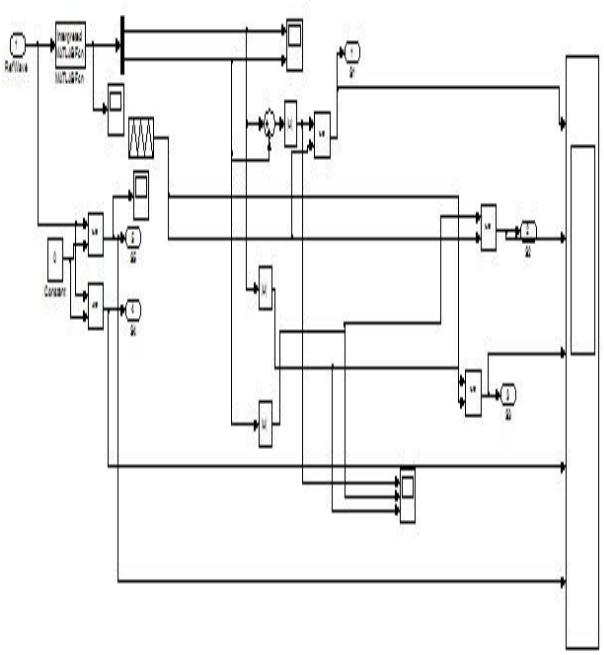

Fig. 4.2. Reference Wave Signal Generation for the Upper Bridge Inverter.

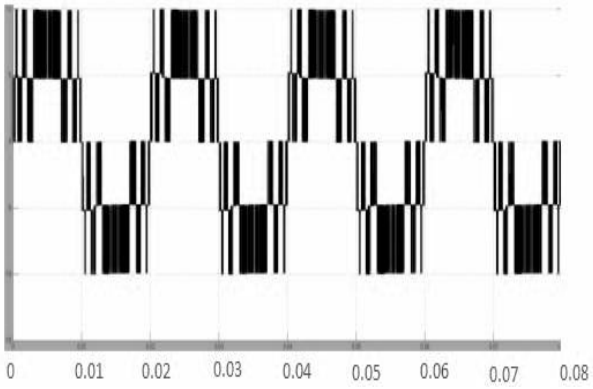

Fig. 4.3. Generated output Waveform for the Upper Bridge Inverter.

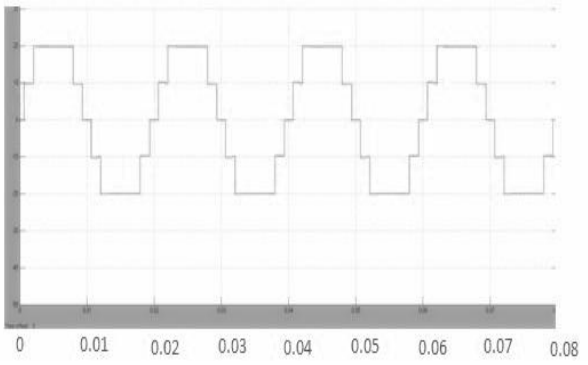

Fig. 4.4. Generated output Waveform for the Middle Bridge Inverter.

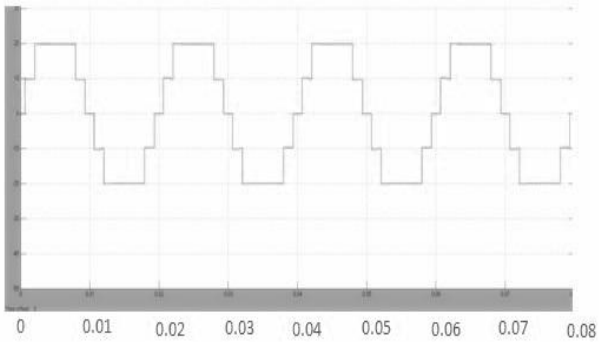

Fig. 4.5. Generated output Waveform for the Lower Bridge Inverter.

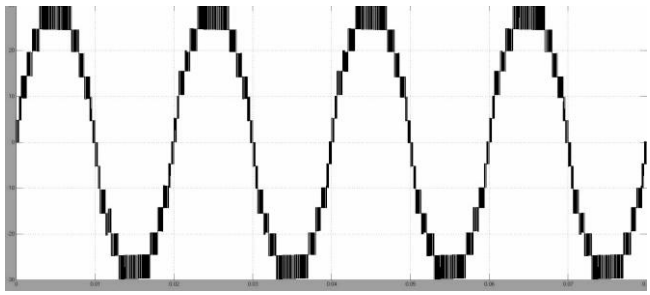

Fig. 4.6. Total Output Voltage for the Proposed Cascaded H-Bridge Inverter.

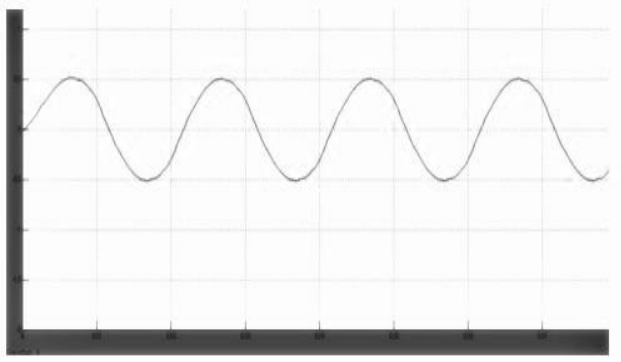

Fig. 4.7. Output Current Waveform for the Proposed Cascaded H-Bridge Inverter.

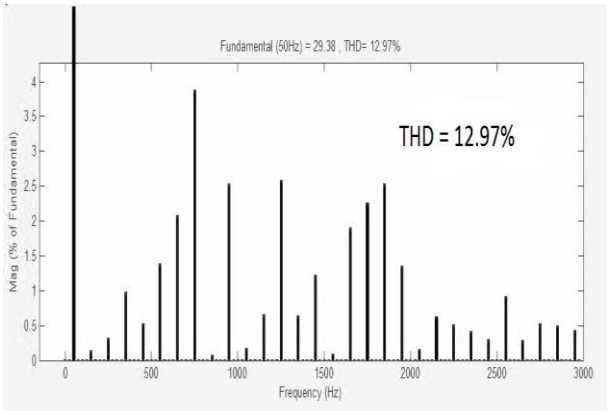

Fig. 4.8. Line Voltage Harmonics with THD value.

V. CONCLUSION

This paper has presents a novel single phase cascaded H-bridge Inverter with reduced number of power electronics devices and isolated DC sources. Simulations are carried out in MATLAB/Simulink. A Generalized switching algorithm which can be used for any number of levels is presented. The performance of the suggested novel cascaded H-Bridge multilevel inverter is investigated in detail. The modulation waveform and the harmonic analysis are also presented for various values of modulation strategies. By properly adjusting the modulation index, the required number of levels of the inverter output voltage can be achieved. This proposed inverter system offers the advantage of reduced switching devices and isolated DC sources when compared to the conventional CHB and MLISPC for the same number of output levels. Also, high frequency switching devices are operated at low voltage and low frequency devices are operated at high voltage. Thus it can be concluded that the proposed novel Cascaded H-Bridge Multilevel inverter can be used for medium and high power applications. The simulation results will be verified experimentally using SPATRAN3A DSP.

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