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A PSCAD/EMTDC Model for H-Bridge Converter Based DVR for Mitigation of All Symmetrical & Asymmetrical Faults

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ABSTRACT— The growth in the use of power electronics has created a greater awareness of power quality. Power Quality (PQ) has been an issue is becoming increasingly pivotal in industrial electricity consumer's point of view in recent times. PQ has become important, especially, with the induction of sophisticated load, whose performance is very sensitive to the quality of power supply, so such type of problems can eliminate by using custom power devices. One of these modern devices is the Dynamic Voltage Restorer (DVR), which is a more efficient and effective modern custom power device. This paper presents the analysis & design of three phase H-bridge converter based DVR for protect sensitive load from polluted distributed network. The main objective of this paper is to save sensitive load from non linear voltages, currents and avoid PQ problem like voltage sag, swell conditions, in addition to the phase angle jump. Modeling & simulation of proposed DVR are implemented in PSCAD/EMTDC platform.

KEYWORDS— Dynamic voltage restorer (DVR), H-bridge converter, voltage sags, Power Quality (PQ), PSCAD/EMTDC.

I. INTRODUCTION

The importance of power quality (PQ) has risen very considerably over the last two decades due to a marked increase in the number of equipment which is sensitive to adverse PQ environments, the disturbances introduced by Non-linear loads, and the proliferation of renewable energy sources, among others. At least 50% of all PQ disturbances are of the voltage quality type, where the interest is the study of any deviation of the voltage waveform from its ideal form. The best well-known disturbances are voltage sags and swells, harmonic and inter-harmonic voltages, and, for three phase systems, voltage imbalances [4]. Voltage sag is normally caused by short-circuit faults in the power network or by the starting up of induction motors of large rating. The ensuing adverse consequences are a reduction in the energy transfers of electric motors and the disconnection of sensitive equipment and industrial processes brought to a standstill.

The DVR is essentially a voltage-source converter connected in series with the ac network via an interfacing transformer, which was originally conceived to ameliorate voltage sags. However, as shown in this paper, its range of applicability can be extended very considerably when provided with a suitable control scheme [5]. The basic operating principle behind the DVR is the injection of an in phase series voltage with the incoming supply to the load, sufficient enough to re-establish the voltage to its pre-sag state [8]. Its rate of success in combating voltage sags in actual installations is well documented, this being one of the reasons why it continues to attract a great deal of interest in industry and in academic circles [7].

This paper presents a H-Bridge cascaded converter avoid unequal device rating and unbalanced dc link voltage problems, in addition with power quality problems. In this paper, the power circuit design and controller design a consideration of an ac stacked multilevel converter using cascaded H-bridges is studied for DVR application [6].

II. Dynamic voltage restorer

Dynamic Voltage Restorer is a series connected device designed to maintain a constant voltage value across a sensitive load. The DVR considered consists of:

a) an injection / series transformer,
b) a harmonic filter,
c) a Voltage Source Converter (VSC),

d) an energy storage and
e) a control system

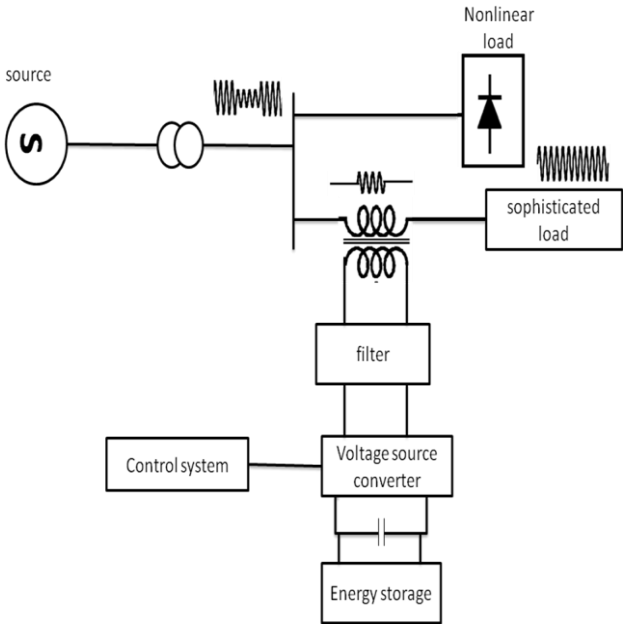

Fig 1 Schematic Diagram of DVR Configuration

The main function of a DVR is the protection of sensitive loads from voltage sags/swells coming from the network. Therefore as shown in Figure 1, the DVR is located on approach of sensitive loads. If a fault occurs or any nonlinear load connected with other lines, DVR inserts series voltage V_{DVR} and compensates load voltage to a pre-fault value. The amplitudes of the three injected phase voltages are controlled such as to eliminate any detrimental effects of a bus fault to the load voltage V_L. This means that any differential voltages caused by transient disturbances in the AC feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the booster transformer. The DVR works independently of the type of fault or any event that happens in the source side, provided that the whole system remains connected to the supply grid, i.e. the line breaker doesn't trip. For most practical cases, a more economical design can be achieved by only compensating the positive and negative sequence components of the voltage disturbance seen at the input of the DVR. This option is Reasonable because for a typical distribution bus configuration, the zero sequence part of a disturbance will not pass through the step down transformer because of infinite impedance for this component.

The DVR has two modes of operation which are: standby mode and boost mode. In standby mode (*VDVR*=0), the booster transformer's low voltage winding is shorted through the converter. No switching of semiconductors occurs in this mode of operation, because the individual converter legs are triggered such as to establish a short-circuit path for the transformer connection. Therefore, only the comparatively low conduction losses of the semiconductors in this current loop contribute to the losses. The DVR will be most of the time in this mode. In boost mode (*VDVR*>0), the DVR is injecting a compensation voltage through the booster transformer due to a detection of a supply voltage disturbance [4].

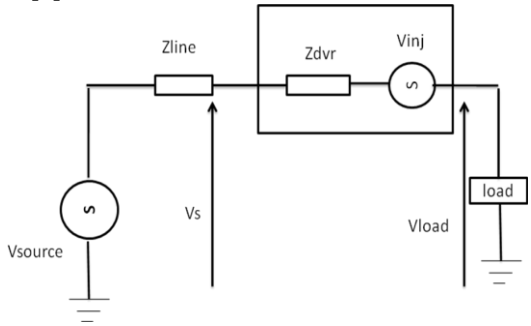

Figure 2 Equivalent circuit of DVR

Figure 2 show the equivalent circuit of DVR when the source voltages is drop or increase, the DVR injects a series voltage V_{inj} through the injection transformer so that the desired load voltages magnitude V_L can maintained. Mathematical expressed the injection satisfies

$$V_L = V_S + V_{inj} \quad (1)$$

Where V_L is load voltage, V_S is supply voltage& is the voltage injected

$$S_L = V_L I_L \quad (2)$$

$$S_L = P_L + jQ_L = (P_S + jQ_S) + (P_{inj} + jQ_{inj}) \quad (3)$$

III. POWER ARCHITECTURE

Although various topologies may be used to realize the VSC illustrated in Fig. 3, at higher power levels H-bridge multilevel power converters are seen to have advantages in several aspects [7], [8]. First, multilevel converters can realize the higher power and high voltage using semiconductor switches of relative small ratings while avoiding the voltage sharing and current sharing problems associated with series and parallel connection of switches commonly employed in two-level converter realization. Second, multilevel converters can integrate the output voltage with smaller steps and reduced harmonic content, while potentially resulting in smaller thus lower electromagnetic interference (EMI). Third, compared with diode clamped multilevel topology, the H-bridge structure can avoid unequal device rating and unbalanced DC link voltage problems. When compared to flying-capacitor topology, the H-bridge multilevel converter has less storage capacitors and requires simpler control [9]. Finally, it is worth noting that the modularity nature of the H-bridge cascaded multilevel converter makes an easier realization.

The proposed power architecture of the transformer coupled H-bridge converter is illuminated in Fig. 3. Each phase is composed of three H-bridge inverters. The outputs of the converters are connected in series through transformers. This architecture fits with the DVR application, which automatically involves a series injection of the compensating voltage source. Furthermore, instead of using isolated dc link for each H-

bridge inverter, a common dc link bus connects all H-bridge inverters dc ports in parallel. This is contrasting from the conventional H-bridge cascaded multilevel converter [13]. This is also different from multiple six-pulse three- Switches (IGBT's) constituting the voltage source converter. The commutation pattern is
Generated by means of the sinusoidal pulse width modulation technique (SPWM); voltages are controlled through the phase modulation. The block diagram of the phase locked loop (PLL) is converters [10].

CONTROL PHILOSOPHY

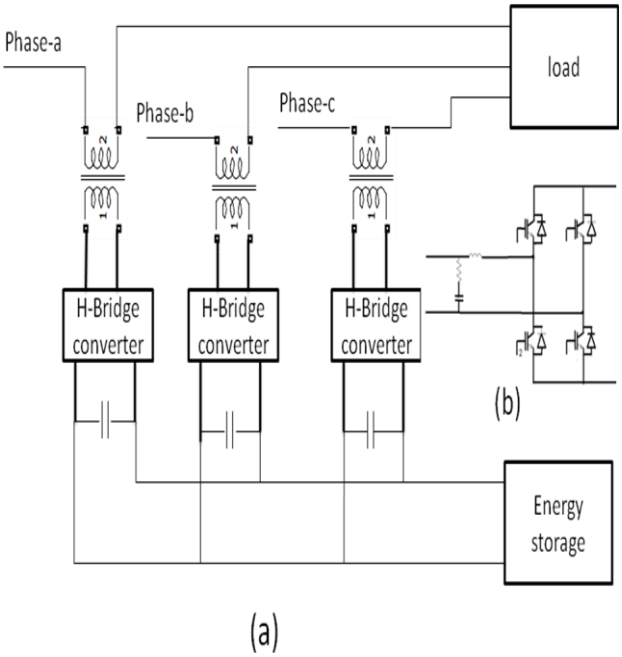

Figure 3 Proposed power architecture of the transformer Coupled H-bridge converter applied to DVR

The basic functions of a controller in a DVR are the detection of voltage sag/swell events in the system; computation of the correcting voltage, generation of trigger pulses to the sinusoidal PWM based DC-AC inverter, correction of any anomalies in the series voltage injection and termination of the trigger pulses when the event has passed. The controller may also be used to shift the DC-AC inverter into a rectifier mode to charge the capacitors in the DC energy link in the absence of voltage sags/swells. The dqo transformation or Park's transformation [11] is used to control of DVR. The dqo method gives the sag depth and phase shift information with start and end times. The quantities are expressed as the instantaneous space vectors. Firstly convert the voltage from a-b-c reference frame to d-q-o reference.

Figure 4 illustrates a flow chart of the feed forward dqo transformation for voltage sags/swells detection. The detection is carried out in each of the three phases. The error signal is used as a modulation signal that allows generating a commutation pattern for the power Illustrated in Figure 4. The PLL circuit is used to generate a unit sinusoidal wave in phase with mains voltage.

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (4)$$

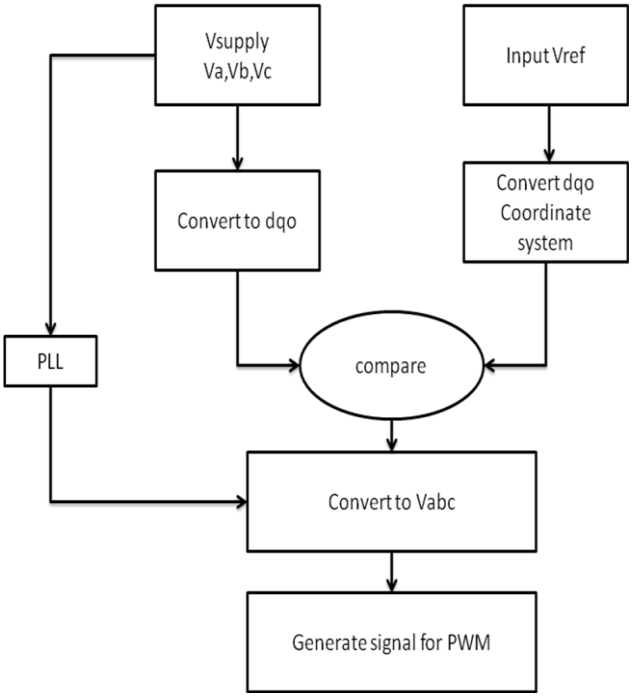

Fig 4 Flow chart of DVR operation

Equation (4) defines the transformation from three phase System abc to dqo stationary frame. In this Transformation, phase A is aligned to the d-axis that is in quadrature with the q-axis. The theta (θ) is defined by the angle between phase A to the d-axis.

IV. SIMULATION RESULTS & DISCUSSIONS

A detailed simulation of the DVR control system is performed using PSCAD/EMTDC model as show in order to verify the operation. The parameters of the DVR system are shown in (Table-1);

Table-1 System data

S.No	Parameters	Values used in the Simulation Models
1	Supply voltage	400V
2	Series transformer turns ration	1:1
3	DC link voltage	400V
4	Filter Inductance	1mH
5	Filter capacitance	10μF
6	Load resistance	0.01/phase
7	Load inductance	0.0024/phase

1) Three phase to ground fault

The figure 7(a) shows voltage sag occurs on source at 0.1sec due to three phase to ground fault and it is kept 0.2s, with total sag duration of 0.1s.Figure 7 (b) and 7 (d) shows the voltage injected by DVR and corresponding load voltages with compensation

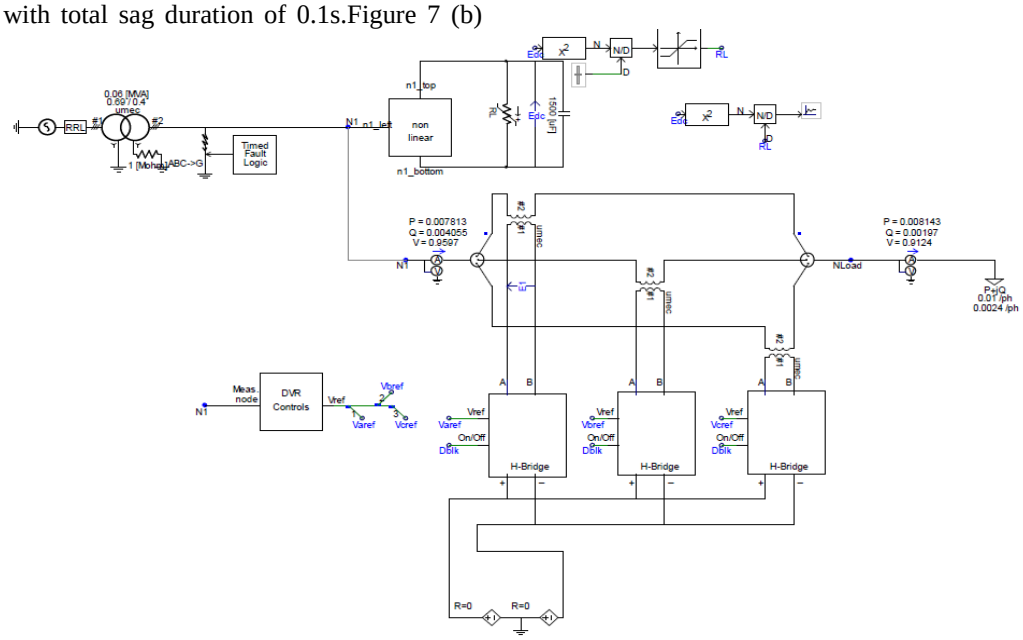

Fig 5 A PSCAD/EMTDC model of proposed H-Bridge converter based Dynamic voltage restorer (DVR)

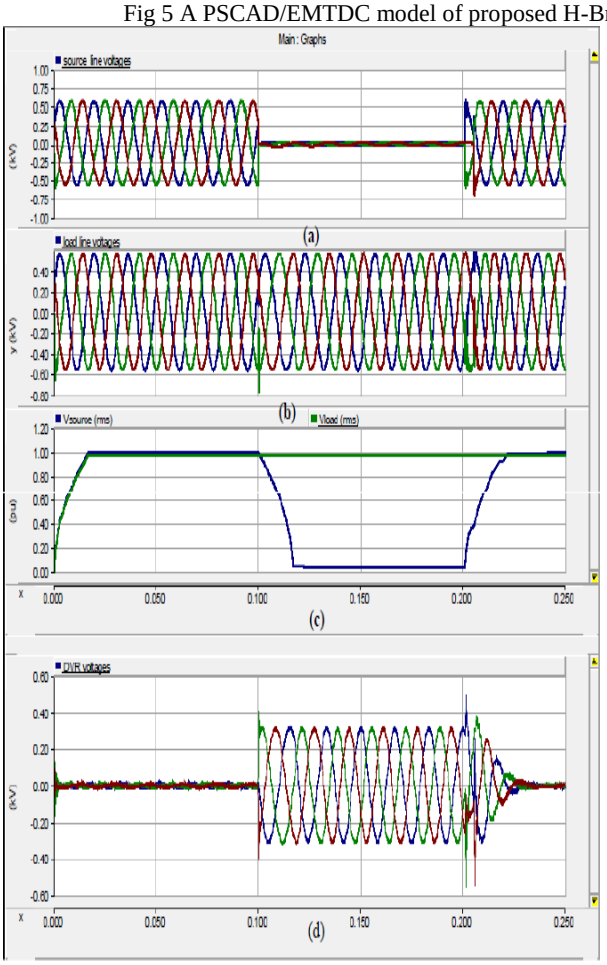

Fig 7(a) source line voltage s (b) load line voltages (c) rms voltages (d) DVR voltages

2) *Three phase fault*

The figure 8(a) shows voltage sag occurs on source at 0.1sec due to three phase to ground fault and it is kept 0.2s, with total sag duration of 0.1s.Figure 8 (b) and 8 (d) shows the voltage injected by DVR and corresponding load voltages with compensation

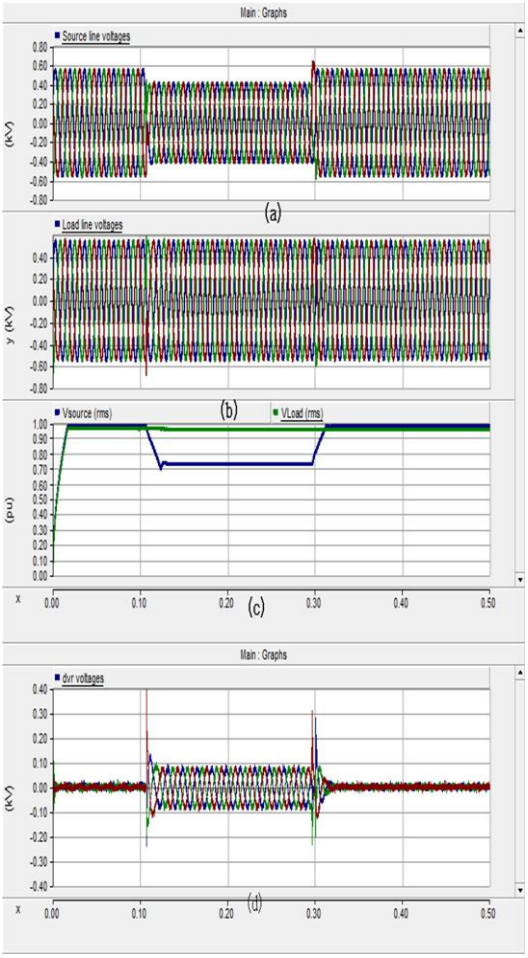

Fig 8(a) source line voltage s (b) load line voltages (c) rms voltages (d) DVR voltages

3) Double line fault

The figure 8(a) shows voltage unbalance occurs on source at 0.1sec due to Double line fault and it is kept 0.2s, with total sag duration of 0.1s.Figure 8 (b) and 8 (d) shows the voltage injected by DVR and corresponding load voltages with compensation.

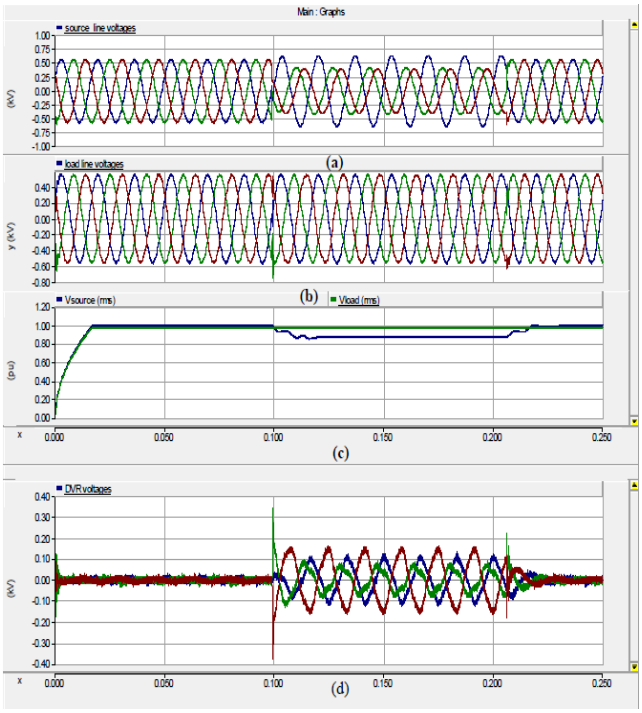

Fig 9 (a) source line voltage s (b) load line voltages (c) rms Voltages (d) DVR voltages

4) *Double line ground fault*

The figure 10(a) shows voltage unbalance occurs on source at 0.1sec due to Double line fault and it is kept 0.2s, with total sag duration of 0.1s.Figure 10 (b) and 10 (d) shows the voltage injected by DVR and corresponding load voltages with compensation.

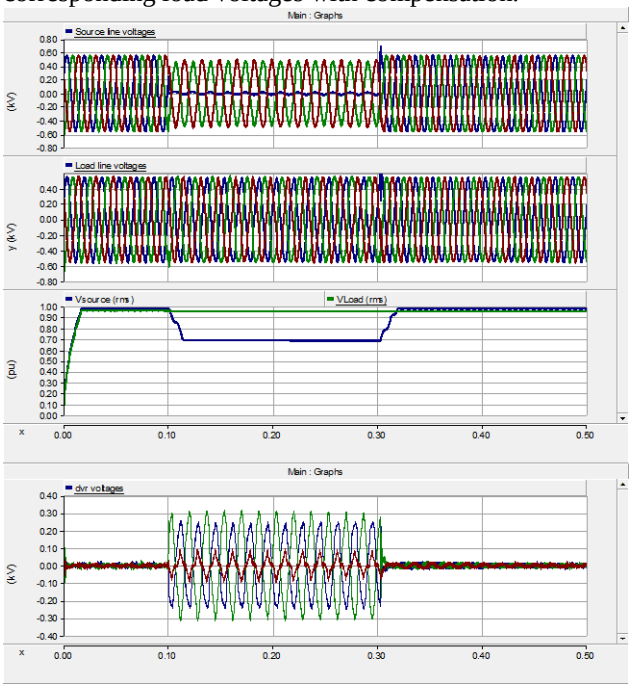

Fig 10(a) source line voltage s (b) load line voltages (c) rms voltages (d) DVR voltages

V.CONCLUSION

In this work, test system is developed using PSCAD/EMTDC software .This paper presents the features of DVR using converter with H-Bridges. H-Bridge cascaded converters avoid unequal device rating and unbalanced dc link voltage problems, in addition with power quality problems. The modeling and simulation of the proposed DVR using PSCAD/EMTDC had been presented. The simulation results shows that H-Bridge converter is protect the sensitive load form non liner voltage disturbances, Voltage sag & swell, and Voltage unbalance. The control system is modeled in the synchronous reference frame accounting for positive and negative sequence voltage sags to be mitigated. The DVR handles both balanced and unbalanced situations with sufficient efficiency and accuracy and injects the appropriate voltage component to correct rapidly any deviation in the supply voltage to keep the load voltage constant at the nominal value.

The main advantages of the proposed DVR are simple and efficient adaptive control and fast response. Future works will include a comparison with a laboratory experiments on a low voltage DVR in order to compare simulation and experimental results and estimate the cost of the practical system.

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