ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 4, April 2015

A Review Article On Design Techniques for Low Power Consumption in a Storage Element

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ABSTRACT: Now a day, There has been increasing demand for high speed digital circuits at low power consumption. The increasing importance of low power consumption is due to ever decreasing the feature size of microelectronic circuits. Low power device design is now a vital field of Research due to increase the demand of portable devices .In this paper an approach is presented For minimizing the power consumption for digital system. This paper gives an overview of minimizing the power consumption in a digital storage elements, like FlipFlops,Latches etc.Flip Flops are basic storage elements in digital circuits .In this paper some techniques is discussed for low power consumption in a storage element. The Techniques are as, GDI(Gate diffusion input) Technique and Modified GDI Technique. The low power techniques that are presented have been applied to design of low power digital storage elements.

KEYWORDS: A Storage element, GDI ,Modified GDI Technology, Low power

I. INTRODUCTION

The increasing trend of portable hand held electronic devices have set a goal of high performance computing with lower energy consumption. The focus of the designer is to achieve best possible tradeoff between power and delay for a circuit. In digital circuit design power consumption is a major concern for the past several years .The storage elements are major power consuming component. The power reduction of storage element leads to reduction of global power consumption of the system.So the Flip flops are the main storage elements of the digital system .The performance of the flip flop is an important parameter to determine the performance of the overall design. They have large impact on the circuit speed and power consumption. Therefore the study on flip flops has become quite significant in recent years. In this paper we proposed a few techniques to design a storage elements with less transistor count and less power consumption. The Techniques are as, GDI Technique and Modified GDI technique. By using these techniques we reduced the transistor count and less power delay product than other conventional methods. The factors which are desirable in storage elements are as like, High speed, low power consumption Noise stability, Smaller area, low glitch probability etc.

II. RELATED WORK

In [1] The authors has introduced a new technique of low power digital circuit design that is GDI(Gate diffusion input) technique which allows reducing power consumption, propogation delay and area of the digital circuit.In this transistor count is reduced by 40% and power dissipation is reduced by 21% to 36% than other conventional methods. [2] Authors have designed an efficient D Flip flop using GDI technique. This DFF design allows reducing power delay product and area of the circuit.[3]in this they proposed a novel low power flip flop circuit.they design the flip flop circuit in two cases single edge triggered or double edge triggered to overcome the problem of poer dissipation and it shows that the circuit has better speed than other conventional methods.[4]In this author have designed a low energy double edge triggered flip flop using a new technique that is clock branch sharing scheme to reduce the number of clocked transistors. As compared to the other d flip flop designs , this new technique has an improvement of 20% in

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power consumption.[5] Author has proposed two flip flop architectures for used in sub threshold region. In this both cells integrate a Gate diffusion input multiplexer in their designs to minimize the area and capacitance. [6] The DET topologies implemented in this work are transmission gate latch mux, symmetric pulse generator FF,static pulsed latch and conditional discharge ff are implemented using DSM technology.it produces the minimal power delay product.The proposed DET topology is a better solution for reducing clock and minize the overall power consumption of the circuit.[7] In this to reduce the redundant transistors at internal nodes of the flip flops a conditional clock technique is presented,then conditional clock pulse based Flip Flop designed.in this power saving is more than 50% when the activity factor os 10% .[8]In this various flip flop design like,Ep-DCO, ACFF, conditional pulse enhancement scheme,signal feed through scheme are designed for low power and area efficient.According to the results signal feed trough scheme is much area eefficient than others.

III. POWER DISSIPATION IN CMOS CIRCUIT

CMOS Technology provides better results than TTL(Transistor- Transistor Logic).But today due to increasing prominence of portable systems like laptops ,speed and low power design are major issues in high performance digital system. Hence two parameters affect the CMOS design:

- Power dissipation
- Delay in CMOS circuits

The average power dissipation in CMOS circuits can be expressed as the some of three main components. Those are as follows:

- Static Power dissipation
- Dynamic power dissipation
- Short circuit power dissipation

2.1:- Static Power Dissipation:- Static power dissipation within CMOS citcuit is due to lekage current between gate and substrate and current between drain and source.The reverse diode lekage occurs when the p-n junction between the drain and the bulk of the transistor is reversly biased.The reverse biased drain junction then conducts a reverse saturation current which is eventually drawn from the power supply Then the reverse potential difference between the nmos drain region and the p type substrate causes a reverse lekage current which is also drawn from the power supply So the static power dissipation is given by:

$$P_s = I_{rev} . \text{supply voltage} . n$$

2.2:- Dynamic Power Dissioation:- In CMOS circuits dynamic power is dissipated when energy is drawn from the power supply to charge up the output node capacitance.The output capictance of the gate consists mainly of the junction parasitic capacitances , which are due to the drain diffusion regions of the MOS transistors in the circuit. The dynamic power of acmos circuit is calculated as:

$$P_{dyn} = C_L . V_{DD}^2 . a . f$$

Where "f" is the operating frequency of the CMOS circuits,"V_{DD}" is the supply voltage of the circuit, "a" is the switching activity of the CMOS gate and C_L is the average gate load capacitance .

2.3:- Short Circuit Power Dissipation: - The final and smallest component of CMOS power is short circuit dissipation during CMOS transition. Since nmos and pmos circuits will typically have different switching times ,there may be a small period when both transistor may be on for a small period of time this situation creates a short circuit between V_{DD} and GND.The current component which passes through both the nmos and pmos devices during switching

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does not contribute to the charging of the capacitances in the circuit, and hence, it is called the short circuit currebt component:

$$P_{SC}=I_{mean}.V_{DD}$$

IV. LOW POWER DESIGN TECHNIQUES

3.1:- GDI(Gate diffusion input) technique :- Gate diffusion input design technique was introduced as a promising alternative to complementary CMOS logic design.The GDI method allow the implementation of a wide range of complex logic functions using only two transistors. It is anovel technique for low power digital circuit design. This technique reduces the power dissipation , propogation delay and area of the digital circuits.The GDI method is based on the use of a simple cell as shown in figure.1.

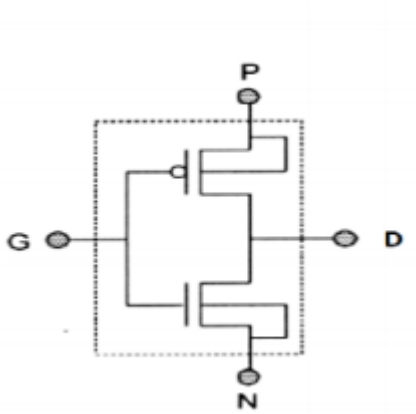

Fig.1. Basic GDI Cell

It contains four terminals, G node ,P node, N node are inputs and D node is output. G node is the common gate input of PMOS and NMOS. P node is the outer diffusion node of PMOS. N node is the outer diffusion node of NMOS. D node is common diffusion of both transistors. P,N,D may be used as a input or output according to the structure requirements.In this it should be noted that the source of PMOS in GDI cell is not connected to VDD or source of NMOS is not connected to GND . This feature gives the GDI cell two extra input pins to use and make the GDI design more flexible than conventional methods.

There are some logical functions that can be implemented by using GDI cell as shown in Table.1.

N	P	G	D	FUNCTION
'0'	B	A	A*B	F1
B	1	A	A+B	F2
'1'	B	A	A+B	OR
B	O	A	AB	AND
C	B	A	AB+AC	MUX
'0'	1	A	A	NOT

Table.1. basic Functions using GDI Cell

It can be seen that large number of functions can be implemented by using GDI cell .Many functions can be implement efficiently by GDI with less transistor count.GDI technique is called Gate diffusion Technique because in this one or more inputs are directly diffused into the gates of Transistors of N type and P type.GDI technique is much efficient than other methods .

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3.2:- Modified GDI(Gate diffusion input) Technique :- Power dissipation becomes the major problem in the design of high performance applications. So power reduction and performance boosting techniques are of profound importance for system development and success. Morgenshtein et. all. Investigated a high speed and multipurpose logic style for low power design .known as GDI(Gate diffusion input) with less power dissipation, reduced area and efficient implementation of broad Varity of logic functions. But the basic GDI technique suffers from some practical limitations. This limitations can be overcome by Modified GDI technique.This technique allows reducing power consumption ,delay and area of the digital circuits.The Modified GDI cell shown in figure .2.

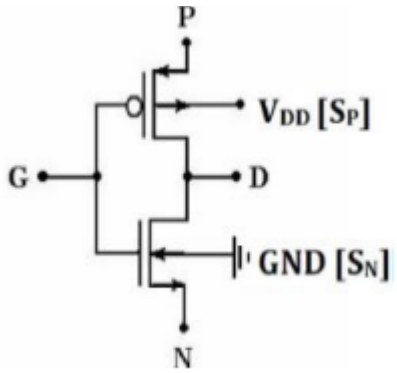

Fig.2. Modified GDI Cell

In contrast with basic GDI cell, Modified Gdi cell Contains

- A low voltage terminal S_P
- A high voltage terminal S_N

S_P is configured to connect with high constant voltage and S_N configured to connect with low constant voltage. With help of modified GDI cell various logic functions can be implemented that are as shown in Table.2.

N	S_N	P	S_P	G	D	FUNCTIONS
O	0	1	1	A	A'	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A'	0	A	1	B	A'B+AB'	XOR
A	0	A'	1	B	AB+A'B'	XNOR
0	0	B	B	A	A'B	FUNCTION 1
B	0	1	1	A	A'+B	FUNCTION 2
C	0	B	1	A	A'B+AC	MUX

Table.2. logic functions implemented by using Modified GDI cell

The Modified GDI technique provides a low power and area efficient substitute to existing logic styles .It is much better for design high speed, low power circuits using reduced number of transistors even as improving swing degradation and static power characteristics. Modified GDI is useful for design of a broad range of logic circuits. So that the Modified GDI circuits design methods is therefore a promising new approach to logic circuit design.

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So for designing of a storage element as like flip flops with less power consumption, GDI and Modified GDI is much better than other conventional methods. Minimum power and less delay produced by sizing, so if transistor count is less then size is also small and power will be less consumed.

V. CONCLUSION

In high performance applications less power consumption, area and less delay by the device are the main technological aspects to prefer a design over the other contending designs. Thus the design of a storage element with GDI Technique and Modified GDI technique is much better than other conventional methods. By using these techniques power consumption is less and transistors count is also reduced. These design techniques are suitable for portable applications, as it is more area and power efficient.

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