A Simplified Space Vector Pulse Width Modulation Method For Cascaded H-Bridge Multilevel Inverters

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ABSTRACT: A major advancement in the research area of space vector pulse width modulation (SVPWM) in recent years is the introduction of the nearest three vector algorithm computational intensity is still a drawback of SVPWM methods in real time applications, especially in the case of multilevel inverter operation. To solve the problem of computational complexity in multilevel inverters due to the large number of space vectors and redundant switching states, a simple space vector PWM method is proposed. Based on this method, the location of the reference voltage vector can be easily determined and the calculation of dwell times becomes very simple. More importantly, the proposed method is general and can be directly applied to the cascaded H-bridge inverter of any voltage levels. This proposed method is tested for seven level and nine level cascaded H-Bridge inverter drive system and the simulated results were presented.

KEYWORDS: Multi-level inverter, SVPWM, redundant states, THD, Cascaded H-Bridge inverter SVPWM.

I. INTRODUCTION

The Multilevel inverters is promising power electronics topology for high power high voltage applications. Because of its low electromagnetic induction and high efficiency [1]. These inverters can solve the problem associated with traditional two level inverters. Their topologies including diode clamped , flying capacitor and cascaded H-bridge structures are intensely studied for high power applications .The cascaded inverters topology has several advantages that have made it attractive in power conditioning systems and medium and high power drive applications. The first advantage is ease of regulation of DC bus .The second advantage is modularity of control can be achieved unlike diode clamped and capacitor clamped inverters where individual phase legs must be modulated by central controller. Large number of states offered by multi level converters can impose massive computational overhead if not carefully optimized .Among all the switching algorithms [4- 6]space vector modulation seems most promising since it offers a great flexibility in optimizing switching pattern design and also well suited for digital implementation. The space vector modulation for more than three level inverter is very complex due to large number of space vectors and redundant switching states and calculation of dwell times is also complicated [5]. A simplified space vector algorithm is proposed in this paper where the location of reference voltage vectors and calculation of dwell times is simplified with minimum voltage harmonic content .For a particular reference voltage it is easy to determine all the redundant switching states and determine the status of switching states whether it is large, small or medium and automatically generates that pattern which need not require any look-up table, hence minimizing the memory requirement and complexity. And can be applied to high level cascaded H – bridge inverters.

II. CASCADED H-BRIDGE INVERTER

Cascaded H-bridge multilevel inverter has been used multiple units of H-bridge power cells connected in series to achieve medium voltage operation and low harmonic distortion. This inverter needs several DC sources to synthesize the output voltage waveform. The single H- Bridge can generate three-level output. When S11 and S21 are on, the output is +Vdci; when S31 and S41 are on, the output is −Vdci; when either pair S11 and S31 or S41 and S21 are on, the output is 0.In symmetric structure of cascaded H-bridge inverter which the DC voltage sources are equal, there are 2N+1 level in output of phase voltage where N is the number of DC voltage sources. The asymmetric input voltages when properly chosen eliminate redundant output levels and maximize the number of different levels generated by the

inverter. Therefore with fewer number of semi conductor switches this topology can achieve the same output voltage quality.The number of levels in phase voltage obtains as

$$V_{dc}i = 2^{(i-1)}E, \ i=1, 2….N \rightarrow n=2^{N+1} - 1 ………..1$$
$$V_{dc}i = 3^{(i-1)}E, \ i=1, 2….N \rightarrow n=3^N ……………….2$$

Where N is the number of DC voltage sources

 The optimal asymmetry has been obtained using voltage sources proportionally scaled to the two- or three- H-bridges.
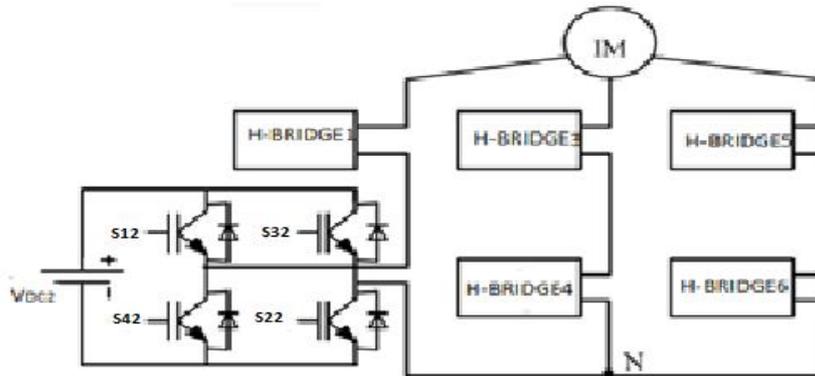

fig1: Nine Level cascaded Asymmetric H-bridge inverter

The various switching states for nine level inverter with inverter H bridge voltages E and 3E are summarizedin Table1.It is worth noting that the inverter phase voltage v_{AN}may not necessarily equal the load phase voltagev_{AO}, which is the voltage at node A with respect to the load neutral O. It can be observed from Table1 that some voltage levels can be obtained by more than one switching state.

Table1: Switch states of nine level cascaded H bridge inverter

v_{AN}	S_{11}	S_{31}	S_{12}	S_{32}	v_{H1}	v_{H2}
4E	1	0	1	0	E	3E
3E	1	1	1	0	0	3E
2E	0	1	1	0	−E	3E
E	1	0	0	0	E	0
0	0	0	0	0	0	0
−E	0	1	1	1	−E	0
−2E	1	0	0	1	E	−3E
−3E	0	0	0	1	0	-3E
−4E	0	1	0	1	−E	−3E

III. SPACE VECTOR MODULATION

The Cascaded H-Bridge uses multiple units of H-bridge sources connected in series to produce high AC output voltages. In the proposed algorithm space vector in $\alpha - \beta$ axis is decomposed in integer scale, which makes an angle of $\pi/3$, it is easy to find out coordinates of any space vectors. The location of the reference voltage vector and the dwell times of the space vectors can be calculated easily. For the 9-level inverter, there are 384 small triangles and the vertex of each triangle represents a space vector. The hexagonal vectors can be divided into six major triangular sectors (I to VI). Only the first sector of the coordinate is used because the vectors located in the other sectors can be transformed to first sector by clockwise rotating by an angle of $k*pi/3$, k =(1,2,3,4,5 for sector 2 to 6). As all the sectors are identical, only details of sector1is given.
Vertex of each triangle represented as space vector defined by

$$\overline{v} = v_{a}e^{j0} + v_{b}e^{2\pi/3} + v_{c}e^{4\pi/3}………......…3$$

V_a, V_b and V_c are phase voltages of
The co-ordinate of each vector in a Cartesian co-ordinate system V_x, V_y can be calculated as

$$V_x = V_a - (V_b + V_c)/2 ………...............…4$$

$$V_{\gamma} = \sqrt{3}(V_b - V_c)/2 \quad\text{……………..........5}$$

The co-ordinates of space vector with unity DC supply voltage (Vdc = 1 p.u). To reduce voltage harmonic distortion, the reference voltage V^* can be synthesized by nearest vector,Because of complexity involved in calculation of dwell lines and identification of triangle where the reference vector end point fall s Cartesian co-ordinate system can be transferred to 60^0 co-ordinate system.

$$V_{\alpha} = \cos\theta - V\sin\theta /\sqrt{3} \quad\text{……………...............6}$$
$$V_{\beta} = V\cos(60-\theta) - V\sin(60-\theta)/\sqrt{3} \quad\text{…..7}$$

Where V_{α} and V_{β} are the co-ordinates of a space vector in 60^0 co-ordinate system V and θ are length (amplitude) and phase angle respectively. The reference vector after decomposition into α and β (60^0 in axis)
For N+1 level inverter the component along α- β axis for reference vector can be written as

$$V_{ref}^{\alpha} = \left(2N.V_{ref}/3V_{dc}\right)\sin(60^0 - \theta) \quad\text{…………..8}$$
$$V_{ref}^{\beta} = \left(2N.V_{ref}/3V_{dc}\right)\sin\theta \quad\text{…………………..9}$$
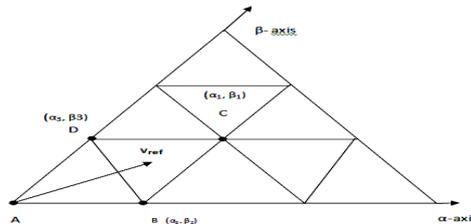
Where θ is the speed of rotation.

fig. 2 Decomposition of reference voltage in α-β axis

Any reference vector V_{ref} and θ lying in a rectangular area specified by ABCD.
However we can obtain rounded integer values (α, β)

$$\alpha = int(V_{ref}^{\alpha}) \quad\text{……………...............10}$$
$$\beta = int(V_{ref}^{\beta}) \quad\text{……………...............11}$$

These α, β are defined by vector (α, β) in α- β axis

$$\text{If } (V_{ref}^{\alpha} + V_{ref}^{\beta}) <= (\alpha + \beta + 1)\text{………12}$$

The V_{ref} is located in ABD, otherwise BDC
If the corresponding three nearest space vectors are (α1, β1) and (α2, β2) and (α3, β3) then dwell times are calculated as

$$\alpha1 T1 + \alpha2 T2 + \alpha3 T3 = T \quad\text{…………….13}$$
$$\beta1 T1 + \beta2 T2 + \beta3 T3 = T\text{………………14}$$
$$T1 + T2 + T3 = T \quad\text{…...........................15}$$

Where T is PWM time period.
$(V_{ref}^{\alpha} + V_{ref}^{\beta}) > N$ for N+1,it becomes over modulation, then this situation is handled by multiplying regional vector V_{ref}^{α}, V_{ref}^{β} by $\frac{N}{(V_{ref}^{\alpha} + V_{ref}^{\beta})}$ and consequent steps are followed.For higher voltage level inverters, the number of redundant switching states also increases. For the CHB multi-level inverter, the general expression which describe the relationship between space vector and their corresponding switching states are given by

$$S_a = \alpha + \beta - m, \alpha + \beta - m + 1, \dots m \quad\text{……16}$$
$$S_b = S_a - \alpha \quad\text{…………...........................…17}$$
$$S_c = S_b - \alpha\text{-}\beta \quad\text{…...............................18}$$

Where $\alpha, \beta = 1, 2, 3\dots\dots2m$ and m$=\frac{n-1}{2}$; for n-level inverter.

The number of redundancy of each space vector for n-level inverter is equal to n- $(\alpha + \beta)$ and the number of redundancy is even or odd if $\alpha + \beta$ is even or odd respectively.To minimize the total number of switching transients and to optimize the harmonic profile of the output voltage, small and large states are applied for even number redundancy and medium is applied for odd number redundancy.
For space vectors (α, β)

$$S_L = (\frac{\alpha+\beta}{2} + \frac{1}{2}, \frac{\beta-\alpha}{2} + \frac{1}{2}, -\frac{\alpha+\beta}{2} + \frac{1}{2})\text{……....19}$$

$$S_M = (\frac{\alpha+\beta}{2}, \frac{\beta-\alpha}{2}, -\frac{\alpha+\beta}{2})\ldots\ldots\ldots\ldots\ldots........20$$

$$S_S = (\frac{\alpha+\beta}{2} - \frac{1}{2}, \frac{\beta-\alpha}{2} - \frac{1}{2}, \frac{\alpha+\beta}{2} - \frac{1}{2})\ldots\ldots\ldots.21$$

Where S_L, S_M and S_S are small, medium and large states.
The switching states in other sectors (II to VI) can be obtained as,

Table-2 switching states of phase a,b and c

Sector	S_a	S_b	S_c
I	S_a	S_b	S_c
II	$-S_b$	$-S_c$	$-S_a$
III	S_c	S_a	S_b
IV	$-S_a$	$-S_b$	$-S_c$
V	S_b	S_c	S_a
VI	$-S_c$	$-S_a$	$-S_b$

In multilevel inverter, the redundant states increase with the voltage level. For example seven and nine level inverters have .The redundant states of six and eight respectively for zero voltage vector. This redundancy is employed to minimize voltage harmonic distortion. The switching sequence design is selected to meet the requirements such as minimization of number of switching's per sampling period and one voltage level change for commutation of switch and adoption of large small and medium states. The corresponding sequence design is given in Table-3 for the next half the sequences are employed from last to first.

Table-3 switching sequence design for half cycle

	TRIANGLE	SWITCHING SEQUENCES
ODD	ABD	$S_{SA} \rightarrow S_{MB} \rightarrow S_{MD} \rightarrow S_{LA}$
	BDC	$S_{SC} \rightarrow S_{MB} \rightarrow S_{MD} \rightarrow S_{LC}$
EVEN	*ABD*	$S_{LB} \rightarrow S_{MA} \rightarrow S_{SD} \rightarrow S_{SB}$ OR $S_{LD} \rightarrow S_{LB} \rightarrow S_{MA} \rightarrow S_{SD}$
	BDC	$S_{LB} \rightarrow S_{MC} \rightarrow S_{SD} \rightarrow S_{SB}$ OR $S_{LD} \rightarrow S_{LB} \rightarrow S_{MC} \rightarrow S_{SD}$

For the next half the sequences are employed from last to first.

IV. RESULT AND DISCUSSION

The simulation results corresponding to m_a =0.8 for seven and nine level inverter are shown .The output voltage is compatible with load The Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm; Stator Resistance and Inductance: 0.01965 p. u. and 0.0397 p. u.; Rotor Resistance and Inductance: 0.0109 p. u. and 0.0397 p. u. with Mutual Inductance: 1.359 p. u., Sampling time Ts=10e-6 sec. This method features easy implementation and more importantly, minimum harmonic content in the inverter output voltage and current of the Induction Motor Load. For seven level output the current THD is 1.24% and the Line voltage THD is 9.32%where as . For nine level the current THD reduces, which is 0.66%and line voltage THD is 6.02%. As different voltages can be obtained by simply changing the modulation index (m_a). So, the results are shown as follows.
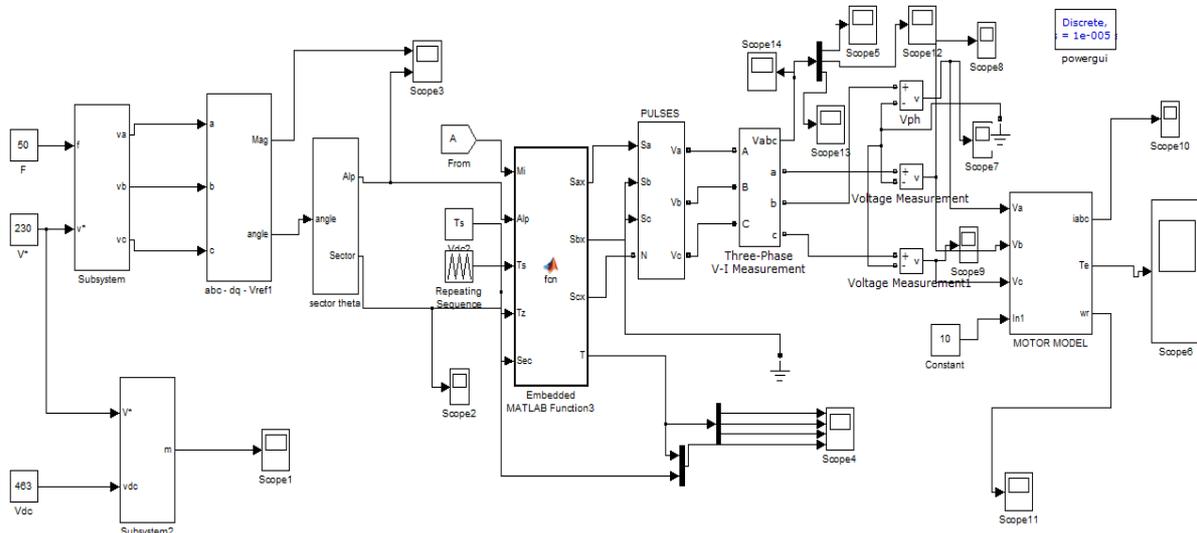
Fig. 3 Simulink model for Asymmetric nine level cascade H-bridge inverter.

In Fig 3 , it shows the Simulink model of nine level asymmetric Cascaded H bridge inverter with input dc voltages as 100V and 300V corresponding to m_a =0.8 with Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm
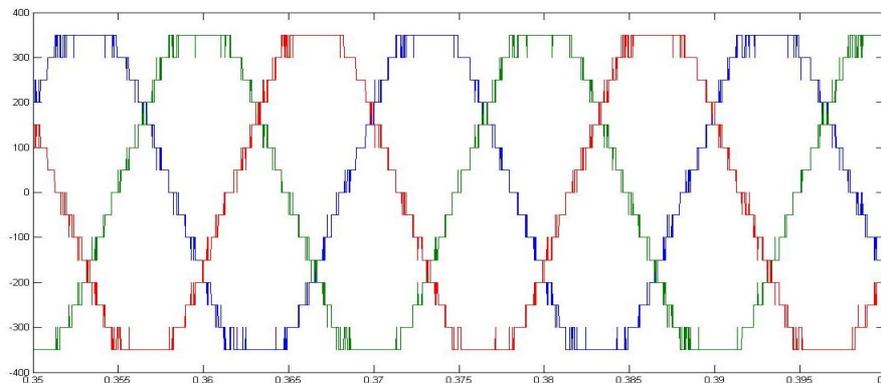

Fig. 4 Three phase output line voltages of nine level Cascaded H bridge inverter

In Fig 4 , it shows the output line voltages of nine level Cascaded H bridge inverter corresponding to m_a =0.8 with Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm
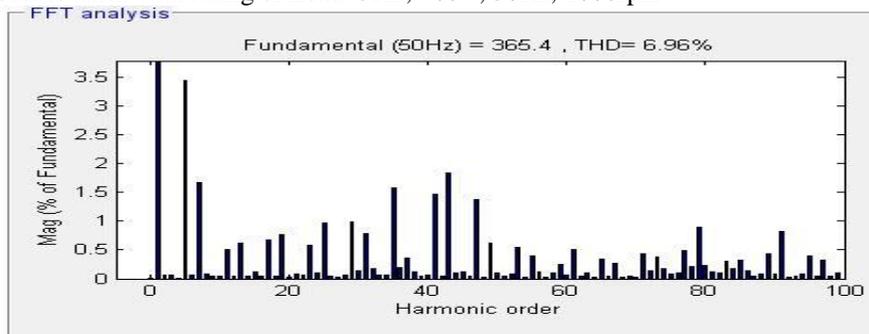
Fig .5 THD of output Line voltage of seven level cascaded H bridge inverter

In Fig 5 , it shows the output line voltages THD of nine level Cascaded H bridge inverter corresponding to m_a =0.8which is 6.96 with Induction Motor Load
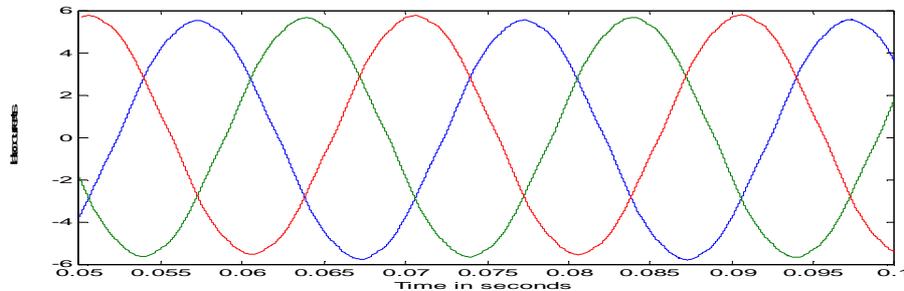

Fig.6 Three phase output line currents of nine level Cascaded H bridge inverter.

In Fig 6 , it shows the output line currents of nine level Cascaded H bridge inverter corresponding to m_a =0.8 withInduction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpmthe current THD reduces, which is 0.66%.
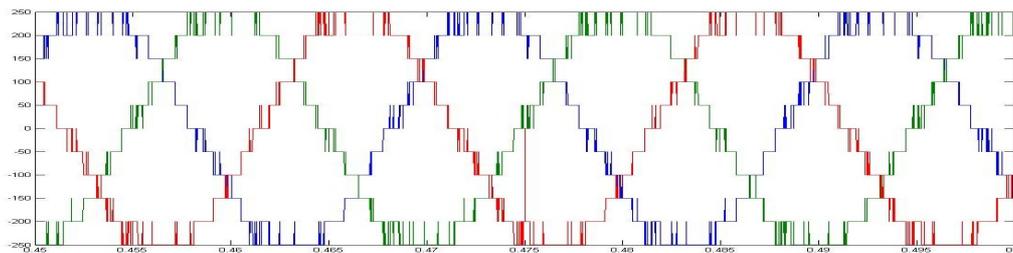

Fig. 7 Three phase output line voltages of seven level Cascaded H bridge inverter.

In Fig 7 , it shows the output line voltages of seven level Cascaded H bridge inverter corresponding to m_a =0.8 with Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm
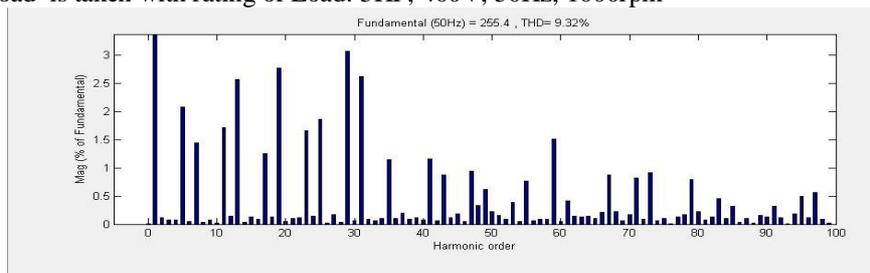

Fig.8 THD of output Line voltage of seven level cascaded H bridge inverter

In Fig 8 , it shows the output line voltages THD of seven level Cascaded H bridge inverter corresponding to m_a =0.8which is 9.32 with Induction Motor Load
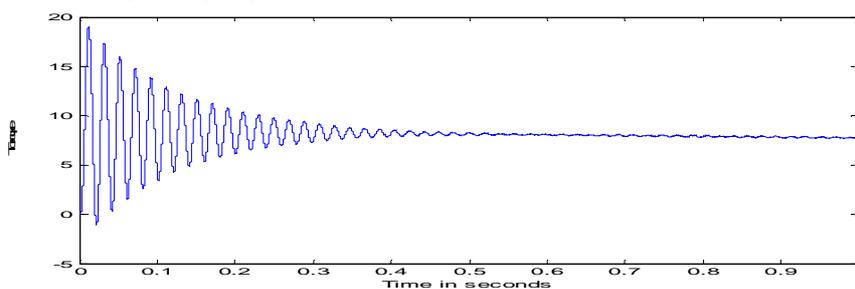

Fig .9 Torque output of seven level Cascaded H bridge inverter

Fig .9 shows the Torque output of seven level Cascaded H bridge inverter. The Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm; Stator Resistance and Inductance: 0.01965 p. u. and 0.0397 p. u.; Rotor Resistance and Inductance: 0.0109 p. u. and 0.0397 p. u. with Mutual Inductance: 1.359 p. u., Sampling time Ts=10e-6 sec.
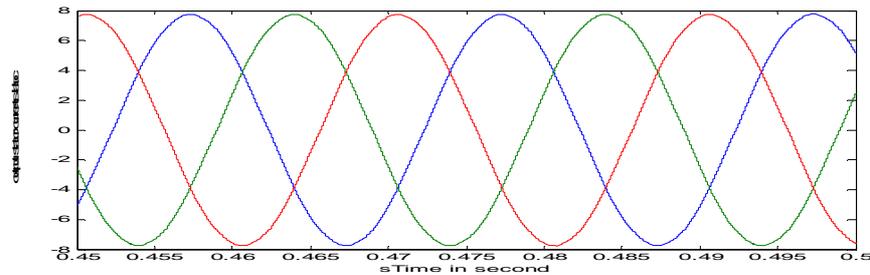

Fig .10 Three phase output line currents of nine level Cascaded H bridge inverter.

Fig .10 shows the Torque output of seven level Cascaded H bridge inverter. The Induction Motor Load is taken with rating of Load: 5HP, 400V, 50Hz, 1000rpm; Stator Resistance and Inductance: 0.01965 p. u. and 0.0397 p. u.; Rotor Resistance and Inductance: 0.0109 p. u. and 0.0397 p. u. with Mutual Inductance: 1.359 p. u., Sampling time Ts=10e-6 sec.
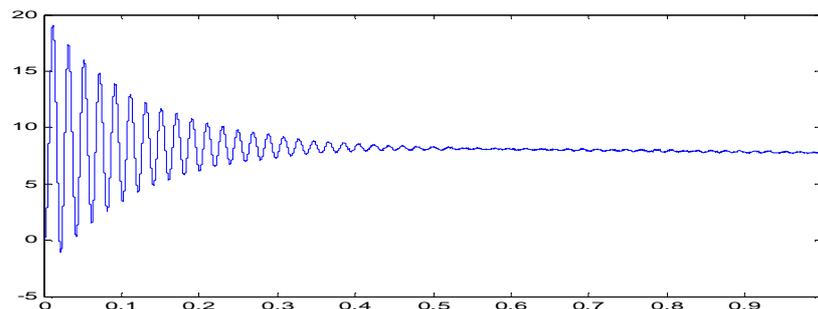

Fig. 11 Torque output of nine level Cascaded H bridge inverter

VI.CONCLUSION

The proposed Space Vector Pulse Width Modulation method simplifies the calculation of space vectors and their corresponding dwell times to facilitate the design and digital implementation .All the space vectors are transformed to 60° co-ordinate system .This algorithm features automatic switching pattern generation with minimum harmonic content in the inverter output voltage and current of induction motor load. This algorithm is verified for five, seven, nine level cascaded H bridge inverter through MATLAB/SIMULINK simulations.

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