ISSN: 2319-8753

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 5, May 2014

A Study of Butterworth Filter Based on Operational Transconductance Amplifier

RenuSahu[1], Zoonubiya Ali[2], BalramTimande[3]

P.G. Student, Department of Electronics and Telecommunication, DishaInstitute of Management and Technology, Raipur, Chhattisgarh, India[1]
Assistant Professor, Department of Electronics and Telecommunication, Disha Institute of Management and Technology, Raipur, Chhattisgarh, India[2]
Head, Department of Electronics and Telecommunication, Disha Institute of Management and Technology, Raipur, Chhattisgarh, India[3]

Abstract-This study presents different structure of operational transconductance amplifier (OTA) which is an integral part of continuous time channel selection filter. It was observed that to enhance the linearity and to reduce the third order harmonic distortion, linearity schemes are used however most of those techniques present important drawback such as reduced effective transconductance, significant power consumption, limited frequency response, increased noise level. It presents new linearity scheme source degeneration and auxiliary differential pair technique by which the linearity can be increased without sacrificing other important parameters such as noise level, power efficiency and frequency response which is better than other schemes.

Keywords-CMOS analog circuits, operational transconductance amplifier (OTA), direct conversion receiver, transconductor, linearity schemes, continuous time filters.

I. INTRODUCTION

High-performance filter is one the most important building block in analog domain for several applications such as read/write channels for hard-disk drivers, intermediate-frequency (IF) filtering for high speed wireless and wired communication systems and adaptive systems as reported in [1]-[12]. In receivers, before the subsequent analog to digital conversion stage, very demanding high performance analogue filters are typically used to block interferers and provide anti alias filtering. Sun Y. et al[13] reported that to design analogue filters with low power consumption and wide tuning range is very challenging.

A. Filter Basics

Filter is defined as the electric network which passes or allows unattenuated transmission of electric signal within certain frequency range and stops or disallows transmission of electric signal outside this range.

B. Types of filter

LacanetteetKerry al [14] presented the filters categorization based on the signals used, based on the components used, based on the frequency response and based on the mathematical functions. All these categorize are divided into subcategory. Signals based filters are divided into digital filters and analog filters, component based filters are divided into switched capacitor filters and active filters, frequency response based filters divided into low pass filters, high pass filters, band pass filters, band stop filters, all pass filters, mathematical functions based filters divided into Butterworth filters, Chebyshev filters and elliptic filters.

Gratz Achimet al [15] mentioned that the operational transconductance amplifier(OTA) has differential input voltage which produces an output current. Thus, it is a voltage controlled current source (VCCS). Also Geiger R. L. et al [16] presented basic structures using the transconductance amplifier.

For direct conversion receiver (DCR) application, wireless applications Butterworth, Elliptic and Chebyshev filters are mostly used.The main objective of this paper is to study the different order Butterworth filter. Also a design technique is presented to enhance the Butterworth filter performance based on OTA.

II. BUTTERWORTH FILTER

Butterworth filter is suitable for applications in which any ripples are intolerable and also have a monotonic amplitude frequency response. Butterworth filter is characterized by having a maximally flat magnitude response for this reason; the Butterworth filter is also called a “maximally-flat magnitude” filters. The equation for Butterworth filter’s magnitude response is shown in fig 1

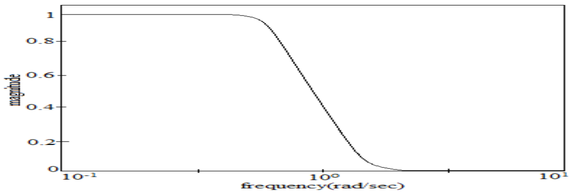


Fig. 1.Butterworth filter response

$$H(\omega) = \frac{1}{1+(\frac{\omega}{\omega_0})^{2n}} \qquad (1)$$

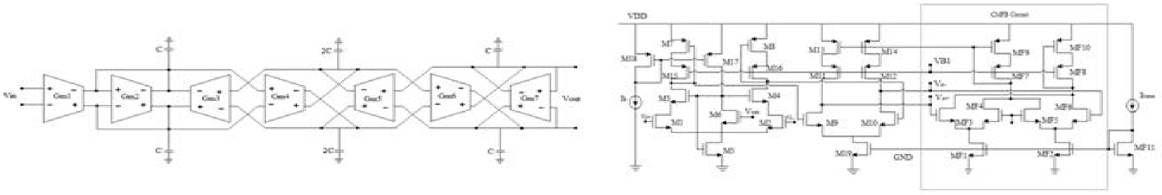
Where n is the order of filter and ω_0 is the 3 dB frequency. The response of Butterworth filter is monotonic, decreasing smoothly from $\Omega = 0$ to $\Omega = \infty$

$$|H(j\Omega)| = \sqrt{1/2} \text{ at } \Omega = 1 \qquad (2)$$

III. FILTER ARCHITECTURE

For the implementation of the filter the Gm-C approach [16] has been chosen because of the easy tuning capability by varying the Gm value of the transconductor. The Gm-C filter has a low noise floor but the ability to handle large signal is limited. Inorder to archive the required value in terms of the linearity, the $G_m$value which depends on the width, length and the bias current of the CMOS transistor has to be chosen carefully.The transconductor structure isdifferent for different applications are as follows

A. Third order Butterworth filter



(a)

(b)

Fig. 2.(a) Implementation of third order Butterworth filter, (b) Implementation of transconductor with the CMFB circuit

As shown in fig 2(a) the third-order Butterworth low-pass G_m–C filter, which consistsof seven identical transconductor, The cutoff frequency of this filter is tuned by changing the bias current I_{tune}. In this filter three CMFB circuits are used to block common mode voltage as shown in fig 2(b)

The performance of the common-mode control topology can be maintained by changing the bias current of CMFB circuit according to I_{tune} value.

a) OTA structure for 3rd order filter

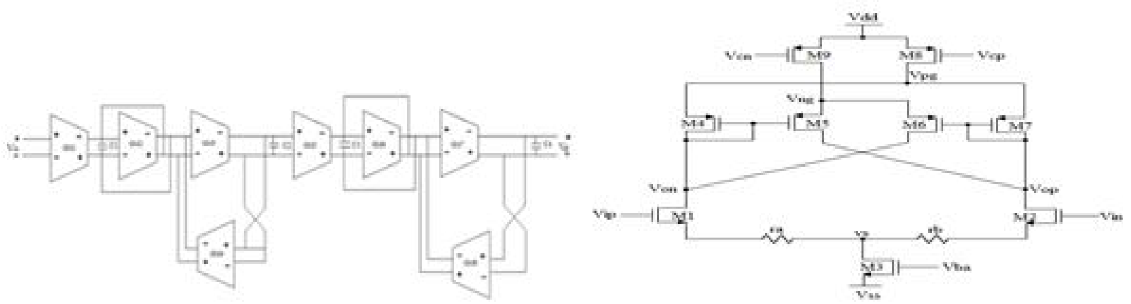
The voltage-to-current (OTA) circuit as shown in fig 2(b) is based on flipped follower circuit (FLF) [17], which is composed by transistors M5 and M6. M1 and M2 transistor provides voltage to current conversion. The gate voltage of transistor M5 is used to provide a bias voltage for transistors M3 and M4, and ensure the linear region operation of transistors M1 and M2. Thus, the drain voltage of transistors M1 and M2 would be kept to a constant value. Input transistors operate in linear region. Besides, the source of transistors M1 and M2 is fixed to a constant value owing to the FVF feedback loop. Low impedance is obtained at the source of transistor M6.The structure suppresses the variation at the source of transistors M1 and M2, and thus the circuit would operate under a class-AB fashion. A common mode feedback (CMFB) circuit is required to control the output common-mode voltage. The output voltage of the transconductor is sensed by transistor MF3 and MF6, and then compared with a reference voltage, which is equal to the input common-mode voltage this input voltage owing to the cascade design of the filter structure. If common mode voltage is not equal to the reference voltage, a corrected current is mirrored by transistor MF9 to the load of the Transconductor, then the output $V_{cm}$is adjusted to the desired voltage. The aspect ratio of transistor M19 would be twice the value of transistors MF1 and MF2.This filter was simulated using 0.18µm CMOS technology provides tuning range 135 KHz - 2.2 MHz consuming power of 1.57 mw - 1.9mw.

B.Fourth Order Butterworth Filter

The fully differential transconductor-capacitor filter is shown in fig 3(a) by using two biquadratic sections fourth-order Butterworth is realized. Each biquad is implemented with 4 OTAs and 2 capacitors. The fully differential transconductor filter is shown in fig 3 (b) [18]a common mode feedback circuit (CMFB) is needed due to the fully differential circuit to set the DC output level of the filter. By varying the current through theOTAs in a range of 1:10 a tuning range of the corner frequency of about 1:3 can be achieved.

a) OTA structure for 4th order filter

In Fig. 3(b) the differential transconductance circuit is comprises a cross-coupled high-impedance load and a source-Coupled pair with poly-silicon degeneration resistors.The linearity is enhanced by the degenerated resistors at the cost of a smaller effective transconductanceG_m and a smaller tunable Gm range. Transistors M8 and M9 operate in the triode region, acting as degeneration resistors to provide different operating points at nodes v_{pg} and v_{ng} and transistors M4, M5, M6 and M7 are matched. M4 and M7 act like a pair of positive resistors R+, while M5 and M6 function as negative resistors R-. The output impedance of the transconductor depends on the parallel combination of R+ and R-, which are controlled by voltages v_{cp} and v_{cn} respectively. As a result, the output impedance, and therefore, the Q of the integrator, can be maximized with proper combinations of v_{cp} and v_{cn}. With this transconductor, a tunable integrator for very-high-frequency integrated filters can be realized by adjusting the voltage v_{ba}, which controls the tail current, and thus, Gm. Good high-speed properties stem from the absence of internal high impedance nodes, which, pushes non-dominant poles to the gigahertz ranges [18]. This filter was designed in 0.18µm CMOS technology provides tuning range from 1.4 MHz – 16 MHz



(a) (b)

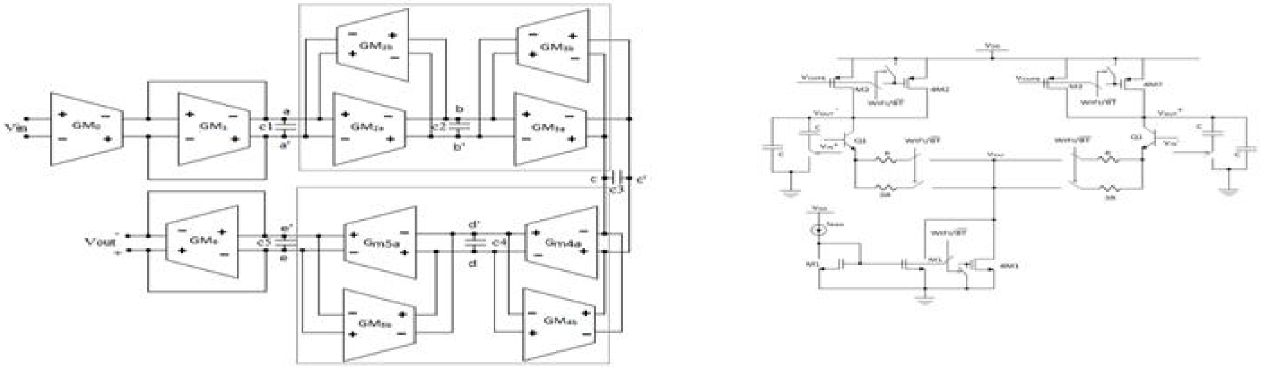
Fig. 3.(a) Implementation of 4th order Butterworth filter, (b) Fully differential OTA implementation

C. Fifth Order Butterworth Filter

The fifth-order OTA-C filter is shown in fig 4(a) [19]the overall circuit is composed of two gyrators A and B, which implement the equivalent inductors $L_2$and L_4 respectively, two grounded resistors $G_{m0}$and G_{m6} and five capacitors C_1-C_5. Five common-mode feedback circuit shared by eleven OTA's reduces power consumption. The common mode feedback circuit provide sensing of common output voltages on nodes a to control the bias voltage v_{b3} of the OTA

a) OTA structure for 5th order filter

The OTA-C structure for 5th order lowpass filter shown in fig 4 (b) was implemented with the two cascaded biquadratic sections. The OTA used source degenerated transconductance with current scaling. It enhances the limited linear input range of the bipolar differential pair. This circuit was simulated in 0.25µm CMOS technology tunable from 600 KHz – 6 MHz with current consumption of 0.9 -2.7 µA.



(a) (b)

Fig.4. **(a)**Fifth order Butterworth filter implementation, (b)Implementation of dual-mode OTA

D. Six Order Butterworth Filter

In fig 5 shows the six order filter consists of two cascade third order complex lowpass filters. The third order complex lowpass filter isshown in Fig 6 (a) was constructed by coupling the two Butterworth low pass filters with the three gyrators which perform the linear frequency translation [20-22]. When the gyrators are turned off the filter works as two low pass filters and when the gyrators are active the filter works as a complex band pass filter. The bandwidth and center frequency of the third-order filter are given by two equations below

$$BW = \frac{g_m}{C} \tag{3}$$

$$f_c = \frac{g_{mc}}{C} \tag{4}$$

Where $g_m$is transconductor, BW is bandwidth and f_c is the center frequency.

a) OTA structure for 6th order filter

In fig 6(b) a widely continuously tunable OTA circuit is presented. To meet distortion, noise and power specifications differential pair is best choice. In this differential pair, there are Three groups of switches: {S50, S51….S5n}, {S30, S31. . . , S3n} and {S10, S11. . . , S1n}.which is used for transconductance tuning. The switching is realized by putting in parallel transistorsinserted by digitally controlled MOSFET switches. By this tuning scheme it is possible to keep the gate overdrive voltage of the input transistors constant and to make the transconductor tunable in a large range step by step. In this way no useless current is dissipated and the linearity performance remains constant. Fine tuning is realized by the bias reference current Iref_f is a stable reference current comes from the fine tuning module. Switches {S60. . . , S6m} are used to tune the bias current Iref_f which is passed to the transconductor's bias circuit in and then transconductance is tuned bit by bit. The coarse tuning and fine tuning are combined, making the transconductance continuously tunable in a large range without heavily sacrificing linearity and power performance. The CMFB circuit is tuned the same way as the transconductor to keep the CMFB loopstable. An automatic frequency tuning scheme is used to compensate for process variation [20] – [26]. In the OTA C filter shown in fig. 6(a) frequency tuning is achieved by tuning the transconductors with digital control signals.This filter was simulated in 0.18µm CMOS technology with tuning range 3 – 24 MHz

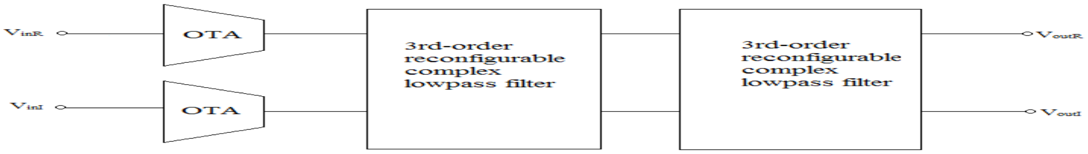
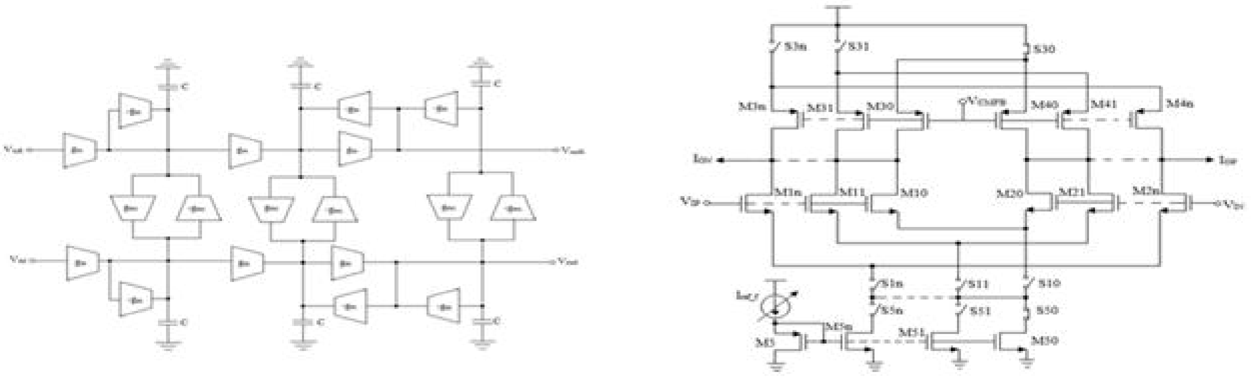


Fig.5.Block-diagram of six-order filter



(a) (b)

Fig.6. (a) Third order complex lowpass filter, (b) Widely Continuously Tunable OTA Circuit

IV. PROPOSED FILTER STRUCTURE

A circuit realization for the second order filter is used because of its advantages in design and layout. The topology of the fully differential circuit block is shown in fig 7(a) the transfer function of the above circuit structure is [27]

$$H(S) = \frac{V_{out}}{V_{in}} = \frac{\frac{g_{m2}g_{m3}g_{m4}}{g_{m4} \quad C_1C_2}}{S^2+\frac{g_{m2}}{C_1}S+\frac{g_{m3}g_{m4}}{C_1C_2}} \qquad (5)$$

Recognizing the common transfer function of 2nd order low-pass filter as

$$H(S) = \frac{\omega_0^2}{S^2+\frac{\omega_0}{Q}S+\omega_0^2} \qquad (6)$$

Where ω_0 is the corner frequency and Q is quality factor.
The transconductance is derived as

$$g_m = \frac{I_{out+}-I_{out-}}{V_{in+}-V_{in-}} \qquad (7)$$

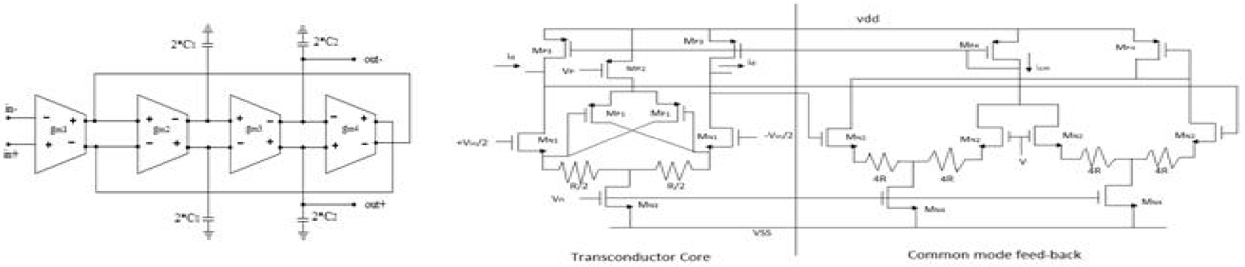
The transconductances of g_{m1}, $g_{m3,}$ and g_{m4} should be kept the same and the transconductance of g_{m2} is 1.848 times the other Transconductances [28]
To get the 2nd order Butterworth low pass filter response.

$$g_{m2} = 1.848*g_m \qquad (8)$$

Three of the four OTAs of the 2nd order low pass filter are identical; the outer OTA can easily be adapted with only changing the OTA current.

V. OTA DESIGN

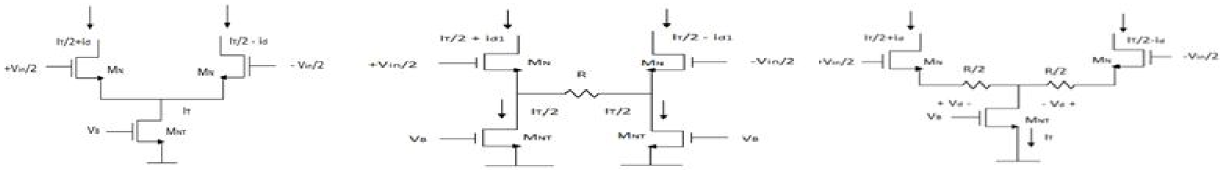
Fig. 7(b*)* shows the complete diagram of OTA including the CMFB circuit. The transconductor core consist of a source degenerated differential pair with auxilliary differential techniqiue is presented.



(a) (b)

Fig. 7.(a)Second orderGm-C low-pass filter circuit, (b) Completetransconductor with common mode feed-back

A. Source Degeneration Technique



(a) (b) (c)

Fig.8.Differential pairs: a) Conventional differential pair; b) Differential pair with degeneration resistance; and c) Differential pair with degeneration resistance and tail current transistor.

In a basic cell (differential pair) as shown in Fig. 8(a)when all transistors operate in saturation region,the large-signal behaviour of the single ended output current (i_d) can be expressed by Taylor series expansion as

$$I_0 = \sum_{n=0}^{\infty} G_{MN\_(2n+1)} \cdot V_{in}^{2n+1} \tag{9}$$

For moderate signal swing, G_{MN_1} and G_{MN_3} are the most significant; is the linear transconductance term and undesired third-order nonlinear term respectively, represented as an equivalent resistor at the Source [29] leads to

$$G_{MN\_1} = \frac{1}{2}\frac{\sqrt{K_P\left({W_N}/{L_N}\right)I_T}}{1+\frac{2}{\epsilon_{crit}}\sqrt{\frac{I_T}{W_N\,L_N K_P}}} \tag{10}$$

The coefficient of the third-order nonlinearity is

$$G_{MN\_3} = -\frac{G_{MN\_1}}{8\left(\frac{I_T L_N}{K_P.W_N}\right)\left(1+\frac{2}{\epsilon_{crit}}\sqrt{\frac{I_T}{W_N L_N K_P}}\right)^3} \tag{11}$$

Where W_N is width and L_N is length of transistor M_N. K_P technological parameter, I_T is the tail Current, ε_{crit} is critical electrical field.

As shown in Fig. 8 (b) and (c), if a source degeneration resistance is connected between source terminals of two M_N transistors the single ended ac component of the output current approximately becomes

$$i_{d1} \cong \frac{G_{MN\_1}}{(1+G_{MN\_1}R)} v_{in} + \frac{G_{MN\_3}}{(1+G_{MN\_1}R)^4} v_{in}^3 \qquad (12)$$

Due to the source degeneration resistance, the source degeneration factor defined as $N_r = G_{M1}R$, according to this, the improvement in third-order harmonic distortion ($HD3_{imp}$) of the circuits Fig. 8(b) & (c),over the circuit Fig. 8(a), is

$$HD3_{imp} = \frac{HD3_{(b,c)}}{HD3_{(a)}} = \frac{1}{(1+N_r)^3} \qquad (13)$$

The input referred thermal noise density for the differential pair of Fig. 8(b), is given by

$$\frac{\overline{V_{inoise}^2}}{\Delta f} = \frac{4KT}{G_{MN\underline{1}}}\left(\Upsilon + N_r + 2\Upsilon N_r^2 \frac{G_{MT}}{G_{MN\underline{T}}}\right) \qquad (14)$$

Where, T is the temperature in Kelvin degrees, k is the Boltzman constant, G_{MT} is the small-signal transconductanceof the transistor $M_{NT.}$

OTA's linearity improves by increasing N_r according to (5), but (6) shows that this approach will increase the input referred noise level, because the two tail current transistor introduce some differential noise if the value of source degenerated resistors is large, by placing the tail current transistor in the middle of the source degeneration resistor as shown in Fig. 8(c),This term can be minimized and the noise of the tail current split equally in both branches and appears as common mode noise which is rejected due to fully differential nature of the topology and the common node is always unaffected by the differential signal variations by using this topology.

The drawback of the circuit shown in Fig. 8(c)is that the additional dc voltage drop through the degeneration resistors, thereby consuming voltage headroom for the input signal. Therefore limited overdriving voltages and source degeneration factor N_r must be used.

B. Auxiliary differential pair technique

In order to reduce the harmonic distortion components without sacrificing other parametersauxiliary differential pair technique is present in this pair.

To illustrate the concept, let us consider several differential pairs with its own degeneration resistor; the transconductance curves for fixedDegeneration resistances and curves for variable degeneration resistance with input voltage are plotted in Fig. 9(a), By using Auxiliary differential pair technique results in a flattened transconductance curve and enhanced linearity, therefore degenerated resistor is replaced by the parallel of a degenerated resistor and ADP shown in Fig. 9(b), Based on the current to voltage relation depicted in (1) for the differential pair of Fig. 8(a), the output current of the circuit in Fig. 9(b) written as

$$i_0 = G_{MN\_1}(v_{in} - v_{res}) + G_{MN\underline{3}}(v_{in} - v_{res})^3 \qquad (15)$$

Where G_{MN_1} is the small-signal transconductance and G_{MN_3} is third-order nonlinear coefficient for the differential pair without source degeneration. $V_{res}$is voltage across the resistance and the ADP. The current of the ADP is given by

$$i_p = -G_{MP\_1}v_{res} - G_{MP\_3}v_{res}^3 \qquad (16)$$

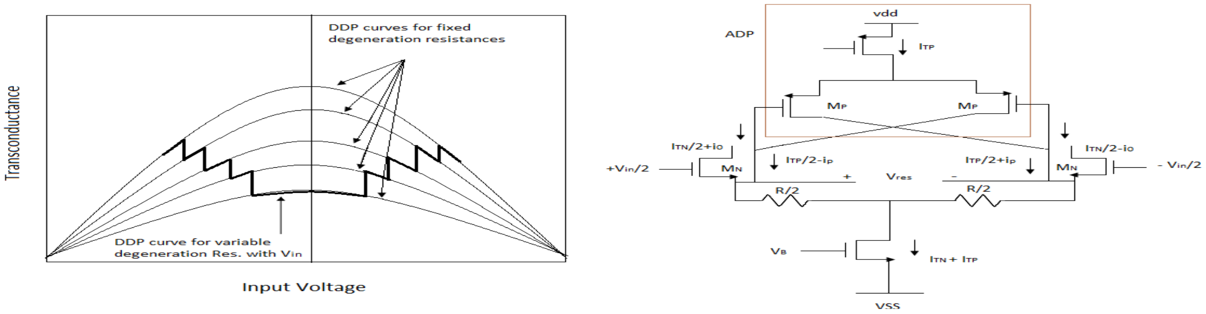
Transconductance and GMP_3 is the nonlinear Where GMP_1 is the small signal coefficient for the ADP. Since i_0 = ip + v_{res}/Rthe output current of OTA can be expressed as [29]

$$i_0 = \frac{G_{MN\underline{1}}}{1+\frac{RG_{MN\underline{1}}}{1-RG_{MP\underline{1}}}} v_{in} + \frac{G_{MN\underline{3}} - G_{MP\underline{3}}\frac{G_{MN\underline{1}}^4}{\left(R^{-1}-G_{MP\underline{1}}\right)^4}}{\left(1+\frac{RG_{MN\underline{1}}}{1-RG_{MP\underline{1}}}\right)^4} v_{in}^3 \qquad (17)$$

The third-order intermodulation distortion (IM3) improvement factor can be described by

$$\frac{HD3_{withADP}}{HD3_{withoutADP}} \cong 1 - \left(\frac{G_{MP\_3}}{G_{MN\_3}}\right)\left(\frac{G_{MN\_1}R}{1-G_{MP\_1}R}\right)^4 \qquad (18)$$

The ADP must be designed such that the right Hand most term remains close to 1.since the ADP transconductance is small, $G_{MP\text{-}1}$<<1, andit is negligible; e.g., 0.1.



(a) (b)

Fig. 9.Linearity enhancement: a) principle of operation; and b) circuit implementation with ADP.

The proposed diagram of OTA including the CMFB circuit, tansistors M_{N1} use an overdrive voltage and the tail current flowing through M_{N3} i.e. tail current transistor, use of folded cascoding or any other additional circuit has been avoided the output is taken directly from the drains of M_{N1} which optimize the structure for power and noise performances. Transistors M_{N1} remain in saturation for output peak voltages of less than one half the threshold voltage of M_{N1}, which is the case for the signals used in the filters implementation. For better transistormatching, all transistors lengths are equal except transistors M_{P3} to enhance the OTA output impedance. The CMFB circuit is designed with a power consumption of ¼ that of the core.
By using these two techniques the circuit area reduces thus we can use this in wireless application such asmobile application as GSM, Bluetooth, and WCDMA etc. to meet the required specification.

VI. COMPARISON

TABLE – I

Comparison of different order Butterworth filter based on different structure of OTAs

Reference → **Parameter ↓**	**Ref 30**	**Ref 28**	**Ref 31**	**Ref 18**	**Ref 17**	**Ref 32**	**Ref 33**
Filter order	7th	4th	5th	4th	3rd	3rd	6th
Technology	0.8 µm pspice	0.35 µm CMOS	0.25 µm CMOS	0.18 µm CMOS	0.18µm CMOS	0.35 µm CMOS	0.18 µm CMOS
Area, mm^2	NA	NA	0.9	0.95	< 0.5	0.25	0.8 × 0.28
Supply voltage, V	1 .5	2.7	2.5	5.0	1.5	1.5	1.8
Tuning range	333KHz - 1 MHz	200KHz – 2.5 MHz	600KHz – 6MHz	1.4MHz - 16 MHz	135 KHz – 2.2 MHz	330 MHz	3 – 24 MHz
Gm, µs	62.8	50	NA	NA	25	NA	NA
Power consumption,	6.43	<620 µA	0.9 - 2.7mA	40	1.57 – 1.92mw	1.4 mw	NA
HD3, dB	-50	-39(0.6 VPP @ 2.5 MHz)	NA	<-60	-50 (0.4 VPP @ 2.5 MHz)	NA	NA

VII. RESULTS AND DISCUSSION

Results obtained from present study is summarized as: a) wide tuning range and high linearity can be achieved using better linearization technique to design operational transconductance amplifier(OTA). b) Low power consumption and small filter area can be easily optimized using lower order filter to fulfill the application requirement.

Filter is a very small element throughout the communication system, thus smaller filter area and low power consumption is required. Higher order filters provide wide tuning range and high linearity. Besides this higher order filterresults in increase power consumption and increased filter area because they have the large number of component.All these parameters can be achieved using two linearization techniques; source degeneration and auxiliary differential pair to design operational transconductance amplifier (OTA) and using lower order filter.

VIII.CONCLUSION

The study of different filter orders has been carried out. Thereafter it is concluded that the increment in filterorder i.e. making higher order filter, leads the increment in the filter components. This is resulting in cost and area enhancement and also the design becomes complex. To optimize the complexity of structure, cost and area the best possible solution is to use the lower order filterwith OTA. The OTA is composed of two techniques which enhances the linearity of filter and does not affect other parameters and this gives wide tuning range with lower order filter.

REFERENCES

[1] ParsiK., BurnsR., ChaikenA., ChambersM., ForniW., HarnishfegerD., TaylorS., PennelM., PerezJ., RaoN., RohrbaughM., RossM., and StuhmillerG., “APRML read/write channel IC using analog signal processing for 200 Mb/s HDD,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 499–531, Apr. 1997.

[2] DehaeneW., SteyaertM. S. J., and SansenW., “A 50-MHz standard CMOS pulse equalizer for hard disk read channels,” *IEEE J. Solid-StateCircuits*, vol. 32, pp. 977–988, July 1997.

[3] PaiP. K. D., BrewsterA. D., and AbidiA. A., “A 160-MHz analog front-end IC for EPR-IV PRML magnetic storage read channels,” *IEEEJ. Solid-State Circuits*, vol. 32, pp. 977–988, July 1997.

[4] ThaparH., LeeS. S., ConroyC., ContrerasR., YeungA., J. ChernG., PanT., and ShihS. M., “Hard disk drive read channel: Technology andtrends,” *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 309–316, 1998.

[5] BloodworthB. E., SiniscalchiP. P., DeVeirmanG. A., JezdicA., R. Pierson, and SundararamanR., “A 450-Mb/s analog front end for PRML read channels,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 1661–1675,Nov. 1999.

[6] KiriakiS., LakshmiT., FeyginG., StaszewskiB., PiersonR., KrenikB., de WitM., and NagarjK., “A 160-Mhz analog equalizer formagnetic disk read channels,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 1839–1850, Nov. 1997.

[7] MehrI. and WellandD. R., “A CMOS continuous-time G –C filter for PRML read channel applications at 150 Mb/s and beyond,” *IEEE J.Solid-State Circuits*, vol. 32, pp. 499–531, Apr. 1997.

[8] RaoN.,BalanV., and ContrerasR., “A 3V 10–100MHz continuous-time seventh-order equiripple linear phase filter,” in *IEEE Int. Solid-StateCircuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1999, pp. 44–46.

[9] Altekar*et*S. *al.*, “A 700 Mb/s BICMOS read channel integrated circuit,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, pp. 184–185.

[10]GopinathanV., TarsiaM., and ChoiD., “Design considerations and implementation of a programmable high-frequency continuous-time filter and variable gain amplifier in submicrometer CMOS,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 1698–1707, Dec. 1999.

[11] VoormanH. and VeenstraH., “Tunable high-frequency G –C filters,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 1097–1108, Aug. 2000.

[12] Sánchez-SinencioE. and MartínezJ. Silva, “CMOS transconductance amplifiers, architectures and active filters:Atutorial,” *Proc. IEE CircuitsDevices Syst.*, vol. 147, no. 1, pp. 3–12, Feb. 2000.

[13] SunY., Edited: Wireless Communication Circuits and Systems, IEE, London, UK, 2004.

[14]LacanetteKerry, “A Basic Introduction to Filter Devices-Active, Passive andSwitched Capacitor”, National Semiconductor Application Note 779, April 1991.

[15]GratzAchim, “Operational Transconductance Amplifiers”, http://synth.stromeko.net/diy/OTA.Pdf.2008

[16] GeigerR. L., Sanchez-SinencioE., “Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial”, IEEE Circuits and Device Magazine, Vol. 1, March 1985

[17]Lo T-Y &Hung C-C, “Multi-mode Gm-C channel selection filter for mobile applications in 1-V supply voltage”, IEEE Trans Circuits &systems-II: Express Briefs, 55 (2008) 314-318

[18] CheungDarwin, BultKlaas, BuchwaldAaron, “10 MHz 60 db dynamic rang 4th order Butterworth low pass filter” 2009

[19] ItakuraT., UenoT., TanimotoH., YasudaA., FujimotoR., AraiT. and KokatsuH. “ A 2.7-v, 200-kHz, 49-dBm, stopband-IIP3,low noise, fully-balanced, Gm-C filter IC”, IEEE J. Solid-State circuits, vol.34, no. 8, PP. 1155-1159, August 1999.

[20] YebingGan, ChengyanMa, GuoshunYuan. “A dual-mode complex filter for GNSS receivers with frequency tuning”, Journal of Semiconductors, 2009, 30(10): 105004

[21] Emira A A, Sanchez-Sinencio E. A pseudo differential complex filter for bluetooth with frequency tuning. IEEE Trans Circuits SystII, 2003, 50(10): 742

[22] Guthrie B, Hughes J, Sayers T, et al. A CMOS gyrator low-IF filter for a dual-mode bluetooth/zigbee transceiver. IEEE J Solid- State Circuits, 2005, 40(9): 1872

[23] Pavan S, Tsividis Y P, Nagaraj K. Widely programmable highfrequency continuous-time filters in digital CMOS technology. IEEE J Solid-State Circuit, 2000, 35: 503

[24] Chen M. A 2-Vpp, 80-200 MHz fourth-order continuous-time linear phase filter with automatic frequency tuning. IEEE J Solid- State Circuits, 2003, 38(10): 1745

[25] Chamla D, Kaiser A, Cathelin A, et al. A switchable-order Gm–C baseband filter with wide digital tuning for configurable radioreceivers. IEEE J Solid-State Circuits, 2007, 42(7): 1513

[26] DequnMa, FuliangCui, JieHe, et al. Design considerations and implementation for low power on-chip automatic tuning. Chinese Journal of Semiconductors, 2004, 25(9): 11869.

[27] KardontichikJ. E., “Introduction to the Design of Transconductance Capacitor Filters”, Kluwer Academic Publishers, 1992

[28] Stehr U, Henkel F, DalligeL, Waldow P,” A fully differential CMS integrated 4th order reconfigurable GM-C low pass filter for mobile communication”, in IEE procInt on Electronics Circuits & Systems,1(Sharjah, UAE) 2003,144-147

[29] GrayP. R., HurstP. J., LewisS. H., and MeyerR. G., Analysis and Design of Analog Integrated Circuits. New York: Wiley, 2001

[30] IbaragiE., HyogoA., SekineK., “A 1-MHZ 7TH-ORDER CONTINUOUS-TIME LOWPASS FILTER USING VERY LOW DISTORTION CMOS OTAS”, ISCAS2000 - IEEE International Symposium onCircuits and Systems, May 28-31, 2000, Geneva, Switzerland.

[31] MohieldinA. N., Senchez-Sinencio E., “A Dual-Mode Low-Pass Filter for 802.11b/Bluetooth Receiver”, 0-7803-8480-6/04/$20.00© 2004 IEEE

[32] Wongnamkum S &Thanachayanont A, “New class-AB operational transconductance amplifier for high-speed switched-capacitor circuits”, in IEEEIntsymp comm. & Inform Tech., 1 (2004) 531-535

[33] WenguangPan, ChengyanMa, YebingGan, and TianchunYe, “A reconfigurable OTA-C baseband filter with wide digital tuning for GNSS receivers”, Journal of Semiconductors Vol. 31, No. 9 September 2010