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An Efficient VLSI Architecture for Primary Synchronization Signal Detector

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ABSTRACT: In this paper, we present a novel design for the detection of primary synchronization signal in a Long Term Evolution (LTE) system based device at the expense of low cost and low power. This is facilitated by using a matched filter architecture which incorporates parallel processing. The approach of a 1-bit analog-to-digital converter (ADC) with down-sampling is compared with that of a 10-bit ADC without down-sampling under multi-path fading conditions defined in LTE standard for user equipment (UE) performance test. A high performance primary synchronization signal detection method is derived in this paper.

Keywords: Low cost, low power, matched filter, primary synchronization signal (PSS).

I. INTRODUCTION

The LTE, also referred as EUTRA (Evolved UMTS Terrestrial Radio Access), is intended to enhance the 3g and 3.5g systems in order for them to adopt higher peak data rates with extremely high mobility support. The LTE, as one of the latest steps in an advancing series of mobile telecommunications system, can be seen to provide a further evolution of functionality, increased speeds and general improved performance comparing to the third generation systems [1].The LTE specification provides downlink peak rates of at least 100 Mbps, and uplink of at least 50 Mbps. Synchronization sequence is more important because its detection affects not only search time but also performance of demodulation. The 3GPP working group decided to adopt Zadoff-Chu (ZC) sequences as the downlink primary synchronization signal (PSS) and the uplink random access preamble. A Zadoff-Chu sequence is a complex-valued mathematical sequence which exhibits the useful property that cyclically shifted versions of it are orthogonal to each other. The ZC sequences have flat frequency domain autocorrelation property and the low frequency offset sensitivity [5]. The primary synchronization signal is detected by using a non coherent detection method since there is no reference information initially. The main objective of this paper is to propose an efficient matched filter architecture that involves less number of complex multiplications to occur. The system model and PSS definition are presented in Section II. A brief review of the matched filter approach is presented in Section III. Afterwards, both the method of 1-bit ADC with down-sampling and that of 10-bitADC without down-sampling for PSS detection are discussed in Section IV. Section V addresses different implementation architectures of PSS detection. Whereas their simulation results are shown in Section V1 Finally, conclusion remarks are given in Section VII.

II. SYSTEM MODEL AND PROBLEM DEFINITION

A. OFDM System Model with Carrier Frequency Offset (CFO)

3GPP adopt OFDM to improve spectrum efficiency. In OFDM systems, a sequence of complex data symbols is considered as orthogonal subcarriers during the k th OFDM blocks, the sequence of data symbols is defined as follows:

$$d(k) = [d0\ (k),\ d1\ (k),\ d2\ (k),\ dN\text{-}1(k)]^{T}. \quad (1)$$

The sequence of data symbols is modulated using an –point inverse discrete Fourier transform (IDFT) process that produces the sequence

$$x\ (k)=W\ d(k) \quad (2)$$

Where W is the normalized-by-N IDFT matrix and x(K) is

$$x\ (k)=[x_0(k),x_1(k)\ldots x_{N-1}(k)]^{T} \quad (3)$$

Consequently, the nth sample in the sequence x (k) can be ex-pressed as

$$xn(k)=\frac{1}{\sqrt{N}}\sum_{i=0}^{N-1} di(k)\ e^{\frac{j2\pi in}{N}},\ n=0,1,\ldots\ldots N\text{-}1 \quad (4)$$

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In fading channels, a time-domain guard interval, which is named as cyclic prefix (CP), is created by copying the last samples of the IDFT output and appending them at the beginning of the OFDM symbol to be transmitted. So the transmitted OFDM block consists of (N + Ng) samples [7].At the receiver side, after removing the first CP samples, the received sequence

$$y(k)=[y0(k),y1(k),y2(k),.....yN\text{-}1(k)]^{T}. \quad (5)$$

Is obtained [9]

$$y(k) = e^{j\frac{2\pi}{N}\mathcal{E}k(N+Ng)}A(\mathcal{E})WH(k)d(k) + N(k) \quad (6)$$

where Ɛ represents the normalized CFO, and A(Є) represents the effect of the accumulated phase rotation caused by the CFO on the time domain samples

$$\mathcal{E} \in (-0.5, 0.5) \quad (7)$$

$$A(\mathcal{E}) = diag\left([e^{j\frac{2\pi\epsilon}{N}X0}, e^{j\frac{2\pi\epsilon}{N}X1}, \dots, e^{j\frac{2\pi\epsilon}{N}X(N-1)}]^{T}\right. \quad (8)$$

H(k) denotes the channel frequency response during the kth OFDM block.

$$H(k) = diag([H0(k),H1(k), H2(k),.....HN\text{-}1(k)]^{T}). \quad (9)$$

N(K)represents a zero-mean complex white Gaussian noise sample with variance N_{σ}.Assuming that the receiver sampling clock is aligned to that of the transmitter, then the nth element of y(K) can be expressed as

$$y_n(k) = \frac{e^{j\frac{2\pi}{N}\epsilon\, k(N+Ng)}}{\sqrt{N}} \sum_{i=0}^{N-1} di(k)Hi(k)e^{j\frac{2\pi n}{N}(i+\epsilon)} + Nn(k) \quad (10)$$

$$R_{spat} = R_{eNB} \otimes R_{UE} = \begin{bmatrix} 1 & \alpha^{\frac{1}{9}} & \alpha^{\frac{4}{9}} & \alpha \\ \alpha^{\frac{1}{9*}} & 1 & \alpha^{\frac{1}{9}} & \alpha^{\frac{4}{9}} \\ \alpha^{\frac{4}{9*}} & \alpha^{\frac{1}{9*}} & 1 & \alpha^{\frac{1}{9}} \\ \alpha^{*} & \alpha^{\frac{4}{9*}} & \alpha^{\frac{1}{9*}} & 1 \end{bmatrix} \otimes \begin{bmatrix} 1 & \beta^{\frac{1}{9}} & \beta^{\frac{4}{9}} & \beta \\ \beta^{\frac{1}{9*}} & 1 & \beta^{\frac{1}{9}} & \beta^{\frac{4}{9}} \\ \beta^{\frac{4}{9*}} & \beta^{\frac{1}{9*}} & 1 & \beta^{\frac{1}{9}} \\ \beta^{*} & \beta^{\frac{4}{9*}} & \beta^{\frac{1}{9*}} & 1 \end{bmatrix} \quad (11)$$

Where α and β is define in Table VI [5], and $\otimes$ denotes Kronecker product.

B. PSS

The P-SCH is used for obtaining the time and frequency synchronization necessary for demodulating the S-SCH [6]. The UE achieves synchronization by correlating the received P-SCH signal with a replica of the transmitted signal (i.e., using a matched filter), thereby identifying a correlation peak at the proper symbol timing. The Primary Synchronization Signals are modulated using one of three different frequency domain Zadoff-Chu sequences. The sequence $d_u(n)$ used for the PSS is generated from a frequency-domain ZC sequence [1] according to

$$du=\begin{cases} e^{-j\frac{\pi un\,(n+1)}{63}} & ,n = 0,1,\dots\dots,30 \\ e^{-j\frac{\pi u\,(n+1)(n+2)}{63}} & ,n = 31,32,\dots.61 \end{cases} \quad (12)$$

Where the ZC root sequence index is given by Table II

The three different ZC sequences are orthogonal to each other, and each sequence corresponds to a sector identity which is in the range of 0 to 2. The Primary Synchronization signal first determines one of three cell identities (0, 1, 2), also represented by N (2) ID. Then the secondary synchronization signal is used to determine a cell ID between 0 and 167 represented by N (1) ID. A Zadoff-Chu sequence is a complex-valued mathematical sequence which exhibits the useful property that cyclically shifted versions of it are orthogonal to each other. Thus, it is easy to detect PSS during the initial synchronization because the ZC sequence has the flat frequency domain autocorrelation property and the low frequency offset sensitivity.

III. FUNDAMENTAL OF PSS DETECTION

The main function of PSS is to detect the boundary of a frame where non-coherent detection method has to be used at the receiver since there is no known reference information initially [7]. Matched filter is a basic non-coherent detection method that can be used to detect PSS efficiently. The sequence in (12) is mapped to the subcarriers around DC and transformed to time domain by 64-point IDFT. To detect this signal at the receiver, the correlation with the time domain signal of the ZC sequence is calculated [2]–[4].

$$Cu(m)=(W^{H}\,du)^{H}y \quad (13)$$

Where y is the successive 64-by-1 received signal vector, is the DFT matrix, and is 64-by-1 vector composed of punctured at DC.

Then, from (13), the coefficients of the matched filter can be obtained

$$Coeff= (W^{H}\,du)^{H} \quad (14)$$

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Where

$$\text{Coeff} = [\text{Coeff}(63)\text{Coeff}(62).....\text{Coeff}(1)\text{Coeff}(0)] \quad (15)$$

and the matched filter can be expressed

$$MF = \sum_{i=0}^{63} \text{coeff}(k)y(t-k) \quad (16)$$

Where y (k) is the received signal.

TABLE I
DELAY PROFILES FOR E-UTRA CHANNEL MODELS

Model	Number of channel taps	Delay Spread (r.m.s)	Maximum excess tap delay (span)
Extended Pedestrian A (EPA)	7	45ns	410ns
Extended vehicular A (EVA)	9	357ns	2510ns
Extended Typical Urban	9	991ns	5000ns

TABLE II
ROOT INDICES FOR THE PSS

$N_{ID}^{(2)}$	Root index u
0	25
1	29
2	34

IV. PROPOSED DESIGN OF PSS

The receiver side of an OFDM system model ADC is present for digital representation of the received signal. 10-bit ADC is generally preferred to be used at the receiver. From the power consumption perspective, a 10-bit analog-to digital converter (ADC) uses more power than 1-bit ADC. Typically, the power consumption of a 1-bit 122.88 MHz ADC composed of one comparator is about 200 W, while the power consumption of a 10-bit 122.88 MHz pipelined ADC is about 50mW.

To come up with a low-power solution, a method of PSS detection using 1-bit ADC is proposed.PSS is transmitted periodically, twice per frame which lasts 10 ms [8]. The sampling rate of the receiver is 122.88 MHz; however, the date rate of input data to the matched filter is 1.92 MHz Thus, 9600 samples at the output of the matched filter need to be buffered during the 5 ms period, which is not area and cost efficient. To come up with a low cost solution, a method of down-sampling by 8 is used at the output of matched filter.

A. Method without Down-Sampling by 8 for 10-Bit ADC

From the last section, the matched filter as expressed in (16) can be reformulated when using a 10-bit, 122.88 MHz pipelined ADC

$$MF\ qt = \sum_{i=0}^{63} \text{coeff}(k)\ y\ qt\ (t-k) \quad (17)$$

where yqt(k) is the received signal sampled by a 10-bit, 122.88 MHz pipelined ADC, and is obtained in (14) and (15).Every output of the matched filter is buffered since there is no down-sampling module, and it needs a large area buffer which is very costly.

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B. Method With Down-Sampling by 8 for 1-Bit ADC

Equation (16) can be reformulated when using a 1-bit, 122.88 MHz ADC

$$\text{MF qo} = \sum_{i=0}^{63} \text{coeff(k)y qo (t} - \text{k)} \qquad (18)$$

Where y_{qo} (K) is the received signal sampled by a 1-bit, 122.88MHz ADC, and is obtained in (14) and (15).Every output of the matched filter is down-sampled by 8

$$\text{MF qod} = \max \begin{cases} MFqo(8n), MFqo(8n+1), \\ MFqo(8n+2), MFqo(8n+3), \\ MFqo(8n+4), MFqo(8n+5), \\ MFqo(8n+6), MFqo(8n+7) \end{cases} \qquad (19)$$

where MF_{qod} is the output of the down-sampling module. Now, only 1200 outputs need to be buffered during 5 ms with an additional comparator of 1 out of 8 implementing the down sampling module. This results in less area which translates to lower cost in a practical system. Its implementation architecture is discussed in next chapter [12].

TABLE III
SIMULATION ASSUMPTIONS

PARAMETER	UNIT
Number of Rx Antenna	4
Number of Tx Antenna	4
Frequency offset	12.5 KHz
Carrier Frequency	2.5Ghz
Symbol detection	Replica-based
Root index	29

V. HARDWARE IMPLEMENTATION

The implementation architecture of the proposed method is presented here along with the new matched filter architecture that reduces the complexity involved in existing methodology. The matched filter is an important component in the PSS detection. We use 64-tap time domain matched filter; hence 64 complex multiplication units per matched filter are used in the calculation in [16].

A. Existing Architecture of Matched Filter

In this architecture input data that is being received is processed serially. As per our simulation assumptions, 84 matched filters are required in the system. So a total of 5376 units of complex multiplication is needed. Instead we can use only one complex multiplication unit during 64 cycles instead of using 64 units of complex multiplication. As a result, 84 units of complex multiplication are enough for the whole system. But the problem that it encounters is that since the data is processed serially, so significant amount of delay is encountered due to the shifting involved in it. This problem is overcome in our proposed method [19].

B. Architecture of PSS Detection

A mismatch of up to 14 part per million (ppm) can exist between the oscillators at the eNodeB and at the UE, so seven groups of matched filters are used to cover the range of 14 ppm, 14 ppm. Each group contains three matched filters to detect three different physical-layer IDs of value 0, 1, or 2 [21]. Therefore, there are 21 hardware units as shown in Fig. 2 for each receiver antenna. Since the system is MIMO 4-by-4 and there are 4 receiver antennas at the UE end, 84 such hardware units are involved in the architecture of the PSS detection. A total of 9600 samples during 5 ms and thus a single port RAM with 9600 addresses is needed.

As described above, there are 84 such RAMs in the system, and the area is too large for the UE chip; therefore an area efficient architecture is proposed as shown in Fig. 2. Compared to the architecture in Fig. 1, a small RAM with 8 addresses is added whose function is to find the maximum value of every eight correlations. As a result, only 1200 correlation values need to be stored in RAM with 1200 addresses, which reduce the RAM size of the whole system by a factor of almost 8 [22]. We can observe that the area of the area-efficient architecture is much smaller than that of the original architecture, which reduces the Cost of the chip significantly. From the power perspective, not only the 1-bit ADC reduces the power consumption, but the hardware of digital logic also does.

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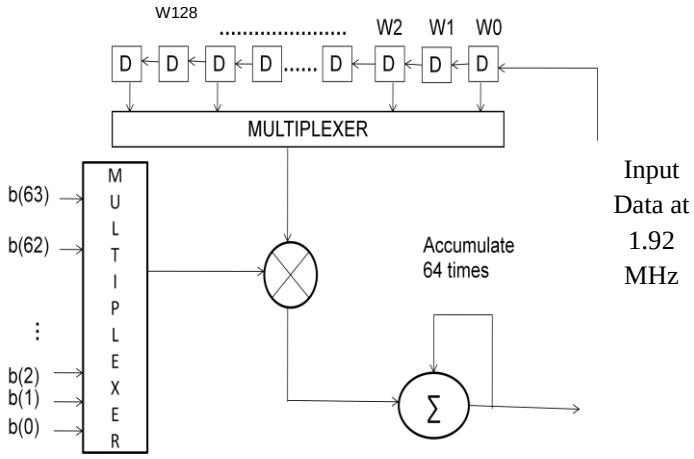

Figure 1 Existing Matched Filter Architecture

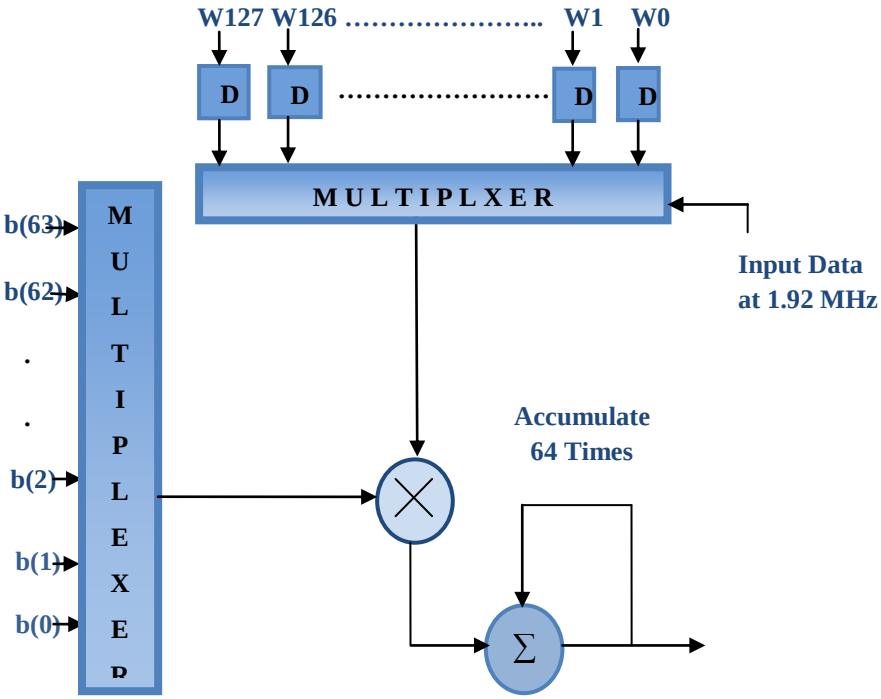

Figure 2 Proposed Matched Filter Architecture

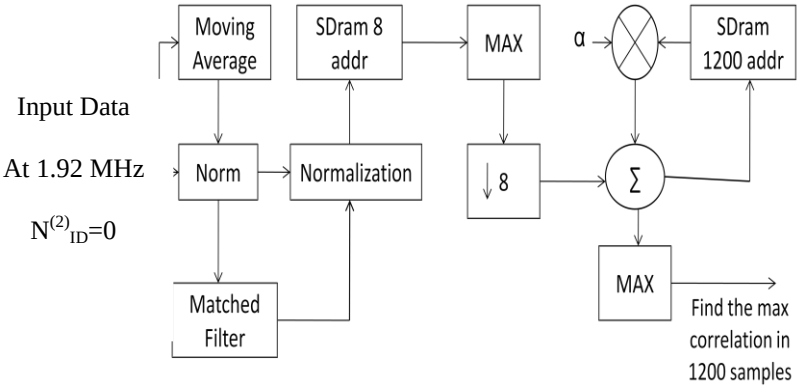

Figure 3 Architecture of PSS Detection

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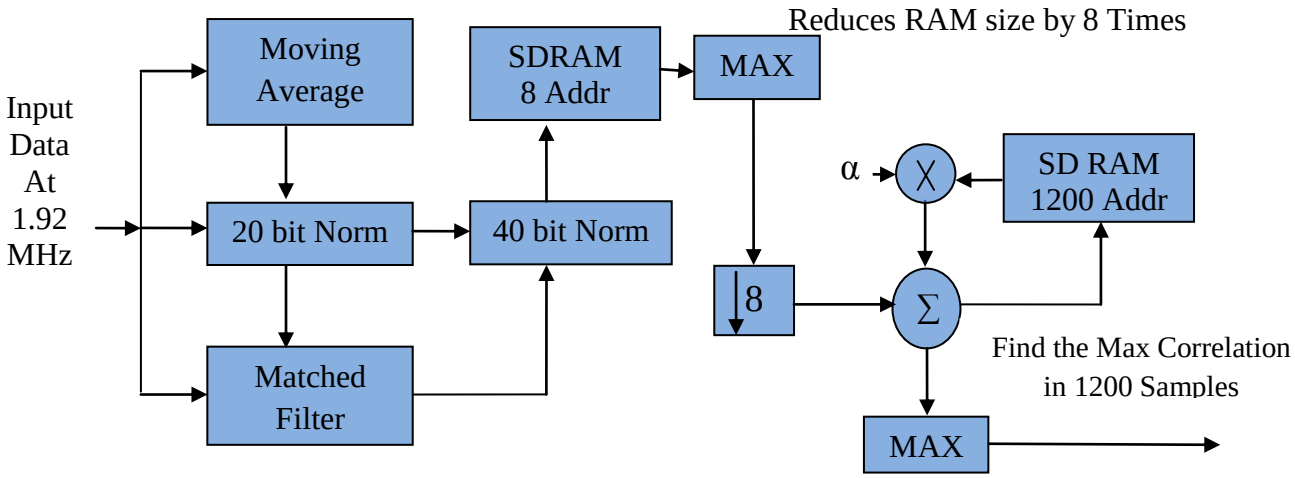

Figure 4 Original architecture of the whole PSS detection

VI. SIMULATION RESULTS

Primary synchronous signal is designed for cell search and handover in 3GPP LTE systems, which is transmitted every 5ms. Search time of PSS detection is an important criterion when measuring its performance. To compare the performance using a 10-bit 122.88MHz ADC without down-sampling and that using a 1-bit 122.88MHz ADC with down-sampling by 8, the parameters listed in Table III are used in the simulation [23].The simulation results for search time of both the methods under EPA 5 Hz channel model are shown. It is clear that the search time of both methods under EPA 5 Hz model with low correlation channel matrix, is very close to each other. The Existing and the proposed model is simulated using altera quartus software.The power and gate analysis are carried out for both the methods.The simulation results show that the performance of our proposed matched filter architecture which incorporates parrellel processing is efficient in terms of power [24]. Furthermore,the implemenation of our proposed architecture with the method of 1-bit adc with down sampling by a factor of 8 results in the reduction of overall gates required for it to be implemented in the user equipment.This is shown in table V.

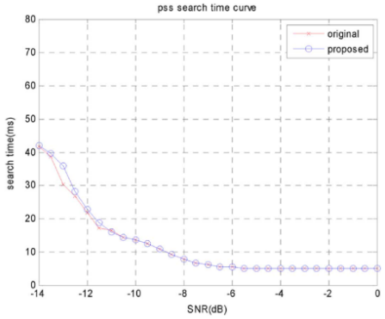

Figure 5 Performance of both methods using low correlation channel matrix and EPA 5 Hz channel model.

TABLE IV : MEMORY CONSUMED BY VARIOUS MODULES

MODULES	MEMORY CONSUMPTION (Kilo Bytes)
Matched Filter	233784
Moving Average	129400
40 bit Norm	116088
20 bit Norm	115064

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TABLE V
RESOURCE UTILIZATION OF VARIOUS MODULES

LOGIC UNITS	MODULES			
	Matched Filter	Moving Average	40 Bit Norm	20 Bit Norm
Adders / Subtractors	-	5	1	2
Comparators	4	-	-	-
IOs	62	41	42	43
Multipliers	2	-	-	-
MUX	-	1	-	-
Accumulator	-	2	-	-
Registers	131	37	11	20
Counters	3	1	1	-
Flip – flops	1338	48	14	20

TABLE VI
HDL SYNTHESIS OF MATCHED FILTER ARCHITECTURE

LOGIC UNITS	EXISITING	PROPOSED
Comparators	7	4
Counters	4	3
Flip – flops	1472	1338
IOs	44	62
Accumulators	6	2
Multipliers	-	2
Registers	259	131

TABLE VII
COMPARISON OF PROPOSED 1 BIT AND 10 BIT ADC

LOGIC UNITS	TEN BIT	ONE BIT
Adders / Subtractors	25	34
Comparators	3	3
Counters	16	16
Flip – flops	5115	1659
IOs	142	124
Multipliers	6	-
MUX	7	7
Accumulator	2	2
Registers	543	543
IO buffer	142	124
Memory in Kilo Bytes	447928	339896

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VII PERFORMANCE WITH EXISTING STATE-OF-THE-ART MATCHED FILTER ARCHITECTURE

The matched filter architecture, in the design [4] uses 84 matched filters and 5376 units of complex multiplication making the practical implementation difficult. The matched filter architecture in the design [22] requires only 84 units of complex multiplication and this is practically possible. But the cost for implementation is high. In the design [40], the matched filter architecture uses a serial mechanism and consumes more logic elements. The proposed architecture is power and area efficient. In the proposed matched filter architecture, a parallel mechanism is used for inputting the data and the logic elements utilized is also significantly reduced. One bit ADC with down sampling by factor 8 consumes 339896 Kilo Byte and the power utilized is less when compared to design [40].Ten bit ADC without down sampling, consumes 46.88Mili Watt as static power and 16.48Mili Watt as dynamic power. The logic elements utilized is also significantly reduced when compared to the existing state of architecture. The problem with the existing architecture is, since the data is processed serially a significant amount of delay is encountered due to the shifting involved in it. This occurs when one value is high and subsequent values are low, no matter what the shift is, the output of the MUX will be the same. This causes unnecessary multiplication to occur and also the delay that is involved affects the overall performance of the system. This problem is overcome in our proposed architecture which incorporates parallel processing. So, there is no shifting of input data during each input clock. As a result of it, the effect of propagation delay is overcome and the table 4.6 shows the comparison with the existing state architecture.

TABLE VIII
SIMULATION RESULTS FOR POWER

POWER	PROPOSED		EXISTING	
	One bit	Ten bit	One bit	Ten bit
Thermal Power	68.02mw	224.39mw	159.77mw	1009.47mw
Core Dynamic Power	1.94mw	16.48 mw	91.44mw	559.56mw
Core Static Thermal Power	46.36mw	46.88mw	46.45mw	48.10mw

TABLE IX
COMPARISON WITH PREVIOUS WORK

WORK	MEMORY (KILO	STATIC POWER	DYNAMIC POWER	LOGIC ELEMENTS
Design [4]	-	-	-	84 Matched Filters (5376 Units Of
Design[11]	-	-	-	84 Units Of Complex Multiplications
	Design [9]			
Matched Filter	247224	-	-	2524
1 Bit ADC With Down Sampling	704696	46.45	91.44	2844
10 Bit ADC Without Down	454072	48.45	559.56	5660
	Proposed Architecture			
Matched Filter	233784	-	-	1733
1 Bit ADC With Down Sampling	339896	46.36	1.94	2244
10 Bit ADC Without Down	447928	46.88	16.48	4877

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VIII CONCLUSION

The detection of PSS plays a primary role in mobile communication. Theoretically, detection with 1-bit ADC and with down-sampling would degrade the performance and prolong the detection time. However, due to the inherent advantage of the ZC sequence, simulation results show that the performance of the proposed method using a 1-bit ADC with down-sampling by 8 does not degrade much compared with that using a 10-bit ADC without down-sampling in the presence of frequency offset under several typical LTE propagation channels. Subsequently, two different implementation architectures of the PSS detection are presented. The area and the power consumption of the original implementation architecture are too large. Based on the simulation results in the proposed architecture, the PSS can be detected efficiently and accurately at a much lower power and lower cost which renders it feasible in the implementation of a UE chip.

IX FUTURE WORK

As first phase of the project, primary synchronization signal (PSS) is simulated using Model Sim. In the future phase of the project, FPGA implementation is proposed to be carried and investigation of real-time performance metrics will also be carried out. Further, detection of Secondary synchronization signal (SSS) will also be done. In case of significant deterioration in the performance, hardware solutions will be investigated.

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