ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 11, November

Analysis of Area – Delay Low Power Adders in QCA Using VHDL Code

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ABSTRACT: As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities.The physical limit can be overcome by using the approach quantum-dot cellular automata (QCA). In this brief, we propose a new adder that outperforms all state-of-theart competitors and achieves the best area-delay tradeoff. The 64-bit version of the novel adder spans over 18.72 μm2 of active area and shows a delay of only nine clock cycles, that is just 36 clock phases.

KEYWORDS: Quantum-dot cellular automata(QCA), Carry-Look ahead Adder (CLA), Ripple Carry Adder(RCA*)*

I. INTRODUCTION

Quantum-dot cellular automata (QCA) is an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a greatdeal of attention. Quantum-dot cellular automata (QCA) which works on array of coupled quantum dots. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic "0"and "1". Ripple-carry (RCA), carry look-ahead (CLA), and conditionalsum adders were presented in [11]. The carry-flow adder (CFA) shown in [12] was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures,including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, andHan–Carlson adders, were analyzed and implemented in QCA in[13] and [14]. In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-of the- art competitors and achieves the lowest area-delay product(ADP).

II. RELATED WORK

A. *Description:*

Multiple full adder circuits can be cascaded in parallel to add an N-bit number.There must be N number of full adder circuits,for constructing an N- bit parallel adder. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. This is due to the propagation delays inside the logic circuitry. The time elapsed between the application of an input and occurrence of the corresponding output is the Propagation delay.

Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. In this case the propagation delay is the time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal.

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ISSN (Print): 2320-9798

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B. *Basic Full adder block:*

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin)bit. Truth table and schematic of a 1 bit Full adder is shown below There is a simple trick to find results of a full adder.

Consider the second last row of the truth table, here the operands are 1, 1, 0 ie (A, B, Cin). Add them together ie 1+1+0 = 10 . In binary system, the number order is 0, 1, 10, 11……. and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result "10″ will give S=0 and Cout = 1 and the second last row is justified.

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

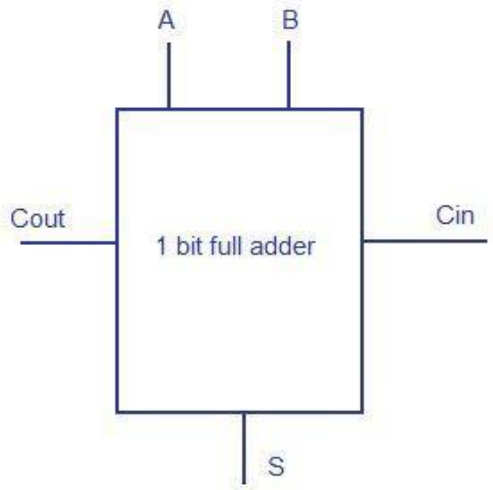

Fig 1. 1 bit full adder schematic and truth table

C.*Carry Lookahead adder* (CLA):

The carry lookahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits a_i and b_i are1, or (2) when one of the two bits is 1and the carry-in is 1. Thus, one can write

$$c_{i+1} = a_i.b_i + (a_i \oplus b_i).c_i$$
$$s_i = (a_i \oplus b_i) \oplus c_i$$

The above two equations can be written in terms of two new signals P_i and G_i, which are shown in Figure :

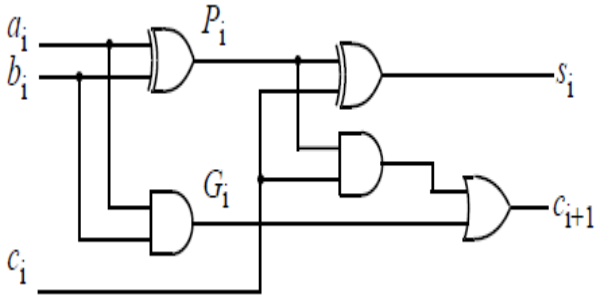

Fig. 2. Full adder at stage i with P_i and G_i shown

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G_i and P_i are called the carry generate and carry propagate terms, respectively. Notice that the generate and propagate terms only depend on the input bits and thus will be valid after one and two gate delay, respectively. If one uses the above expression to calculate the carry signals, onedoes not need to wait for the carry to ripple through all the previous stages to find its proper value.

Let's apply this to a 4-bit adder to make it clear.

Let Ai and Bi be the I bits of the input data and C_{i-1} the carry-in for stage i,the usual method computing the carry-out C_i is

$C_i = G_i + P_i . C_{i-1}$ For i=0,1,2,3…, (1)

Where the generate 'G_i' in a full adder is given by

$G_i = A_i . B_i$ For i=0,1,2,3…, (2)

And the propagate 'Pi' in a full adder is given by

$P_i = A_i$ Xor B_i For i=0,1,2,3…, (3)

Expanding equ(1) The carry is generated by

$C_i = G_i + P_i G_{i-1} + P_i . P_{i-1} G_{i-2} + \ldots\ldots + P_i . P_{i-1\ldots\ldots} P_1 . C_0$ For i=0,1,2,3.., (4)

The sum is generated by

$S_i = C_{i-1}$ Xor A_i Xor $B_i = C_{i-1}$ Xor P_i For i=0,1,2,3.., (5)

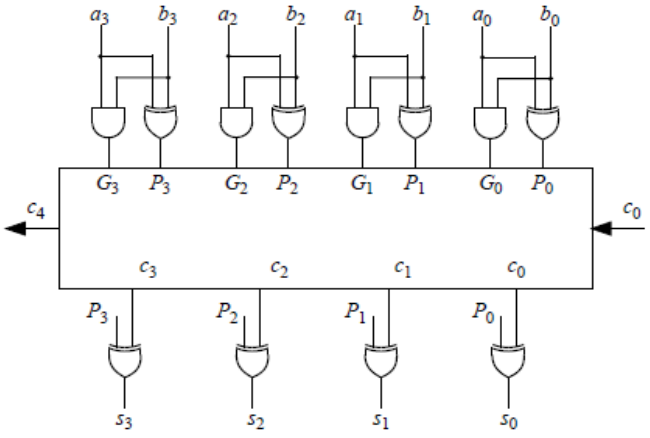

Fig. 3.4-Bit carry lookahead adder implementation detail.

D. *Ripple Carry Adder(RCA):*

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simpleadder and can be used to add unrestricted bit length numbers, it is however not very efficientwhen large bit numbers are used. One of the most serious drawbacks of this adder is that thedelay increases linearly with the bit length. Theworst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated.

$$T=(n-1)t_c+t_s$$

Where t_c is the delay through the carry stage of a full adder, and t_s is the delay to compute the sum of the last stage. The delay of ripple carry adder is linearly proportional to n, the number of bits, therefore the performance of the RCA is limited when n grows bigger. Hence, delay is more as the number of bits is increased in RCA.The advantages of the RCA are lower power consumption as well as compact layout giving smaller chip area.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

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Vol. 2, Issue 11, November

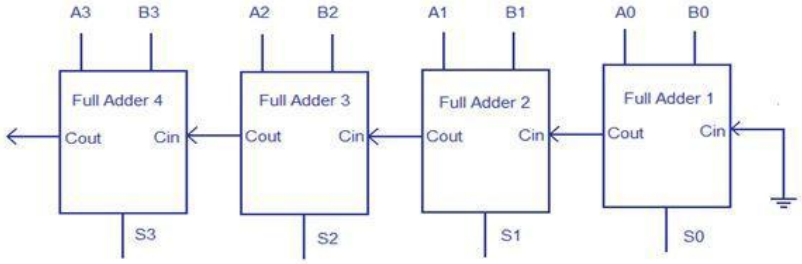

Fig .4. Architecture of ripple carry adder

The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

III. PROPOSED ALGORITHM

A. *Description:*

Quantum Dot Cellular Automata (sometimes referred to simply as quantum cellular automata, or QCA) are proposed models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. Standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Just like any CA, Quantum (-dot) Cellular Automata are based on the simple interaction rules between cells placed on a grid.

A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them. A new bitserial QCA adder has also been proposed , which uses carry feedback and only requires three majority gates and two inverters Two extra electrons are introduced to the quantum cell.As electrons have the ability to tunnel from one quantum dot to the next the repelling force of electrons moves the charge to opposite corners of the quantum cell, resulting in two possible arrangements, representing binary 0 and 1.It uses electrons in cells to store and transmit data.The electrons move between different positions via electron tunneling and the logic functions performed by Coulumbic interactions.

B. *Cell Design:*

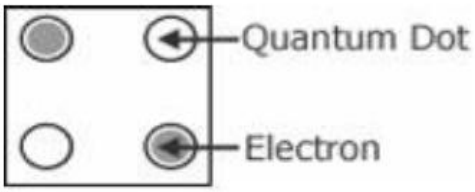

Fig.5. Simplified Diagram of QCA Cell

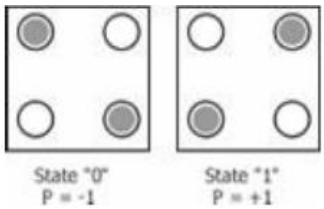

Fig.6. Four Dot Quantum Cell

C. *Structure of Majority gate:*

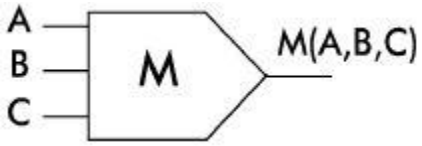

Fig.7. Structure of Majority gate

D. *QCA Majority Gate:*

The QCA majority gate performs a three-input logic function. Assuming the inputs are A ,B and C, the logic function of the majority gate is

$$M = AB+BC+CA$$

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E. *Architecture of Basic Novel 2-bit adder:*

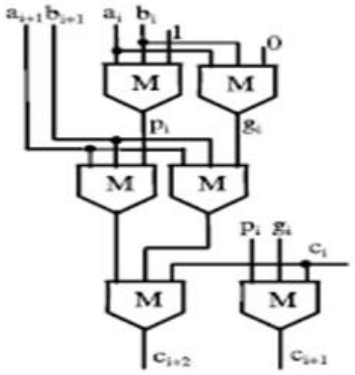
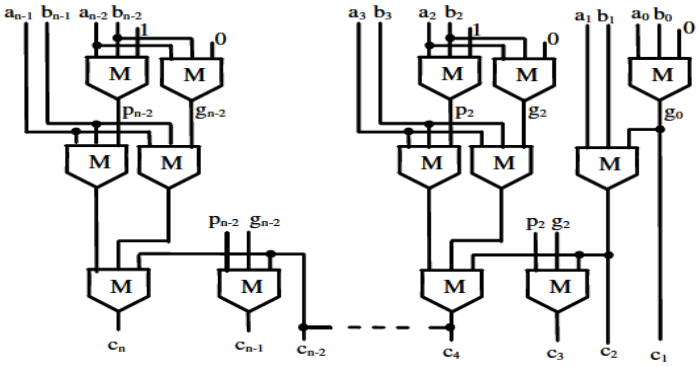
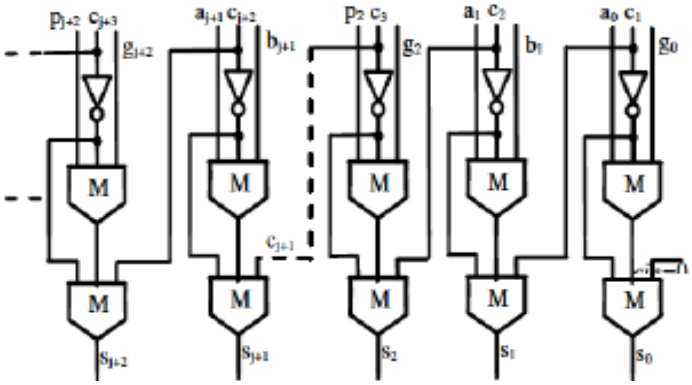


Fig.8. Novel 2-bit basic module.

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and suppose that for the i^{th} bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $P_i = a_i + b_i$ and This article has been accepted for inclusion in a future issue of this journal. $G_i = a_i \cdot b_i$, are computed. *Ci being* the carry produced at the generic $(i-1)^{th}$ bit position, the carry signal C_{i+2},furnished at the $(i+1)$the bit position.



(a)



(b)

Fig. 9. Novel *n*-bit adder (a) carry chain and (b) sum block.

Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

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IV. SIMULATION RESULTS

The proposed addition architecture is implemented for several operands word lengths using the QCA Designer tool [16]adopting the same rules and simulation settings used in [11]–[16]. The quantum-dot diameter is 5 nm; the multilayer wire crossing structure is exploited. Simulations performed on 64-bit adders have shown that the first valid result is outputted after nine latency clock cycles.

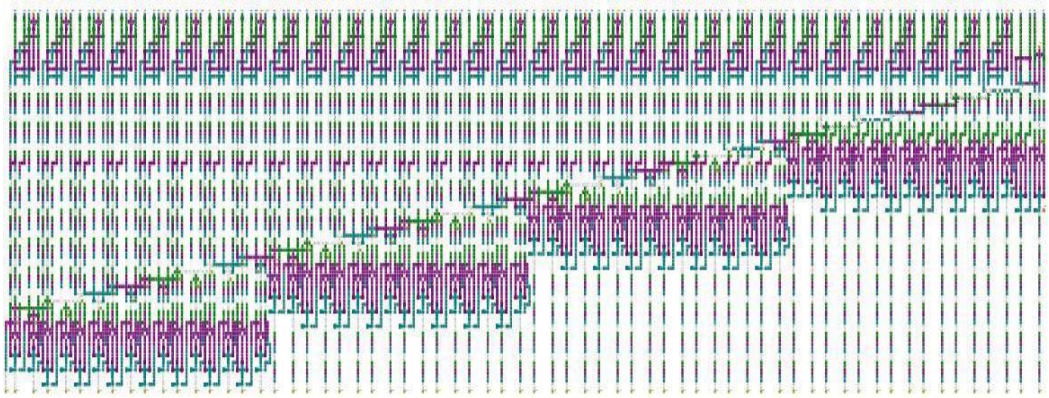

Fig. 10. Novel 64-bit adder.

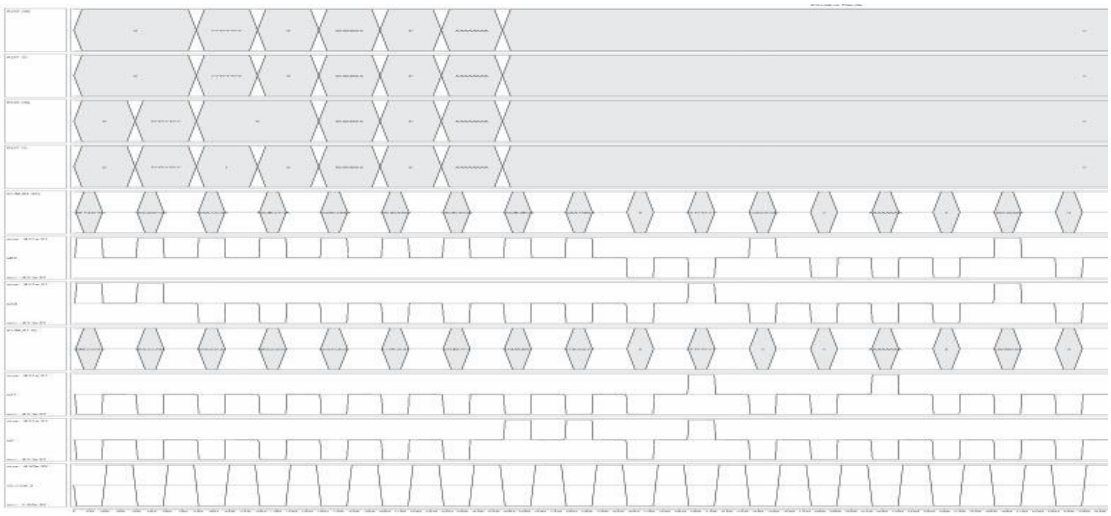

Fig. 11. Simulation results obtained for the novel 64-bit adder.

As an example, the 20 clock phases (or five cycles delay) of the 32-bit adder are as follows: one clock phase is needed for inputs acquisition; the carry $c2$ related to the least significant bit positions is then computed within the two subsequent clock phases;15 phases are required for the carry propagation through the remaining bit positions; finally, two more phases are needed for the sum computation.

Critical path consistencies and post layout characteristics, such as cell count, overall size, delay, number of clock phases, and ADP, are shown in Table II for all the compared adders. The number of cascaded MGs within the worst case computational path directly impacts on the achieved speed performances as an MG always adds one more clock phase.

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ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

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V. CONCLUSION AND FUTURE WORK

The simulation results showed that the proposed algorithm performs better with the total transmission energy metric than the maximum number of hops metric. The proposed algorithm provides energy efficient path for data transmission and maximizes the lifetime of entire network. As the performance of the proposed algorithm is analyzed between two metrics in future with some modifications in design considerations the performance of the proposed algorithm can be compared with other energy efficient algorithm. We have used very small network of 5 nodes, as number of nodes increases the complexity will increase. We can increase the number of nodes and analyze the performance.

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