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Analysis of Current Starved Voltage Controlled Oscillator using 45nm CMOS Technology

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ABSTRACT: An oscillator is an electronic device that used for the aim of generating a signal or waveform. Applications vary from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillators, oscillators' topologies and performance parameters. VCO can be built using many circuit techniques. This paper deals with the design and implementation of Current Starved voltage controlled oscillators (CSVCO) using 45nm CMOS technology. CMOS circuitry in VLSI dissipates less power when static, and is denser than other implementations having same functionality. A VCO is an oscillator, where the control voltage controls the oscillator output frequency. The simulation of CSVCO is done in LT-Spice.

KEYWORDS: CMOS VCO, Current-Starved VCO,LT SPICE IV

I.INTRODUCTION

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits. In a wireless system the quality of the communication link is determined in large part by the characteristics of the VCO and in today's wireless communication systems greater frequency range is required by the VCOs. Traditionally, VCOs using CMOS technology have been used for low frequency applications, but submicron processes have allowed CMOS oscillators to achieve frequencies in the gigahertz range [2]. This range is made possible with the use of automatic swing control. VCO can be built using many circuit techniques [5]. In this paper designing of CMOS VCO using LT spice here current starved VCO is design. Though there are so many design requirements of a VCO, which are phase stability, large electrical tuning range, linearity of frequency verses control voltage, large gain factor, capability of accepting wideband modulation and low cost but the most important factor in designing the VCO is the linearity, on the basis of which the comparison between CMOS VCOs is described [6]. With respect to digital phones that use these circuits, low power consumption, small size and low fabrication costs are important design factors.

II. CURRENT STARVED VCO

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure 1, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of all lower NMOS transistors [4].

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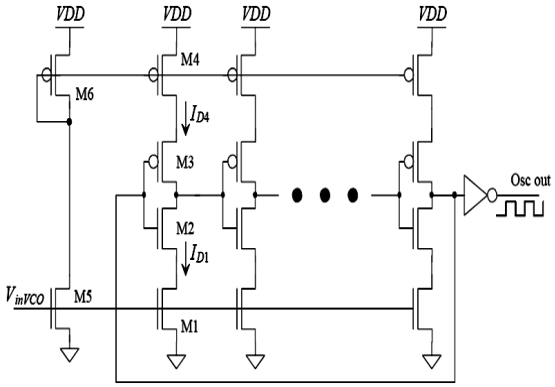

Fig 1. Current-Starved VCO

III. CALCULATING ASPECT RATIO

The drain current of a short channel MOSFET operating in saturation region is given by:

$$I_D = W \cdot v_{sat} \cdot C'_{ox} \cdot (V_{GS} - V_{THN} - V_{DS,sat})$$

From this equation we can write the equation for the width of NMOS, which is given by:

$$\text{Wn} = \frac{I_D}{[\text{Vsat}\cdot\text{Cox}\cdot(\text{Vgs}-\text{Vthn}-\text{Vds,sat})]}$$

Now, BSIM4 MOSFET model Parameters are:

Short-Channel MOSFET parameters VDD=1V and a scale factor of 45nm		
Parameter	NMOS	PMOS
Bias Current, ID	10µA	10µA
VDS,sat and VSD,sat	50 mV	50 mV
VGS and VSG	350 mV	350 mV
VTHN and VTHP	280 mV	280 mV
vsatn and vsatp	110 × 103 m/s	90 × 103 m/s
Tox	14Å	14Å
C'ox	25 f F/µm2	25 f F/µm2

Table 1. Short-Channel MOSFET parameters

By putting the values of these parameters in the equation of Wn, we get the value Wn in 45nm technology, which is given by:

Wn = 180nm

For the Ratio of W/L,

$$(W/L)\ p = 2.5(W/L)\ n$$

Now, we know that the values of L for NMOS and PMOS are same in 45 nm technology, so we get

Lp = Ln = 45nm

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So, the ratio will be

$$Wp = 2.5Wn$$

By putting the values of Wn in above equation, we get

$$Wp = 450nm$$

Finally we get the ratio of W/L for NMOS & PMOS in 45nm technology:

- For NMOS: Wn = 180nm, Ln = 45nm.
- For PMOS: Wp = 450nm, Lp = 45nm

IV. DESIGN OF VCO

To determine the design equations for use with the current-starved VCO, the total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C'_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C'_{ox}(W_p L_p + W_n L_n) \quad \ldots(1)$$

This is simply the output and input capacitances of the inverter. The equation can be written in more useful form as

$$C_{tot} = \frac{5}{2} C'_{ox}(W_p L_p + W_n L_n) \quad \ldots\ldots(2)$$

The time it takes to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}} \quad \ldots\ldots\ldots\ldots\ldots(3)$$

While the time it takes to discharge C_{tot} from VDD to V_{SP} is given by

$$t_2 = C_{tot} \cdot \frac{VDD - V_{SP}}{I_{D1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

If $I_{D4} = I_{D1} = I_D$ (which is labelled as $I_{Dcenter}$ when V_{inVCO} = VDD/2), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = C_{tot} \cdot \frac{VDD}{I_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

The oscillation frequency of the current starved VCO for N (an odd number >= 5) of stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{1}{N \cdot C_{tot} \cdot VDD} \quad \ldots\ldots\ldots (6)$$

The centre frequency (f centre) of the VCO when $I_D = I_{Dcenter}$. The VCO stops oscillating, neglecting sub-threshold currents, when $V_{inVCO} < V_{THN}$. Therefore, $V_{min} = V_{THN}$ and $f_{min} = 0$.

The maximum VCO oscillation frequency, f_{max}, is determined by finding I_D when V_{inVCO} = VDD. At the maximum frequency, V_{max} = VDD.

The output of the current starved VCO normally has its output buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency or lower the gain of the oscillator enough to kill oscillations altogether.

The average current drawn by the VCO is

$$I_{avg} = N \cdot \frac{VDD \cdot C_{tot}}{T} = N \cdot VDD \cdot C_{tot} \cdot f_{osc} \quad \ldots. (7)$$

Or

$$I_{avg} = I_D \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

The average power dissipated by the VCO is

$$P_{avg} = I_{avg} \cdot VDD = VDD \cdot I_D \quad \ldots\ldots\ldots\ldots\ldots (9)$$

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If the power dissipated by the mirror MOSFETs, M5 and M6, is also included then the power is doubled from that given by the equation (9), assuming that $I_D = I_{D5} = I_{D6}$. For low power dissipation I_D should be kept low, or in other words oscillation frequency should be low [4].
We begin by calculating the total capacitance Ctot. Using equation and assuming the inverters, M2 and M3, are sized for equal drive, that is, Ln = Lp = 1,
Wn = 10 and Wp =20, the capacitance is

$$C_{tot} = \frac{5}{2} \cdot 25 \cdot \frac{fF}{\mu m^2} \cdot (20 \cdot 1 + 10 \cdot 1) \cdot (0.045\ \mu m^2) = 1.77 fF$$

Let's use a centre drain current of 10μA based on ID - VGS characteristics of the MOSFETs. The selection of the current is important because when VinVCO is VDD/2, the oscillation frequency to be 1GHz.
The oscillation frequency of the current-starved VCO for N of stages is given by [2]

$$fosc = \frac{I_D}{V_{DD} N C_{tot}}$$

Where, ID = ID3= ID4
N is the number of stages
Ctot is the total capacitance
Vdd is the supply voltage

The number of stages, using equation, is given by

$$N = \frac{I_D}{V_{DD} \cdot C_{tot} \cdot fosc} = \frac{10\ \mu A}{1 \cdot 1.77 fF \cdot 1 GH_z} \cong 5$$

So the number of the design stage is 5.

V. SIMULATION RESULT OF CURRENT STARVED VCO

Functional simulation Of Current Starved VCO is done In LT-Spice software using 45 nm CMOS technology. The five stage CSVCO implementation is shown in figure 2.There are two number of buffers .The tuning range of VCO is from 8Mhz to 7346Mhz.The simulation result of current starved VCO of 5 stage is shown 3.

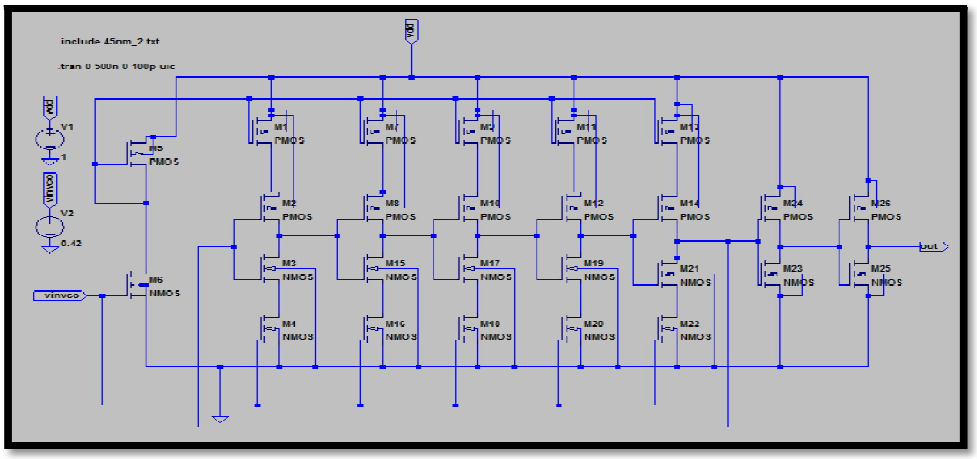

Fig 2. Implimentation of CSVCO.

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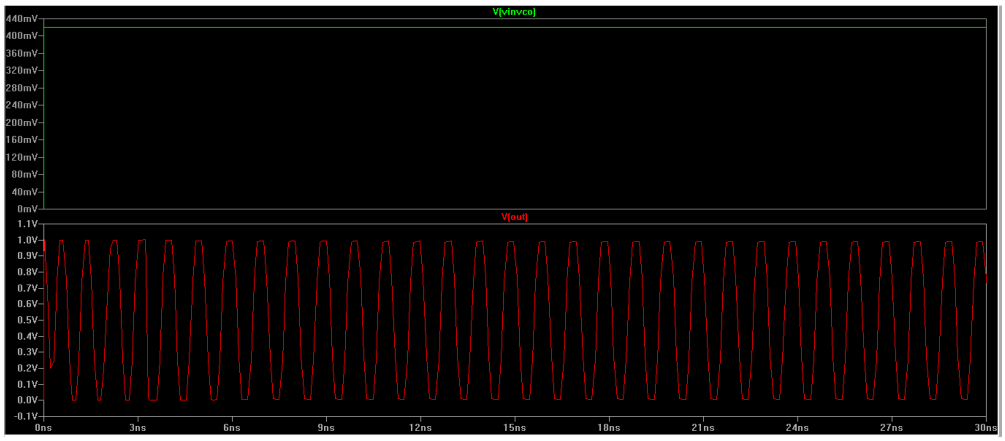

Fig 3. Output Waveform of Current Starved VCO

When we apply control voltage of 0.42v then we get output waveform of central frequency 1Ghz sown in fig 3.Similarly for different control voltage we get different oscillation frequency range from 8 MHz to 7346 MHz is shown in table 2.

Control voltage in Volts	Oscillation frequency in MHz	Control voltage in Volts	Oscillation frequency in MHz
0.1	8	0.6	4476
0.15	20	0.65	4772
0.2	48	0.7	5428
0.25	108	0.75	5930
0.3	232	0.8	6312
0.35	478	0.85	6642
0.4	898	0.9	6952
0.45	1596	0.95	7152
0.5	2518	1.0	7346
0.55	3572		

Table 2. Tuning range of CSVCO

VI.CONCLUSION

In this paper we observed that in current starved voltage controlled oscillator (VCO) generates 1GHz frequency at input control voltage (VinVCO) of 420mV. Since Phase locked loop (PLL) is widely used in wireless communication systems, hence we can generate any desire frequency based on application requirements.The comparative analysis of csvco with the reference paper is show.

Parameter	**Specification (This work)**	**Reference[8]**
Technology (CMOS)	45 nm	100 nm
Center Frequency	1 GHz	1 GHz
Gain (K_{VCO})	3.93 GHz/V	1.531 GHz/V
Tuning range	8 MHz to 7.34 GHz	Not mentioned
Power Dissipation	55.257 µW	432.456 Mw

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