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Cascaded H-bridge Multilevel Inverter Using New Phase Shifted Carrier Pulse Width Modulation Technique

Ch.Lokeshwar Reddy[1], P.Satish Kumar[2], M.Sushama[3]

Dept of EEE, CVR College of Engineering, Hyderabad, India[1]

Dept of EEE, College of Engineering, Osmania University, Hyderabad, India[2]

JNTU College of Engineering, Kukatpally, Hyderabad, India[3]

ABSTRACT: This paper presents a new Phase shifted carrier PWM technique for Cascaded Multilevel Inverter. The main objective of this technique is to reduce the THD of inverter output voltage. This strategy leads to the cancellation of all carrier and associated sideband harmonics up to $2N_c^{th}$ carrier group where $N_c$is the number of H-bridges in a phase. In this modulation process, the switching frequency preferably high to reduce the undesired side effects of discontinuous power flow at switching and to reduce lower harmonics in the output voltage. Comparison of harmonic spectrum for different carrier frequencies and different modulation indexes for a eleven inverter is presented in this paper. This technique can be extended to any number of levels.

KEYWORDS: Cascaded Multilevel Inverter (CMLI), Modulation Index, Phase shifted carrier PWM.

I.INTRODUCTION

Multilevel inverters are finding increased attention in industries for medium voltage and high power applications. Multilevel converters are mainly used to get desired single or three phase voltage waveforms, because of improving waveform of the inverter reduces its harmonic content, the size of the filter used and the level of electromagnetic interference generated by switching operation[1]. The required multi staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra capacitors are the most common independent sources used. Multilevel converters are mainly used for medium and high power applications. There exists three commercial topologies of multilevel inverters; these are Diode clamped multilevel converters (or) Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded Multilevel Inverter (CMLI)[2]. The CMLI appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter [3].

Diode clamped multilevel converters are used in conventional high power ac motor drive applications like conveyers, pumps, fans, and mills. They are also utilized in oil, gas, metals, power, mining, water, marine, and chemical industries. They have also been used in back-to-back configuration for regenerative applications. Flying capacitor multilevel converters have been used in high bandwidth and high switching frequency applications such as medium voltage traction drives. Cascaded multilevel inverters are used where high power and power quality are essential, for example, Static synchronous compensators (STATCOM) and reactive power compensation applications, photovoltaic power conversion, and uninterruptable power supplies. One of the increasing applications for multilevel converter is electric and hybrid power trains.

In this paper Cascaded H-bridge eleven level inverter is modeled for different modulation indexes and different carrier signal frequencies, harmonic analysis is carried out and compared among them. The most preferred PWM technique for Cascaded H-bridge inverters is Phase shifted Carrier PWM [3].

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II. CASCADED MULTILEVEL INVERTERS

In this topology single phase full bridge inverter cells with different dc sources are connected in series. Fig 1 shows the power circuit for three phase eleven level inverter with five cells in each phase and Fig 2 shows the circuit representation of each H-bridge cell. The resulting phase voltage is the addition of voltages generated by the different cells in that phase. Each single phase full bridge inverter generates three voltages: +Vdc, 0, and –Vdc at the output. The output phase voltage swings from -5Vdc to +5Vdc with eleven levels and the resulting waveform is nearly sinusoidal, even without filtering. The number level in phase voltage is 2Nc+1, where Nc is number of single phase inverter cells used in a phase and the number of level in line voltage is 2m-1, where m is the number of levels in phase voltage. CMLI researches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology [5].

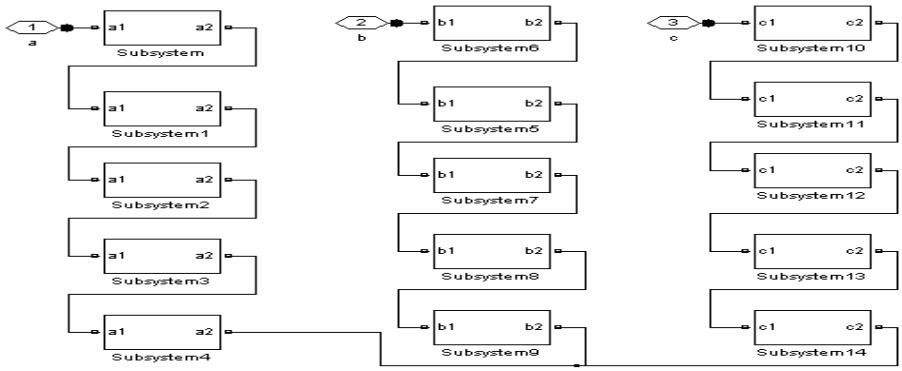

Fig.1. Three phase eleven level Cascaded H-bridge inverter

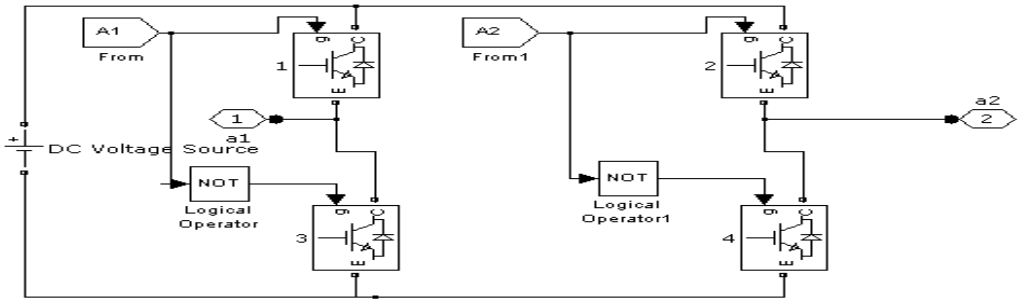

Fig.2. Circuit of each H-bridge cell

III. NEW PHASE SHIFTED CARRIER PWM

Most of the modulation methods developed for multilevel inverters are based on carrier arrangements. The carriers can be arranged with vertical shift (phase disposition-PD, phase opposition disposition-POD, and alternative phase opposition disposition-APOD), or with horizontal displacements (phase shifted carrier PWM)[6]. For the cascaded inverter, phase shifted carrier PWM is the most common strategy with an improved harmonic performance, it offers an evenly power distribution across all cells and it is very easy to implement independently for the number of inverters[7]. In this approach, the carriers shifted by an angle $360^0/N_c$ (where N_c is number of single phase inverter cells used in a phase leg). This strategy leads to the cancellation of all carrier and associated sideband harmonics up to $2N_c^{th}$ carrier group[8]. The modulation index is always multiples of three to have symmetry in the output voltage. The switching frequency preferably should be high, to reduce the undesired side effects of discontinuous power flow at switching and

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to reduce lower harmonics in the output voltage. Fig.3. shows the half cycle of sinusoidal reference and carrier signals for eleven level PWM operation.

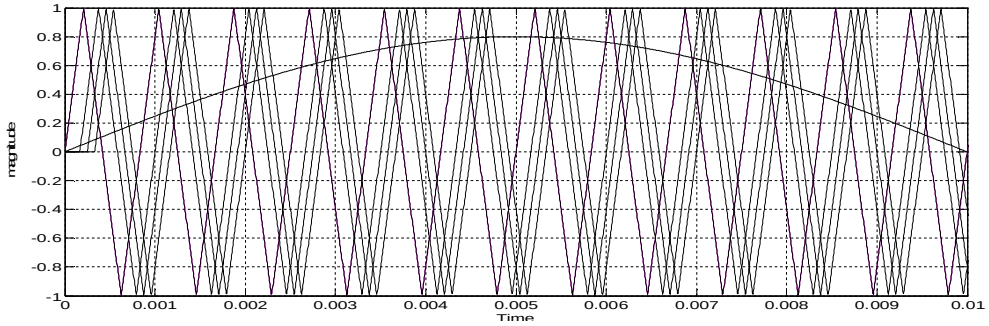

Fig.3. Carrier and reference waveform arrangements (Half cycle only) for a eleven level phase shifted carrier strategy

IV.SIMULATION AND RESULTS

The eleven level CMLI was simulated with RL load, and the DC voltage given is 100V. Fig 4 shows the circuit arrangement for eleven level CMLI with PWM generator. Fig 5 shows the generation of phase shifted carrier PWM signals for one phase. The simulation was done for 900Hz and 1200Hz carrier frequencies, and for modulation indexes M=0.8 and M=1.

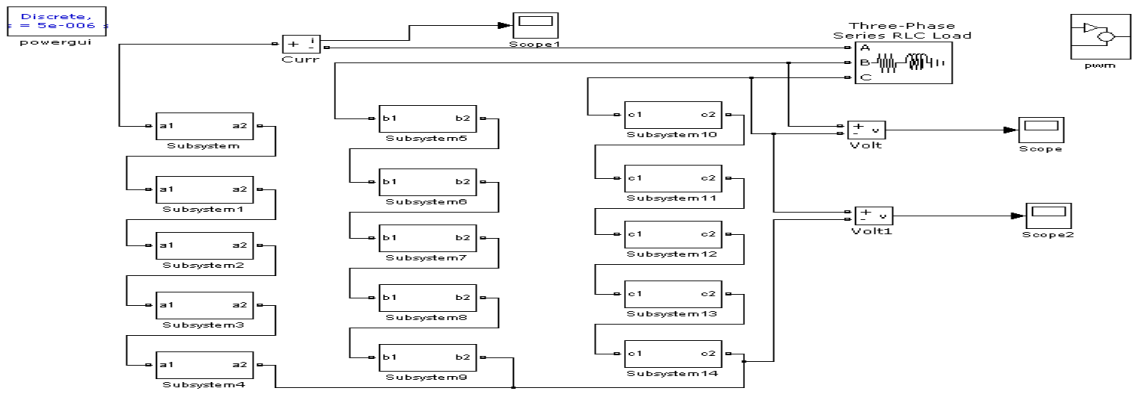

Fig.4. Eleven level Cascaded H-bridge Multilevel Inverter

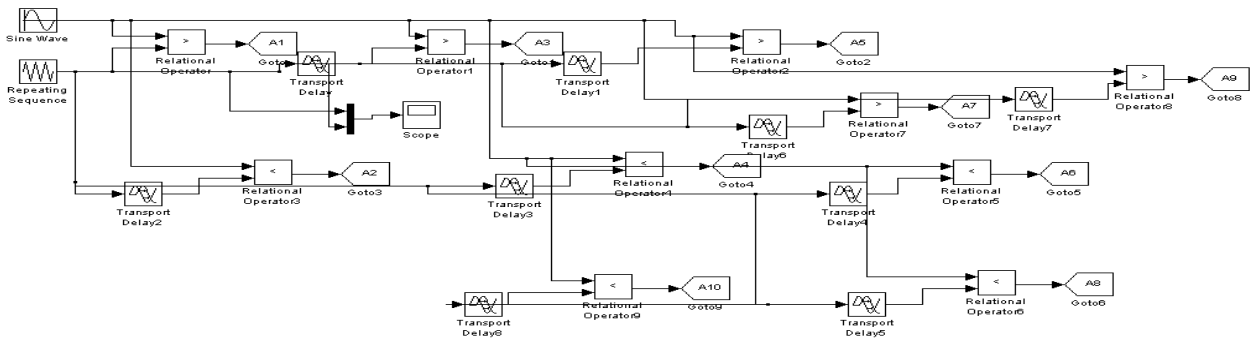

Fig.5. Circuit model to generate phase shifted carrier PWM signals (one phase) for eleven level CMLI

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Fig 6 and Fig 8 shows the output Line and phase voltages of eleven level CMLI and Fig 7 and Fig 9 shows the corresponding FFT analysis, with modulation index M=0.8 and carrier frequency Fc=1200. From the Fig 7 and 9 all the carrier and associated sideband harmonics up to 2Ncth carrier group i.e up to 12 kHz frequency was cancelled. It was due to the phase shifted PWM strategy. And also the peak value of phase voltage is M*Nc*Vdc it can verified from the Fig 8.

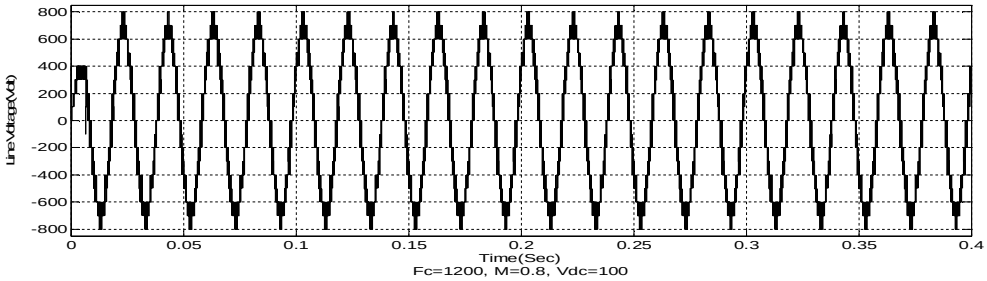

Fig.6. Eleven level CMLI output line voltage with M=0.8 and Fc=1200

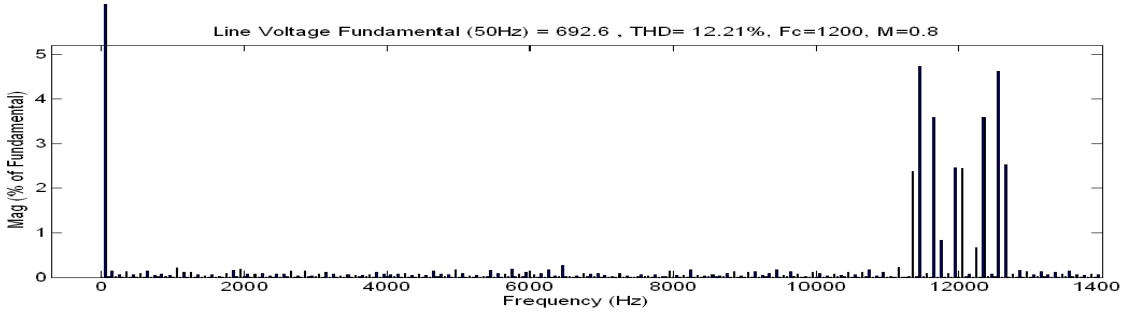

Fig.7. FFT analysis of Eleven level CMLI output line voltage with M=0.8 and Fc=1200

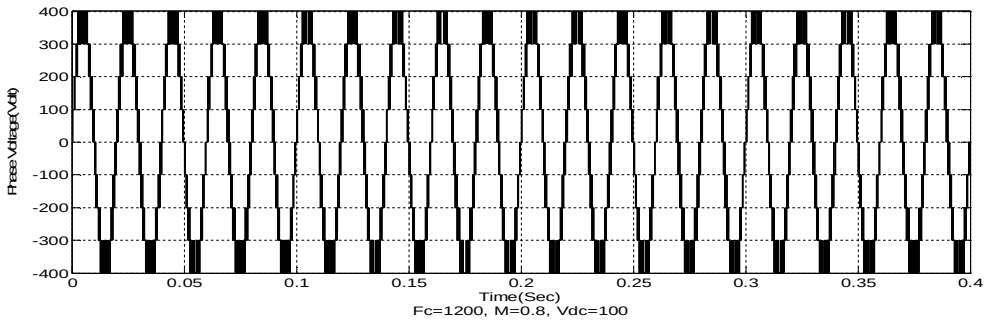

Fig.8. Eleven level CMLI output Phase voltage with M=0.8 and Fc=1200

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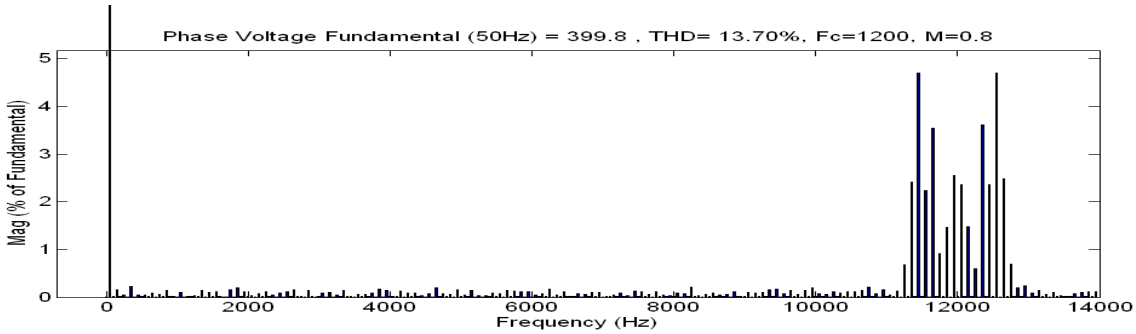

Fig.9. FFT analysis of Eleven level CMLI output Phase voltage with M=0.8 and Fc=1200

Fig 10 and Fig 12 shows the output Line and phase voltages of eleven level CMLI and Fig 11 and Fig 13 shows the corresponding FFT analysis, with modulation index M=1 and carrier frequency Fc=1200. From the Fig 11 and 13 all the carrier and associated sideband harmonics up to $2N_c^{th}$ carrier group i.e up to 12 kHz frequency was cancelled. It was due to the phase shifted PWM strategy. And also the peak value of phase voltage is $M*N_c*V_{dc}$ it can verified from the Fig 12.Peak value of phase and line voltages are increased if the modulation index is increased.

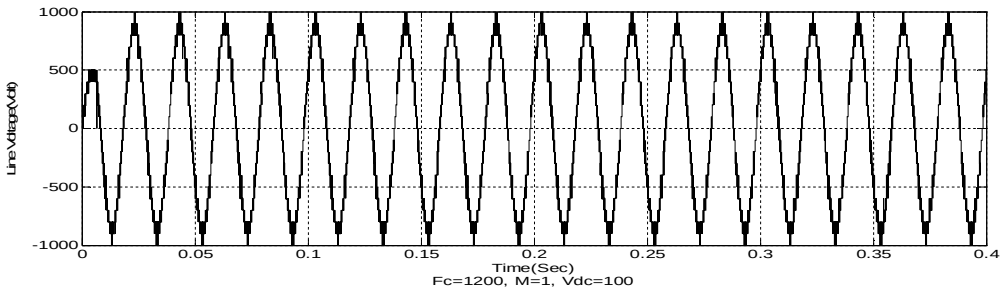

Fig.10. Eleven level CMLI output line voltage with M=1 and Fc=1200

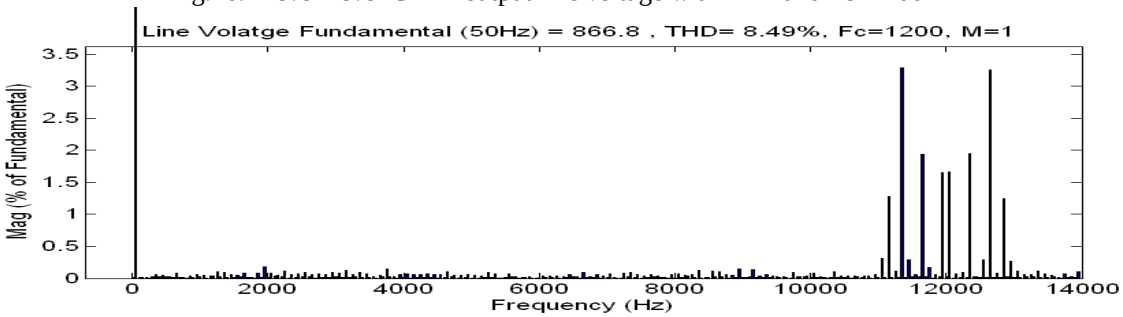

Fig.11. FFT analysis of Eleven level CMLI output line voltage with M=1 and Fc=1200

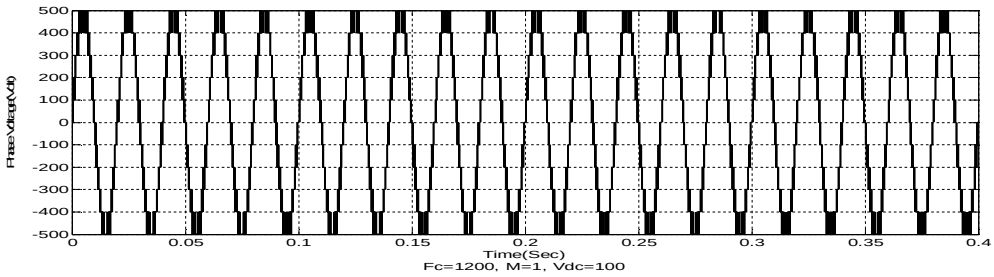

Fig.12. Eleven level CMLI output Phase voltage with M=1 and Fc=1200

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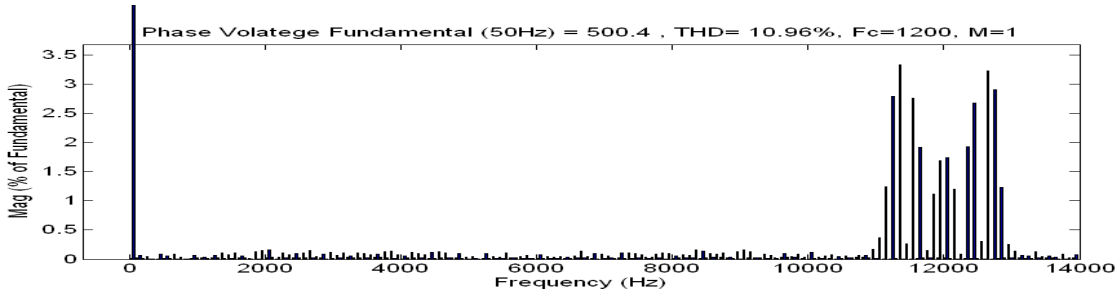

Fig.13. FFT analysis of Eleven level CMLI output Phase voltage with M=1 and Fc=1200

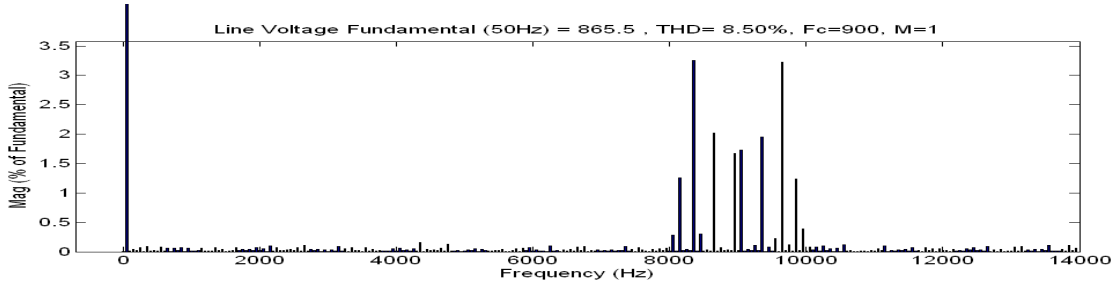

Fig.14. FFT analysis of Eleven level CMLI output line voltage with M=1 and Fc=900

Fig 14 and 15 shows the FFT analysis of line and phase voltages for modulation index M=1 and the carrier frequency Fc=900 Hz. It is observed that from the FFT analysis of line voltages and phase voltages, the total harmonic distortion is reduced if the frequency for carrier signals is increased. Fig 16 shows the FFT analysis of phase voltage for modulation index M=0.8 and carrier frequency Fc=900.

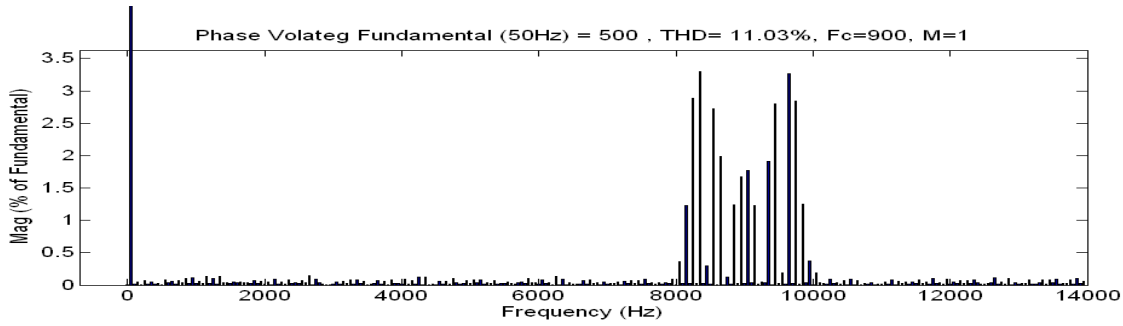

Fig.15. FFT analysis of Eleven level CMLI output Phase voltage with M=1 and Fc=900

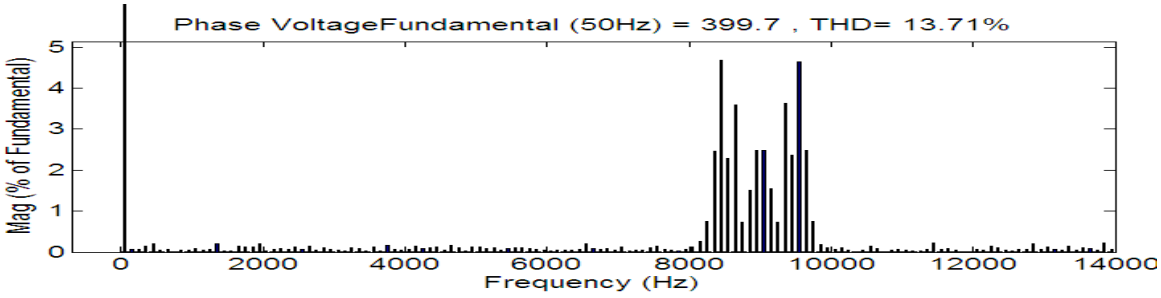

Fig.16. FFT analysis of Eleven level CMLI output Phase voltage with M=1 and Fc=900

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Fig 17 shows the load current for modulation index M=1 and carrier frequency Fc=1200, and Fig 18 shows FFT analysis of the load current. It is observed that the load current seen almost sinusoidal wave and the harmonics it consists of is very low. Table 1 shows the comparison of output voltage THDs for different carrier frequencies and different Modulation indexes.

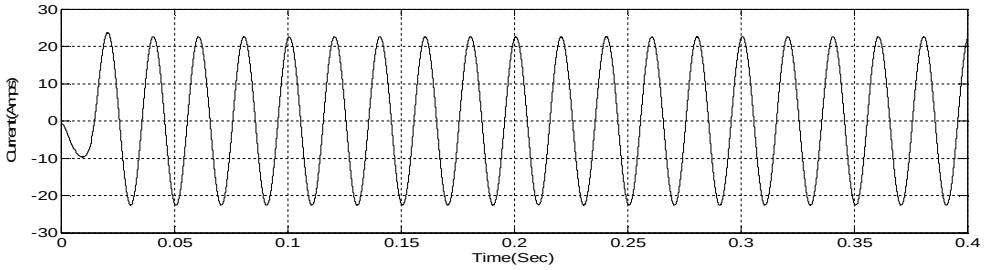

Fig.17. Eleven level CMLI output load current with M=1 and Fc=1200

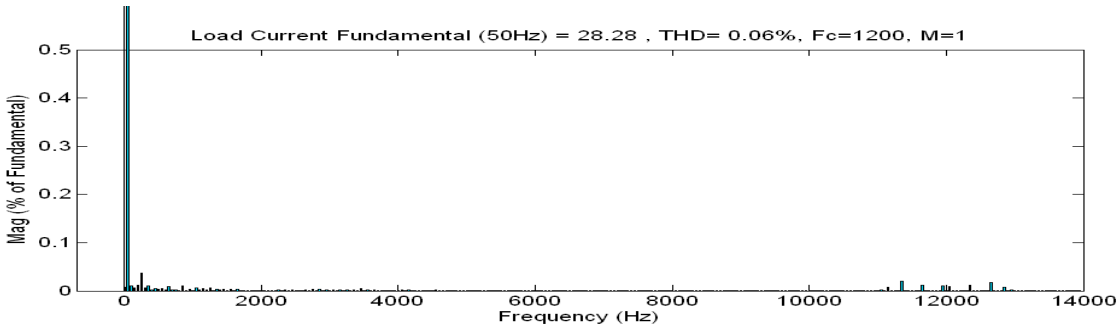

Fig.18. FFT analysis of Eleven level CMLI load current with M=1 and Fc=1200

S.No	Carrier Frequency(Fc)	Modualtion Index(M)	%THD (Phase Voltage)
1	1200	0.8	13.70
2	1200	1	10.96
3	900	0.8	13.71
4	900	1	11.03

Table 1. Comparison of results

V.CONCLUSION

Eleven level CMLI connected with RL load was simulated by using new phase shifted carrier PWM technique. The results were compared and shown in Table 1 for different carrier frequencies and for different modulation indexes. The total harmonic distortion was reduced by increasing carrier frequency. In this method the carrier frequency should always be high. In this technique the lower order harmonics were gets cancelled up to the $2N_c^{th}$ carrier group. This technique can be increased to any number of levels but to implement practically the number of components and cost is increased

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