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# Characteristic Comparison and Improvement of 3D Multi Gate FINFETS

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**ABSTRACT**— In this paper the characteristic parameters such as threshold voltage, drain currents ($I_{ON}$ and $I_{OFF}$), sub threshold slope of 3-Dimensional SOI Double Gate FINFET, Tri- gate FINFET and Independent Gate FINFET are evaluated with the help of TCAD. Drain currents are optimized by using high-K dielectric and analyzed over different gate lengths. The threshold voltage of these three devices are analyzed using various gate materials of different work functions consequently minimize the short channel effects. It also highlights the electrostatic control on channel by increasing the number of gates.

**KEYWORDS-**
Dimensional,SOI,Multigate,ShortChannel effects,High-k Dielectrics.

## I. INTRODUCTION

Three-dimensional SOI(silicon-on-insulator) devices with multiple gates (double,triple,pi. **π**-gate, **Ω**-gate,GAA(gate all around) etc) are evolved from from classical, planar, single-gate devices due to the increasing need for higher current drive and better short-channel characteristics[1] . The current drive of a double-gate device is twice that of a single-gate transistor with same gate length and width because current drive capability of multiple-gate depends on the total gate width[1]. In case of reduced short channel effects (SCEs), higher current drivability, nearly ideal subthreshold swing (SS), and mobility enhancement,Multi-gate devices are promising structures [4],[5] In multi-gate devices the FINFET is most suitable structure because it can have simple self-aligned DG and TG structure with good process compatibility and easier thickness control of fin body.

The structural difference between DG(double gate) FINFET and Tri-gate FINFET is that the gate oxide layer in DG FINFET is thicker at the top portion of fin so that only two gate remains effective for the channel control. The tri gate FINFET provides a symmetric device architecture where the channel is controlled by gate from three sides of the Si film. Since the gate control is increased, the scaling of Si film thickness in Tri-gate FINFET is better implemented as compared to DGFINFET. In IG(independent gate) FINFET the two gates are independent unlike In DG and TG FINFET the gates are electrically connected. To avoid poly depletion problem of polysilicon gate, metal gates are used in every device. It increases carrier mobility by reducing the transverse electrical field at a given gate overdrive.

## II. DEVICE STRUCTURE AND DIMENSIONS

To study the characteristics variation of Multi-gate SOI FINFET ,devices are simulated using tcad simulator .3-D simulations have been performed for a wide range of proposed technology nodes (Table 1) with proportional device dimensions and dielectric values to meet the requirements of ITRS[12].

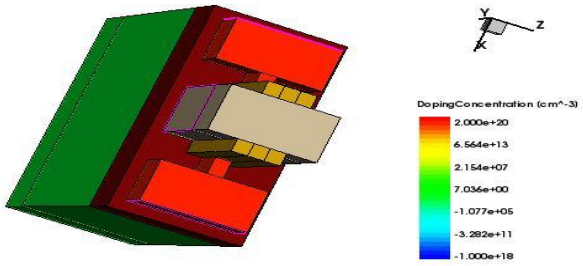


Fig -1(a) 3D Double or Tri-gate FinFET structure

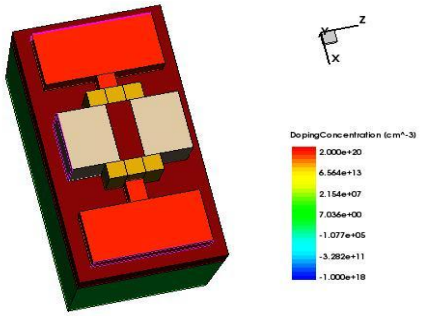


Fig-1(b) 3D Independent Gate FinFET structure

Here in this structure gate is available for the channel more than one side, so control over the channel is increased, while

for drain side control remains same in case of short channel. Buried oxide thickness is maintained sufficient in order to decrease SCEs. Extended source/drain is doped highly to minimize series resistance[10].

TABLE I
SPECIFICATIONS USED FOR 3-D FINFET DEVICE SIMULATIONS

| | | | |
|---|---|---|---|
| $V_{dd}$ | 1 Volt | $W_{fin}$(Fin width) | 6 nm |
| Channel doping($cm^{-3}$) | 1e+18 | $H_{fin}$(Fin height) | 14 nm |
| DRAINS/SOURCE Doping($cm^{-3}$) | 1e+20 | $t_{ox}$ (Oxide thickness) | 1 nm |
| Gate oxide | $SiO_2$/ $HfO_2$ | Spacer length | 8 nm |
| N type dopant | arsenic | P type dopant | boron |
| Gate contact material | metal | thickness SOI isolation | 20 nm |

## III. DEVICE SIMULATON AND RESULTS

Here TCAD simulation tool is used for characteristic comparison of Double gate(DG), independent double gate(IG) and Tri-gate FINFET by using high-k material and varying gate length.

### *A.Imact Of High-K Dielectric*

Keeping the oxide capacitance constant, if we replace SiO2 with HfO2, the physical oxide thickness will scale up almost 5 times, which improves the leakage characteristics of the device. For the simulations in this section, SiO2 (k=3.9) thickness was selected as 1.0nm and HfO2 (k=22) thickness was selected as 6.0nm.

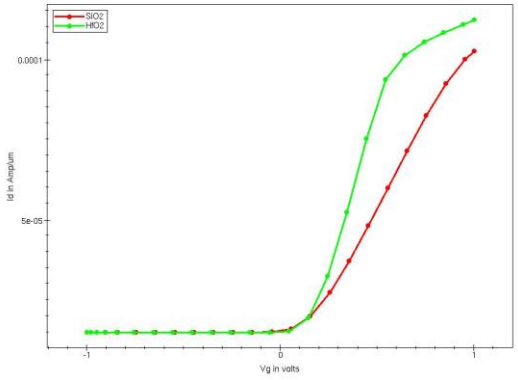


Fig-2 Drain current($I_d$) Vs Gate voltage ($V_g$) of FinFET using different gate oxide

It is clear that with increase in physical gate oxide thickness, gate gradually loses control over the channel and hence $V_T$ decreases as we replace SiO2 with HfO2. As a result, $I_{off}$ and $I_{on}$ increases and if we gradually change k value from 3.9 to 40, it can be noticed that $I_{off}$ shows an exponential increase whereas Ion shows a linear increase with increasing values of k [7]. Degradation of subthreshold slope is observed as we increase the k value and are given in table-2. This behavior is due to the presence of increased fringing fields near the source junction .

| **material** | **k** | **$I_{ON}$(A)** | **IOFF(A)** | **ION/ IOFF** | **VT volts** | **SS mV/dec** |
|---|---|---|---|---|---|---|
| $SiO_2$ | 3.9 | 1.01E-4 | 7.45 E-13 | 1.35 E-8 | 0.196 | 72.07 |
| $HfO_2$ | 22 | 2.29E-4 | 5.78 E-13 | 3.9 E-8 | 0.167 | 78.06 |

Table.2: Device performance parameters obtained for simulations with $SiO_2$ and $HfO_2$ as dielectrics of 25 nm DG FinFET

### *B.Varying Channel Length*

Here DG FinFET devices are simulated across different channel lengths using TCAD.The result curves are showing in figure-3(a), 3(b).Similarly the same is done for TG FinFET and IG FinFET devices.

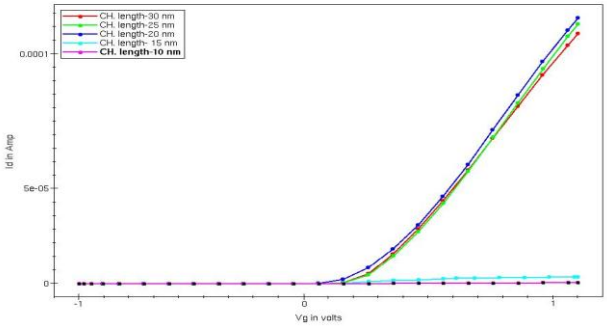


Fig-3(a) Drain current(Id) Vs Gate voltage (Vg) of $SiO_2$ gate oxide DG FinFET varying channel length.

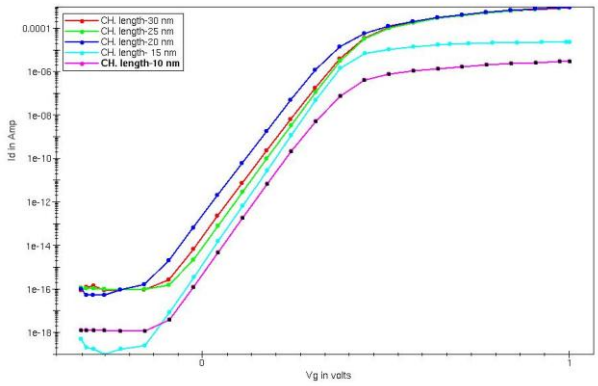


Fig-3(b)logarithmic drain current variation of Figure-3(a)

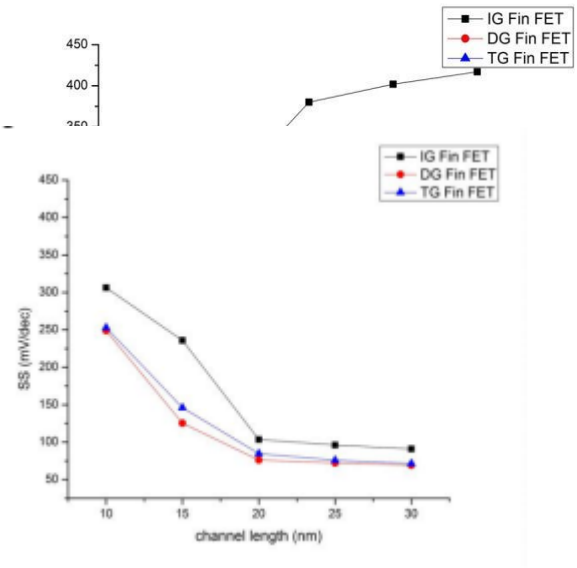


Fig-3(c)Threshold Voltage($V_T$) over different channel lengths for 3D FinFETs

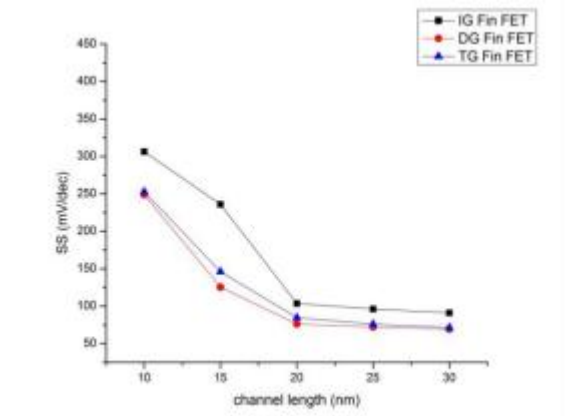


Fig-3(d)Subthreshold Swing(SS) over different channel lengths of 3D FinFETs

In the above $V_T$ is higher for IG FinFET because more one gate lateral electric field is acting simultaneously in case of DG FinFET and TG FinFET, which drives the current for lower value of potential.For scaling down the channel length drain induced barrier lowering occurs, so lesser values of Vg drain current Id changes more. Hence SS is more for shorter channels. IG FinFET has more subthreshold swing values because lesser control over channel due to two gates are different potential, sometimes one is higher potential and another at zero potential looking as single gate device.

## IV.C ONCLUSION

For DG FinFET and TG FinFET, the subthreshold slope is almost constant over the range of 20nm to 30 nm channel length.In this way we can easily control the short channel effects and current drivecapability with suitable threshold voltage though $V_T$ is lesser than IG FinFET. Drain current increases for high-k dielectric $HfO_2$,but in case of $V_T$ and subthreshold swing,SiO2 is showing better results. Moreover $SiO_2$ material is more compatible with fabrication technology.

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