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CMOS Design, Simulation and Physical Design of a Two Channel Demodulator

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ABSTRACT:In this paper, we present a two channel direct demodulator design for differential signals. The two-channel demodulator accepts two independent input signals in a differential mode and demodulates to provide a filtered DC output. Based on analog multiplexer (AM) select pin, one channel is selected out of 2 channels for the differential signal (v1,v2) processing. Demodulator section consists of precision full wave rectifier (PR), 2nd order Butterworth low pass filter (AF), and summing & difference amplifiers (SA & DA).The Filtered outputs are added, subtracted & amplified to get -(v1+v2) & (v2-v1) outputs respectively which are of bipolarities. This finds applications in processing signals from differential transformers. The mentioned method of demodulation is much superior to that of synchronous demodulation on parameters of noise performance, phase error, additional clock, components count and accuracy.

KEYWORDS:CMOS amplifiers, Rectifiers, Filters, AnalogLayout

I.INTRODUCTION

The block diagram of the proposed 2-channel demodulator is as shown in Figure-1. It basically consists of analog multiplexer, operational amplifier, precision rectifiers, active filters,summing and difference amplifiers.Circuit design& simulation of modules were carried and characterized with Cadence Tool. All the modules were integrated and full functionality were verified with the specification as given in Table 1. Layouts of the design completed and verified with Calibre tool.

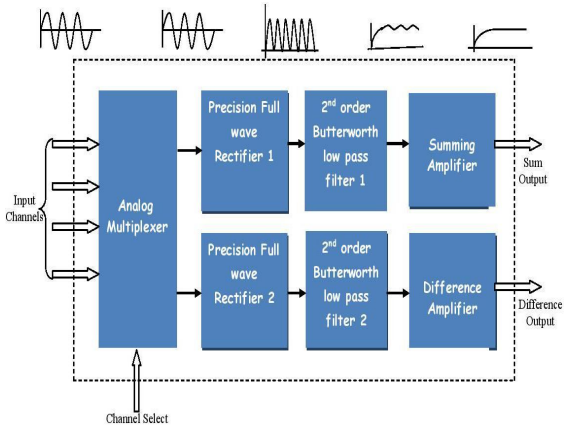

Figure 1.Block Diagram of a 2-channel demodulator

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parameters	value
Supply Voltage	±5V...±10 %(tolerance)
Input Voltage Range	-4V to +4V
Temp. Range	-55°C to 125°C
Supply Current	20mA
Output Impedance	200Ω
Output Offset Voltage	$\pm 15mV_{dc}$
Output Current	500µA
Difference Output	±3.88V
Summer Output	±1.48V
Frequency of Operation	3.4KHz
Digital Inputs	CMOS/TTL

Table 1: Specifications of a 2- Channel Demodulator

II. LITERATURE SURVEY

Mike Donnelly [1] presents a systematic process for developing and examining of Simulink models for Inductive Displacement Transducer (IDT) and signal conditioning circuit. This paper presents a Simulink model based on dual half-wave rectifiers was developed to simulate the behaviour of the signal conditioning circuit. The results of simulation clearly demonstrate the sensitivity and performance at frequency around 4.8KHz.This technique was used in designing an ASIC based demodulator. R.A. Williams [2] and Z.Z. Yu [3][7][8][9] clearly discuss the inductive based imaging and tomographic process for industry which employed the inductive sensing and signal conditioning. Richard Poley [6] in Texas application notes writes about the practical signal conditioning techniques and characteristics of every component in LVDT measurement. This paper also suggest the various means of error correction techniques both hardware and software to improve the sensitivity of the system.

III.CIRCUIT IMPLEMENTATION

Op-Amp: Due to high gain and high output swing requirement, a 2-stage op-amp had been chosen. The Op-amp has PMOS input differential pair as the 1st gain stage& common source amplifier as 2nd gain stagewith frequency compensation. Cascoded current mirror biasing circuit is used to bias multiple circuits of a 2-stage op-amp. The design specification of the 2-stage op-amp specification is given in Table -2. A schematic diagram is presented in Figure-2 which shows the final design. This circuit is designed especially for low output impedance(~200Ω).The op-amp characteristics such as gain & phase ,slew rate , CMRR ,PSRR ,output swing, output impedance,quiescent current were measured & observed to be as shown in the Table-2. Same op-amp is used for few more blocks in this project.

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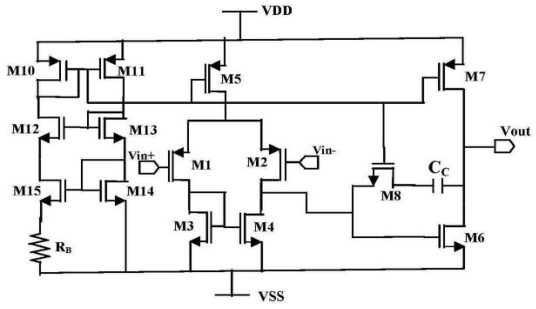

Figure-2: Schematic of a 2-stage Op-Amp

AnalogMultiplexer: Analog Multiplexer consists of two 2:1 multiplexers with selection logic. Multiplexersare implemented by designing Analog CMOS switches in Transmission Gates (TG) principle. TG provides low ON resistance, less distortion & loss. Op-amp buffer is used at the output of AM to avoid loading effect. Buffers are used for level shifting supply voltage levels from 0&5v to ±5v.Decoderconsists of minimal number of gates& decides which channel to be selected depending on the channel select pin. The characteristics such as rise time,fall time & propagation delay were measured.

Precision Rectifiers: Full Wave precision rectifieris implemented using op-amps whichcancel the forward voltage drop of the diode. So very low level signals (well below the diodes forward voltage) can still be rectified with minimal error. Full Wave precision rectifierprovides a better efficiency (81%).Characteristics of a full wave precision rectifiersuch as ripple factor, form factor were measured.

Parameters	Specifications	Simulated Result
Open loop gain	60dB	76.30dB
CMRR	>50dB	63.50dB
PSRR	60dB	76.30dB
DC offset voltage	±15mV	717.85µV
Slew Rate	5V/µs	5.438V/µs
Output voltage Swing	±4.5V	±4.63V
Distortion		32.05mV
Output Impedance	200Ω	174.70 Ω
Quiescent Current		±1.79A

Table-2: Specifications of 2-Stage Op-Amp

Active Filters: 2ndorder low pass butter worth filter provides maximally flat pass band response & less ripple (~38mv). 2nd order low pass butter worth filter characteristics such as gain, roll off, cutoff frequency, quality factor etc were designed for the specified input signals.

Summing amplifier & Difference amplifier: The summing amplifiers have been designed with the consideration that the amplifier operates in the linear region even at the maximum output swing. The difference amplifier subtracts the filtered v1 and v2 DC signal. (This difference signal provides magnitude information with polarity). The circuit has been designed with very low input offset to reduce the offset component in the output. The sum & difference outputs fordifferent input voltages were measured & plotted to be as shown in the Table-3.

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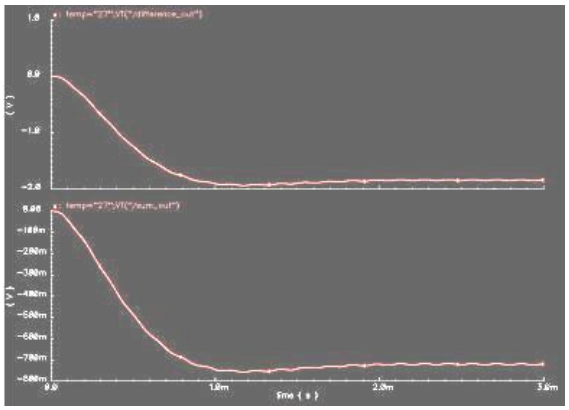

Graph.1.: Summing & Difference output

Peak Voltage(Vp)	Vdiff(Theory)	Vdiff(Practical)	Vsum(Theory)	Vsum(Practical)
0.5v	-451.1mv	-459.7mv	-181.7m	-180.2mv
2v	-1.8044	-1.85	-726.8m	-724.9m
4v	-3.6088	-3.708	-1.4536	-1.454
0v(offset)	0	-25.01n	0	-1.968u

Table-3: Simulated results of 2-Channel Demodulator

The graph 1. shows the output of low pass filter after the summer and difference amplifier. It is seen that there is a small difference in theoretical and practical values which is mainly due to the offset voltage of the operational amplifier which in the range of 25nV to 1.7 micro volts in difference amplifier and summer respectively. In spite of this the system delivered output with noise margin less than -33mv.

IV.ANALOG LAYOUT IMPLEMENTATION

Following are the analogue layout techniques that were implemented in this project: Matching Antenna effect, Electro migration, Electrostatic Discharge, Guard Ring, GDSII conversion, Bond Padding, floor plan etc. Design Rule Check(DRC) & layout versus schematic (LVS) are the two verification steps that were carried out using standard EDA tools. The complete layout is as shown below.

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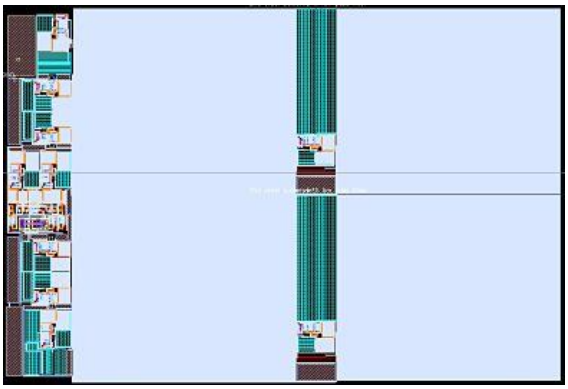

Figure-3: Complete Layout

V.CONCLUSION

A 2-channel demodulator for LVDT measurement with low ripple and low offset was design, the design process undertaken was discussed, and the resulting simulation and analysis were presented. It is seen that the resulting ASIC design matched the design specifications.

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