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Comparative Analysis of THD in Symmetrical and Asymmetrical Cascaded H-Bridge Seven Level Inverter

M.S.Sivagamasundari[1], Dr.P.Melba Mary[2], N.K.Jawahar Muthu[3]

Assistant Professor , Department of EEE,V V College of Engineering,Tisaiyanvilai, Tamilnadu, India[1]

Principal , Department of EEE,V V College of Engineering,Tisaiyanvilai, Tamilnadu, Indi [2]

Assistant Executive Engineer, Tamilnadu Electricity Board, Tamilnadu, India [3]

Abstract: – In this paper , the performance of symmetrical and asymmetrical single phase cascaded h-bridge seven level inverter with respect to harmonics content and voltage stress across the switch with photovoltaic cell as its input source is simulated by using MATLAB/Simulink. Multicarrier pulse width modulation control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage. Hence we could achieve the improved efficiency of the system The simulated output shows very favorable result.

Keywords: Multilevel inverter, Cascaded H-Bridge inverter, Total Harmonic Distortion, Photovoltaic cell

1. INTRODUCTION

Recently multilevel inverters have become more attractive to researchers and industrial companies due to fast developing of high power devices and related control techniques.[1]

The recent advancement in power electronics has initiated to improve the level of inverter to cater to the need of medium voltage high power applications without transformer. These converter topologies can generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental. It significantly reduces the harmonics problem with reduced voltage stress across the switch.[2]

The importance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and with less THD. Numerous topologies have been introduced and widely studied for utility of non conventional sources and also for drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and in drive systems[3].

The multilevel inverter is a promising inverter topology for high voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a stepped AC output that approaches the pure sine waveform. It has the advantages like high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and switching losses, higher efficiency, reduction of dv/dt stresses etc. It gives the possibility of working with low speed semiconductors in comparison with the two-level inverters. Numerous of MLI topologies and modulation techniques have been introduced. But most popular MLI topology is Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI). In this paper we are using a CMLI that consist of several H-Bridge inverters with equal and un-equal DC sources named as Symmetrical and Asymmetrical type Cascaded Multilevel Inverter [4].

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II. PHOTOVOLTAIC CELL

A Photovoltaic cell is a device used to convert solar radiation directly into electricity. It consists of two or more thin layers of semiconducting material, most commonly silicon. When the silicon is exposed to light , electrical charges are generated.[5] A PV cell is usually represented by an electrical equivalent one-diode model shown in fig.1.

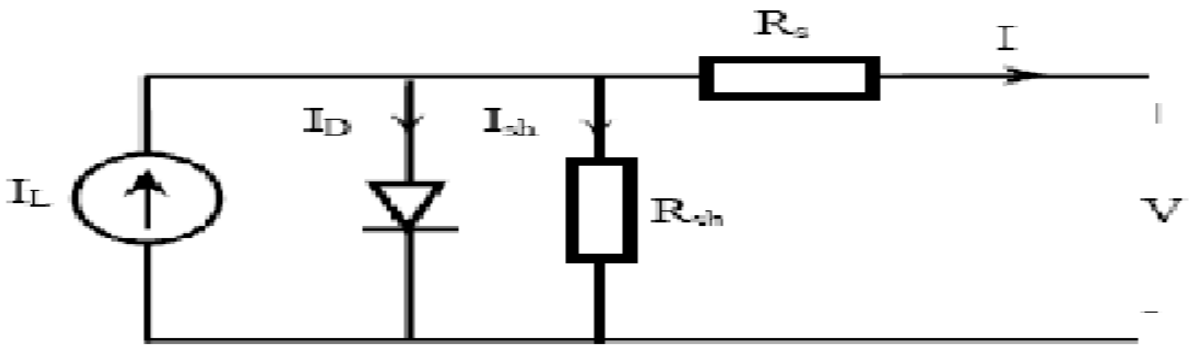

Fig. 1. Single PV cell model

The model contains a current source, one diode, internal shunt resistance and a series resistance which represents the resistance inside each cell. The net current is the difference between the photo current and the normal diode current is given by the equation.[6].

$$Id = Io\ [e^{\frac{q(V+IRs}{KT}} -1] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$I = I_L - I_o[e^{\frac{q(V+IRs}{KT}} -1]-\frac{V+IRs}{Rsh} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where

I is the cell current (A).
q is the charge of electron (coul).
K is the Boltzmann's constant (j/K).
T is the cell temperature (K).
I_L is the photo current (A).
Io is the diode saturation current.(A)
Rs , Rsh are cell series and shunt resistances (ohms). V is the cell output voltage (V).

III. ASYMMETRICAL CASCADED H-BRIDGE INVERTER

Asymmetrical Cascaded H-Bridge Inverter consists of a series connection of multiple H bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. Each H bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage

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waveform is produced. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of bridges as shown in equation.

If ACMLI has N no. of H-Bridges,

The output voltage could be expressed as ; $Vo(t) = Vo1(t) + Vo2(t) + ... + Vo\,N(t)$ (1)

Where, $Vo1(t)$,$Vo2(t)$, ... $Vo\,N(t)$ are the output of individual H-bridge.

In ACMLI DC voltage with ratio binary and ternary are the most popular. In binary progression within H-Bridge inverters , the DC voltages having ratio 1: 2: 4: 8. . : 2N and the maximum voltage output would be (2^N-1) V dc and the voltage levels will be $(2^{N+1}-1)$. While in the ternary progression the amplitude of DC voltages having ratio 1: 3: 9: 27. . : 3N and the maximum output voltage reaches to $((3^N- 1)/2)$ V dc and the voltage levels will be(3^N) .[7]

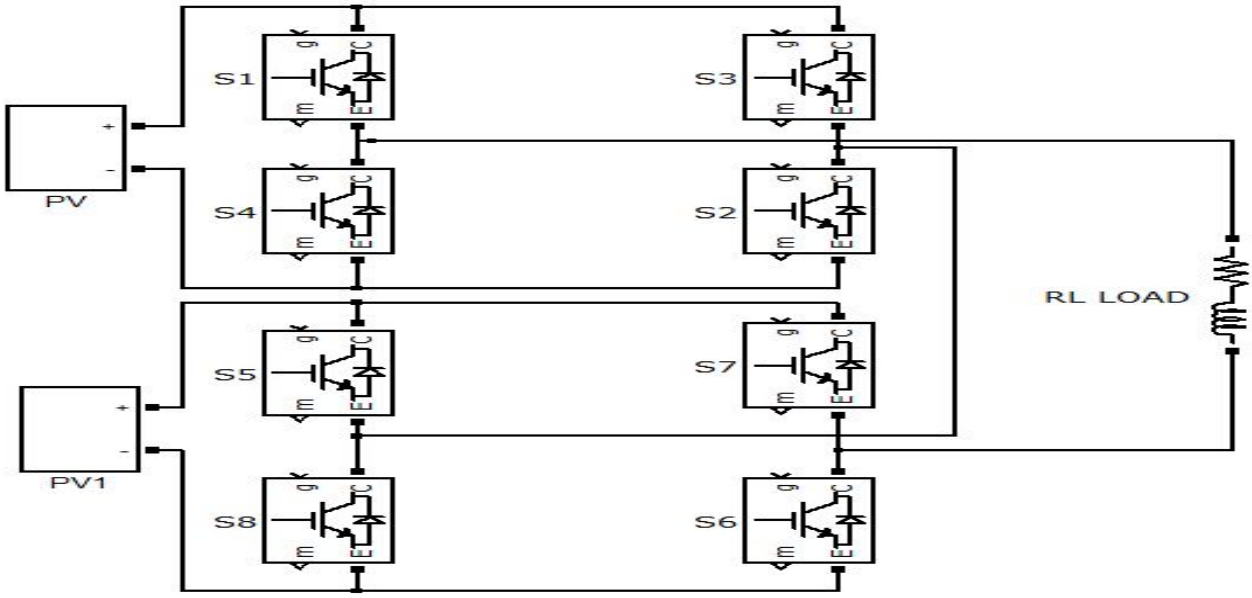

Fig.2.Proposed Asymmetrical cascaded h-bridge seven level inverter

IV. SYMMETRICAL CASCADED H-BRIDGE INVERTER

The Cascaded H-Bridge Multilevel converters are simply a number of conventional two-level bridges whose AC terminals are simply connected in series to synthesize the output waveforms. The CHB Inverter needs several independent DC sources which may be obtained from batteries, Fuel cells or Solar cells. Through different combinations of the four switches of each cell, each converter level can generate three different voltage outputs, +Vdc, 0, -Vdc. The AC output is the sum of the individual converter outputs. The number of output phase voltage levels is defined by

$$N=2M+1$$

Where

M is the number of DC Sources

N is the number of voltage levels

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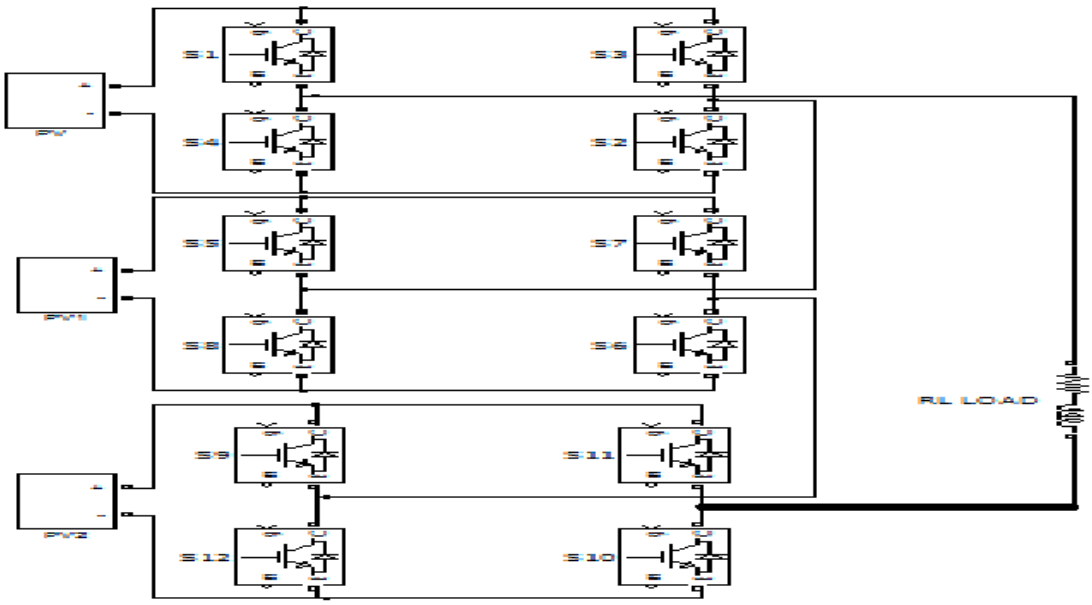

Fig.3.Proposed Symmetrical cascaded h-bridge seven level inverter

V. PWM FOR HARMONICS REDUCTION

Several modulation strategies have been developed for multilevel inverters. The most commonly used is the multi carrier PWM technique. The principle of the multicarrier PWM is based on a comparison of a sinusoidal reference waveform with triangular carrier waveforms. m-1 carriers are required to generate m levels. The carriers are in continuous bands around the reference zero. They have the same amplitude Ac and the same frequency fc. The sine reference waveform has a frequency fr and Ar is the peak to peak value of the reference waveform. At each instant, the result of the comparison is 1 if the triangular carrier is greater than the reference signal and 0 otherwise. The output of the modulator is the sum of the different comparisons which represents the voltage level. The strategy is therefore characterized by the two following parameters called amplitude modulation index ma and frequency modulation index mf .[8]

VI. SIMULATION RESULTS

In this paper, the simulation model is developed with MATLAB/SIMULINK. The simulation model of the proposed cascaded h-bridge seven level inverter is shown in figure 4 and the line voltage is shown in figure 5. The proposed circuit needs independent dc source which is supplied from photovoltaic cell. THD analysis for seven level asymmetrical and symmetrical cascaded h-bridge inverter are shown in figure 6 and 7.

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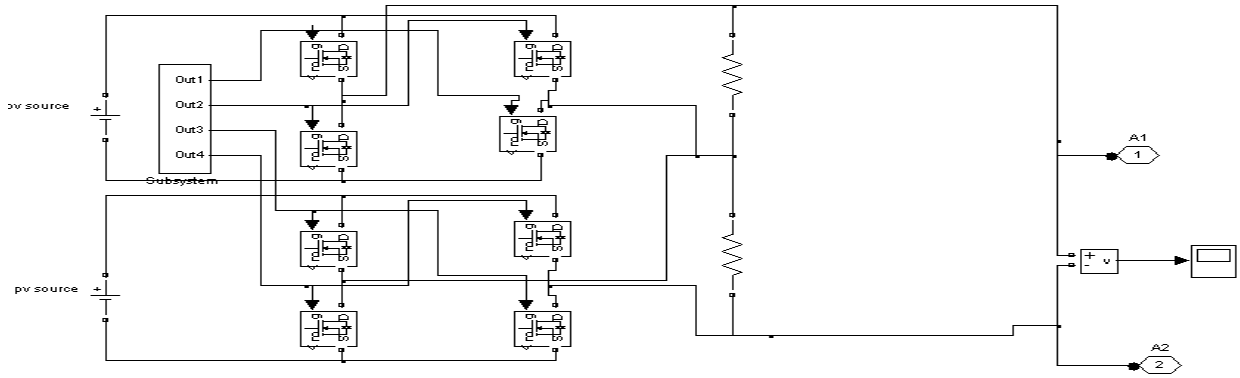

Fig.4.Proposed topology

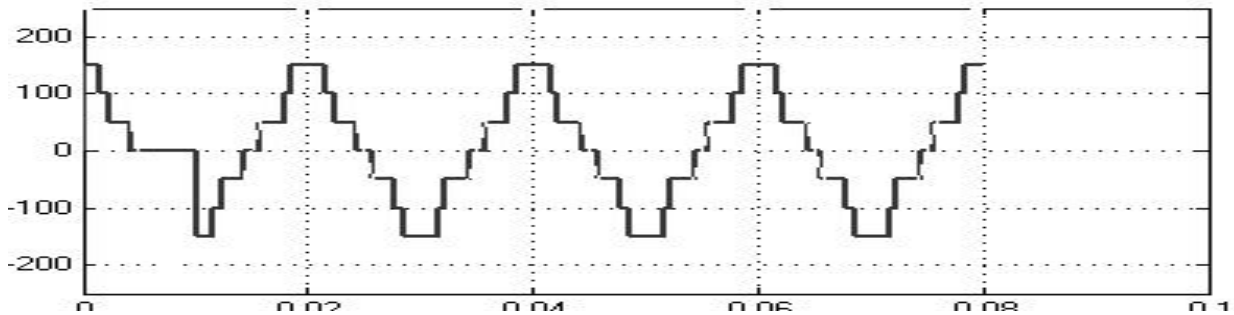

Fig.5.Output voltage waveform

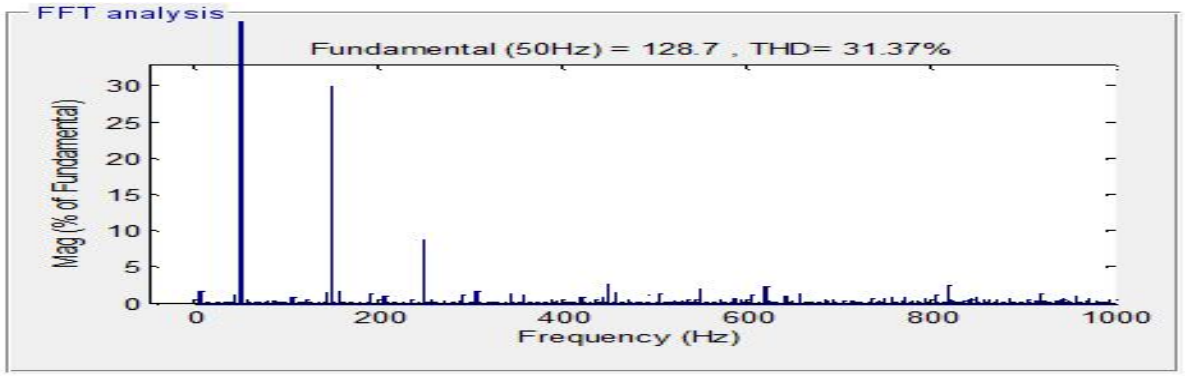

Fig.6.THD analysis(Asymmetrical)

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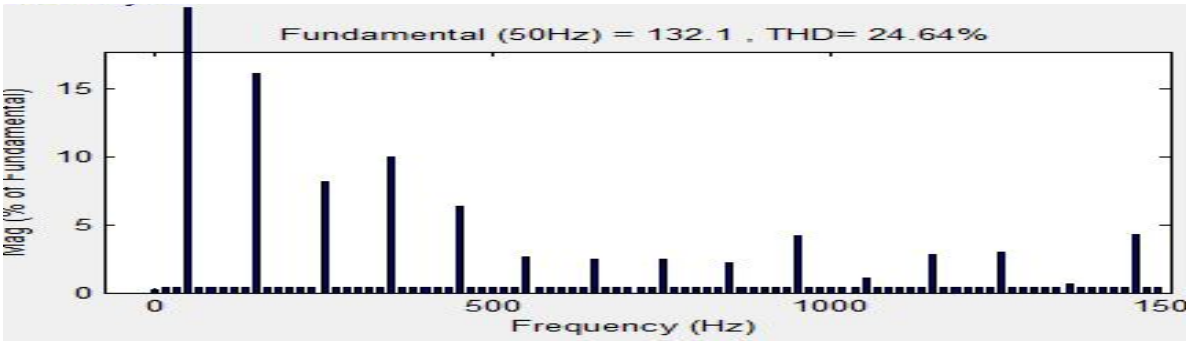

Fig.7.THD analysis(Symmetrical)

Table .I Comparison of THD performance and voltage stress

Cascaded H-Bridge Inverter	THD(%)	Voltage Stress(V)
Symmetrical	24.64	31.8
Asymmetrical	31.37	63.6

VII. CONCLUSION

In the present work, performance of symmetrical and asymmetrical cascaded h-bridge seven level inverter with photovoltaic cell as its input source by using multicarrier pwm technique has been analyzed by the MATLAB/Simulink From the simulated analysis total harmonic distortion of the symmetrical cascaded h-bridge seven level inverter is low (24.64%) and develops a minimum voltage stress across the switch (31.8V) when compared to symmetrical cascaded h-bridge seven level inverter. Hence we could achieve the improved efficiency of the system and the future work may be focused on implementing closed loop control to achieve better performance.

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