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Comparison of Interleaved Boost Converter Topologies with Voltage Multiplier for Battery Charging Of PHEV

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ABSTRACT: This paper deals with three different topologies of voltage multiplier cells with Interleaved Boost Converter (IBC) for charging the battery of Plug-in Hybrid Electric Vehicle (PHEV). A DC-DC boost converter is used to step-up the voltage. Here, interleaving structure is used to reduce the input current ripple, output voltage ripple, power loss and to reduce the input current that is fed to the battery of the PHEV. Voltage multiplier cells are used to reduce the narrow turn-off periods. Three topologies are compared in this paper: i) Interleaved Boost Converter ii) Interleaved Boost Converter with Diode-Capacitor multiplier iii) Interleaved Boost Converter with switched capacitor and coupled inductor. Simulation studies of the proposed topologies are carried out in MATLAB. The various performance parameters are compared and the best topology is chosen for the battery charging of the PHEV. The results are verified.

KEYWORDS: IBC; Voltage multiplier module; PHEV

I. INTRODUCTION

Hybrid Electric vehicles are beingdeveloped by manufacturers to reduce the carbon dioxide emissions and to reduce the conventional fuel energy consumption.Recently, automotive manufacturers are developing plug-in hybrid electric vehicles (PHEV) which reduces the environmental pollution[1]. These vehicles have an AC/DC converter which supplies power from a commercial power supply to an on-board charger along with a DC/DC converter to supply power to its accessories. Because of the limitation in the charging time and restricted space, the DC/DC converters have to be designed efficiently[2].

Interleaved Boost Converter (IBC) is employed in this work to step-up the input voltage that is being converted into DC by the rectifier. A two-phase interleaved structure is taken for this study because increasing the number of phases enhances the efficiency but the converter design becomes complex. Therefore, two-phase structure is preferred. Interleaving structure has two inductors connected in parallel and so the current path gets divided into two and the conduction loss can be reduced thus improving the overall efficiency η of the system[3].

The duty ratio of the IBC is chosen to be 0.6,since it gives the maximum efficiency. The ripple reduction is a function of duty cycle. Because the two phases are combined at the output capacitor, effective ripple frequency is doubled, making ripple reduction much easier[4]. Since the output ripple is double the frequency of the individual phases and at a low rms current value, the size and the rating of the passive components that is being used can be reduced considerably.

Voltage multiplier cells are used to avoid narrow turn-off periods and to reduce the current ripple. Interleaved structure is used in the input side to distribute the current and voltage multiplier cells on the output side to achieve a high step-up gain.

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A comparison between the topologies is done based on the various parameters like input current ripple, output voltage ripple, gain of the converter and the best one is chosen to be used along with the rectifier in the On-board battery charger. The main aim is to obtain a high gain converter with reduced input current ripple and reduced output voltage ripple.

II. IBC TOPOLOGIES

A. *Basic Interleaved Boost Converter:*

The conventional two phase boost converter consists of two single boost converters that are connected in parallel as shown in Fig 1.

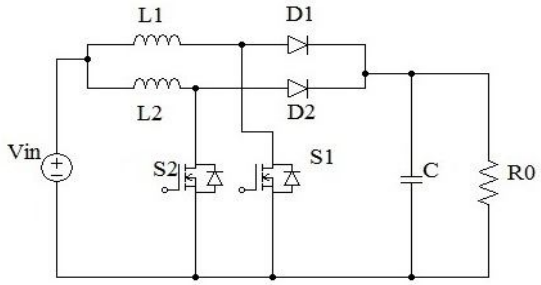

Fig 1.Circuit diagram of the Conventional Interleaved Boost Converter

Each switch is gated with a difference of 360/n where n is the number of phases and since here its two, the switches are gated with a phase difference of 180^0.Using the IBC instead of the Conventional Boost Converter reduces the THD to about 40% in a PHEV[5].

Operation:

Firstly when the device S1 is turned ON, the current in the inductor iL1 increases linearly. During this period energy is stored in the inductor L1. When S1 is turned OFF, diode D1 conducts and the stored energy in the inductor ramps down with a slope based on the difference between the input and output voltage. The inductor starts to discharge and transfer the current via the diode to the load. After half switching cycle of S1, S2 is also turned ON completing the same cycle of events.

The conversion ratio is a function of the duty cycle and the relation is as follows:

$$\frac{V_0}{V_{in}} = \frac{1}{1\text{-}D} \quad \text{eq.(1)}$$

where V_{in} is the input voltage, V_0 is the output voltage and D is the duty ratio.

B. *IBC with Diode-Capacitor multiplier:*

The diode-capacitor multiplier cells helps to enlarge the voltage conversion ratio and to avoid extreme duty cycles. The voltage stress on the devices is less in this topology[6]. Here one stage of voltage multiplier cell is employed to reduce the complexity. The circuit diagram of the IBC with the diode-capacitor multiplier cells is as follows:

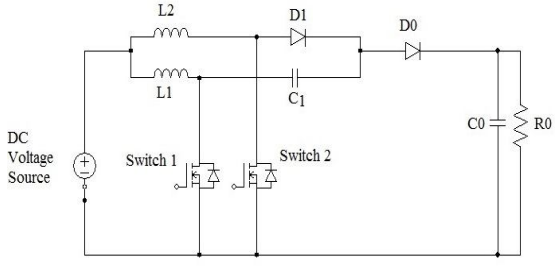

Fig 2. IBC with diode-capacitor multiplier

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Operation :

The operation can be explained in four modes.

Mode 1:

At t = t0, switch S1 is ON, thus diode D0 is OFF. Switch S2 is also ON and thus D1 is OFF. Current increases linearly from its minimum value at t0 and current il2 increases linearly up to itsmaximum value at t1. iC1 is zero and uc1 is kept constant.

Mode 2:

The gating signal of switch S2 is removed; thus diode D1 is ON. Switch S1 is ON making diode D0 to turn OFF. Current il1 still increases linearly, inductor L2 charges C1 and then switch S2 is gated.

Mode 3:

Mode 3 operation is similar to that of mode 1.

Mode 4:

At t=t3, switch S1 is gated OFF, and diode D0 is turned ON. Switch S2 is kept ON and current il1 begins to decreases linearly through C1 which gets discharged. Whereas, current il2 still increases linearly.The time t4 is the ending of a switching cycle Ts.

The switching pattern of the DCM is as follows:

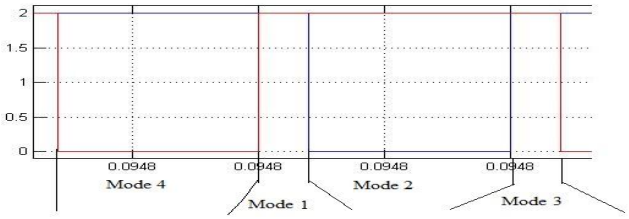

Fig 3. Switching pattern of the IBC with diode-capacitor multiplier

The conversion ratio here is given by :

$$M=\frac{u_0}{u_{in}}=\frac{n+1}{1-D} \quad \text{eq.(2)}$$

where u_0 and u_{in} are the input and output voltages and n is the number of the multiplier cells.

C. *IBC with Switched capacitor and Coupled inductor*

The voltage multiplier module here consists of switched capacitors and coupled inductors. Using switched capacitor into an IBC makes the voltage gain to reduplicate, but the coupled inductor if not employed limits the voltage gain. Oppositely, if coupled inductors are used along with IBC the voltage gain is higher and adjustable but without switched capacitor the voltage gain is ordinary[7]. So, we integrate both into the circuit to obtain high step-up gain, high efficiency and low voltage stress.

The circuit diagram of this topology is as follows:

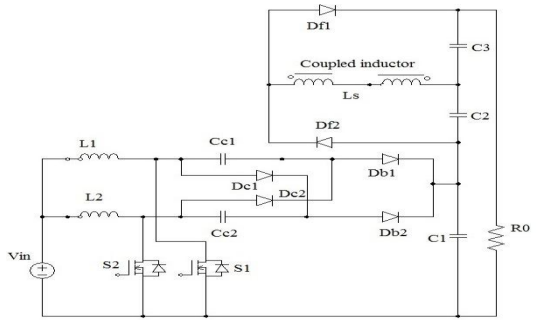

Fig 4. IBC with Switched capacitor and coupled inductor

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The coupled inductors extend the step-up conversion ratio whereas the switched capacitors offer extra voltage conversion ratio. The coupled inductors reduce the core loss in the circuit. The voltage conversion ratio here is given by:

$$V_0 = \frac{2n+2}{1-D} V_{in} \quad \text{eq.(3)}$$

where V_o and V_{in} are the input and output voltages and n is the number of the Voltage Multiplier Module(VMM).

Operation:
The operation of this circuit can be explained in eight modes:

Mode 1:
At time t=t0 , switch S2 remains in the ON state and S1 begins to turn ON. The coupled inductor release the stored energy to the output terminal through the forward diode *Df*2.The diodes *Dc*1, *Dc*2, *Db*1, *Db*2, and *Df*1 are reversed biased. The inductor L1 transfers energy to the secondary side of the coupled inductor.

Mode 2:
At *t* = *t*1, both of the power switches *S*1 and *S*2 remain in ON state, and all diodes are reversed biased. Both currents through leakage inductors *L*1 and *L*2 are increased linearly due to charging by input voltage source *V*in.

Mode 3:
At *t* = *t*2, *S*1 ON state &*S*2 begins to turn off. The diodes Dc1, Db1, and Df2 are reversed biased.The diodes *Dc*1, *Db*1, and *Df*2 are reversed biased. The energy stored in the L2 is transferred to the secondary side of the coupled inductor. The current through the coupled inductor flows to output capacitor C3 through the flyback diode Df1. The voltage stress on the power switch S2 is clamped by the Cc1 which is equal to the output voltage.

Mode 4:
At t = t3, the current iDc2 has naturally decreased to zero due to the magnetizing current distribution, and hence, diode reverse recovery losses are alleviated and conduction losses are decreased. Both power switches and all diodes remain in previous states except the clamp diode Dc2 .

Mode 5:
At t = t4, the power switch S1 remains in ON state, and the other power switch S2 begins to turn on. The diodes Dc1, Dc2, Db1, Db2, and Df2 are reversed biased. The coupled inductor quickly releases the stored energy to the output terminal. Thus, the inductor L2 still transfers energy to the secondary side of coupled inductors.

Mode 6:
At t = t5, both of the power switches S1 and S2 remain in ON state, and all diodes are reversed biased. Both currents through inductors L1 and L2 are increased linearly due to charging by input voltage source Vin

Mode 7:
At t = t6, S2 is ON state, and S1 begins to turn off. The diodes Dc2, Db2 and Df1 are reverse biased. The voltage stress on power switch S1 is clamped by clamp capacitor Cc2 which equals the output voltage of the boost converter. The inductor L1 and capacitor Cc1 release energy to the output terminal. Thus the Vc1 obtains double output voltage of the boost converter.

Mode 8:
At t=t7, the current iDc1 has naturally decreased to zero and thus diode reverse recovery losses are alleviated.

D. *Design Equations:*
The capacitors and inductors are designed using formulas given below:

- The value of the capacitor is got from:

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$$C=\frac{DV_0T}{R\Delta V_0} \text{ eq.(4)}$$

where V_0 is the output voltage
T is the time period
R is the resistance
ΔV_0 is the ripple of the output voltage
D is the duty ratio

- The value of the inductor is got from :

$$L=\frac{V_{in}D}{\Delta I_L f_S} \text{ eq.(5)}$$

where V_{in} is the input voltage
fs is the switching frequency
ΔI_L is the ripple content in the Inductor

E. *Simulation Results:*

The three topologies are simulated in MATLAB with the following parameters constant for all the three topologies:

Duty Ratio ∂	0.6
Input Voltage Vin	40 V
Frequency fs	50kHz
Capacitor C	40µF
Inductor L	640µH

Table 1.Simulation parameters for all the three topologies

The simulation results of the three topologies are as follows:

An output voltage of 95V was obtained with the Interleaved Boost Converter. The fig5.andfig 6. shows the output voltage waveform and output voltage ripple waveform obtained with this topology.

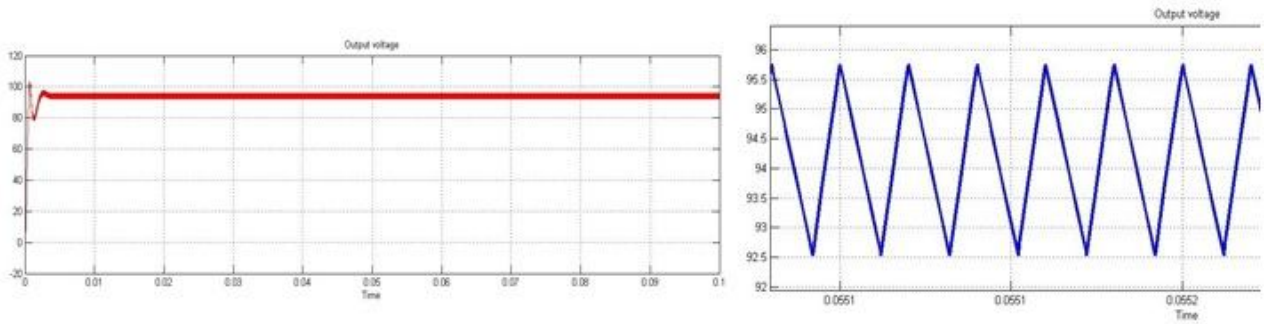

Fig 5.Output of the Conventional IBCFig 6. Output voltage ripple of the IBC

The IBC with diode-capacitor multiplier produced an output voltage of about 176V. The output voltage waveform and the output voltage ripple waveform that was obtained in Matlab for this topology is shown in fig 7. and in fig 8. respectively.

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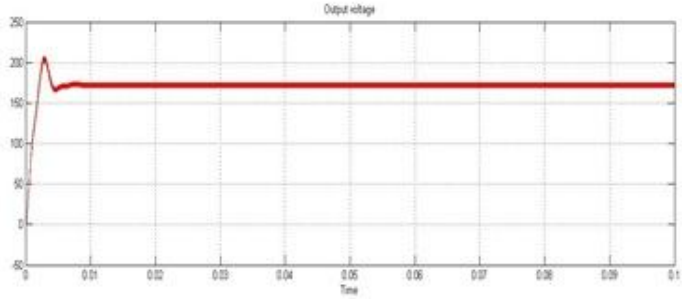


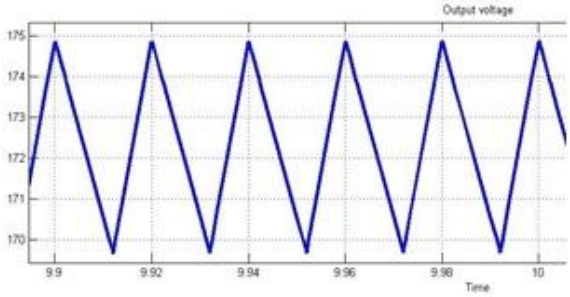
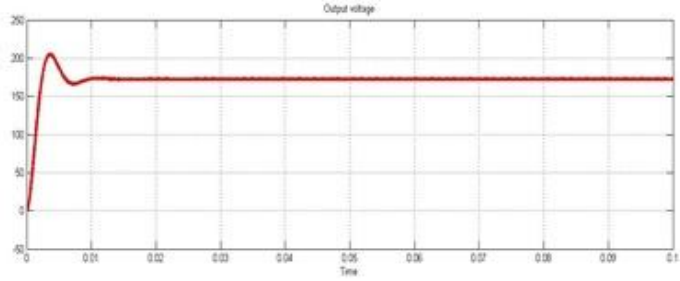


Fig 7.Output of the IBC with diode-capacitor multiplierFig 8. Output voltage ripple of the IBC with DCM

The output voltage that was obtained with the IBC with switched capacitor and coupled inductor was 173V. The output waveform and the output voltage ripple waveform are represented in the fig 9. and fig 10. respectively.



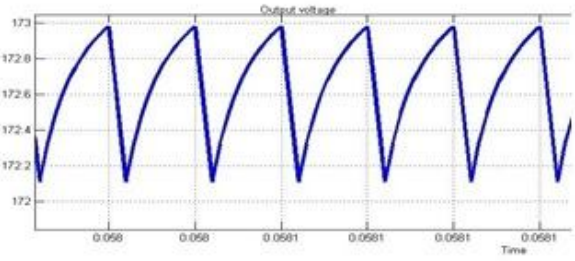


Fig 9.Output of the IBCwith switched capacitor and coupled inductorcapacitor and coupled inductor

Fig 10. Output voltage ripple of IBC with switched

Comparison between the three topologies based on the various parameters:

	Input Current Ripple (%)	Output Voltage Ripple (%)	Output Voltage	Gain (%)
Interleaved Boost Converter	1.475	3.175	95	0.4
With Diode-Capacitor multiplier	**0.346**	**2.11**	**176**	**4.4**
With switched capacitor and coupled inductor	0.315	0.521	173	4.325

Table 2. Comparison between the three topologies

Inferences :

The comparison of the three topologies have shown that though the output voltage ripple and input current ripple of the Diode-Capacitor multiplier is little higher compared to the other three topology, it is the optimum one and thus it is chosen for the battery charging application of PHEV.

F. *Conclusion :*

Various topologies of Voltage multiplier cells are simulated in the paper and comparison based on the various parameters are done. The IBC with the Diode-capacitor multiplier is proposed to be the best one to be used along with the rectifier for a PHEV with reduced input current and reduced output voltage ripple so that the size of the passive

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components like inductors and capacitors are reduced. A compact and efficient DC/DC converter thus can be developed.

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