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Design and Analysis of Low-Power 11-Transistor Full Adder

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ABSTRACT: Full adders are exigent components in applications such as digital signal processors (DSP) architectures and microprocessors. In this paper, we propose a technique to build a new 11-transistor FA .We have done HSPICE simulation runs the new design 11-T full adders .In CMOS integrated circuit design there is a tradeoff between static power consumption and technology scaling. Static power dissipation is a challenge for the circuit designer. So we reduce the static power dissipation. In order to achieve lower static power consumption, one has to scarifies design area and circuit performance. In this paper we propose a new circuit of 11-Transistor full adder in CMOS VLSI circuit.

KEYWORDS: F.A., low power, very large-scale integration (VLSI).

I. INTRODUCTION

THE Elevated growth in laptop, moveable systems, and cellular networks has intensified the examine efforts in low-power microelectronics. Today, there is an ever growing no. of moveable applications requiring low power and high throughput circuits. Therefore, low-power design has develop into a major design consideration.

The adder is one of the most necessary components of a processor, as it is used in the automatic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access. The full adder performance would affect the system as a whole. A variety of full adders using static or energetic logic styles have been reported in the literature. The conventional adder uses 28 transistors implemented in CMOS technique. Figure 1. is shown the conventional 28-T full adder circuit. A new full adder uses only 11 transistors, which has the least number of transistors and has reported to be the best in power consumption.

Power consumption is one of the top concerns of Very Large Scale Integration (VLSI) circuit design, for which Complementary Metal Oxide Semiconductor (CMOS) is the primary technology. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI technique to reduce leakage power, we use dual sleep technique.This technique provides an efficient way to reduce leakage power. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

Previously, the circuit of 10-transistor full adder is designed and its consumes a large power. so here we design a 11 transistor full adder. the 11 transistor full adder circuit is consume less power as compare to previous 10 transistor full adder. Comparison is shown in the table I.

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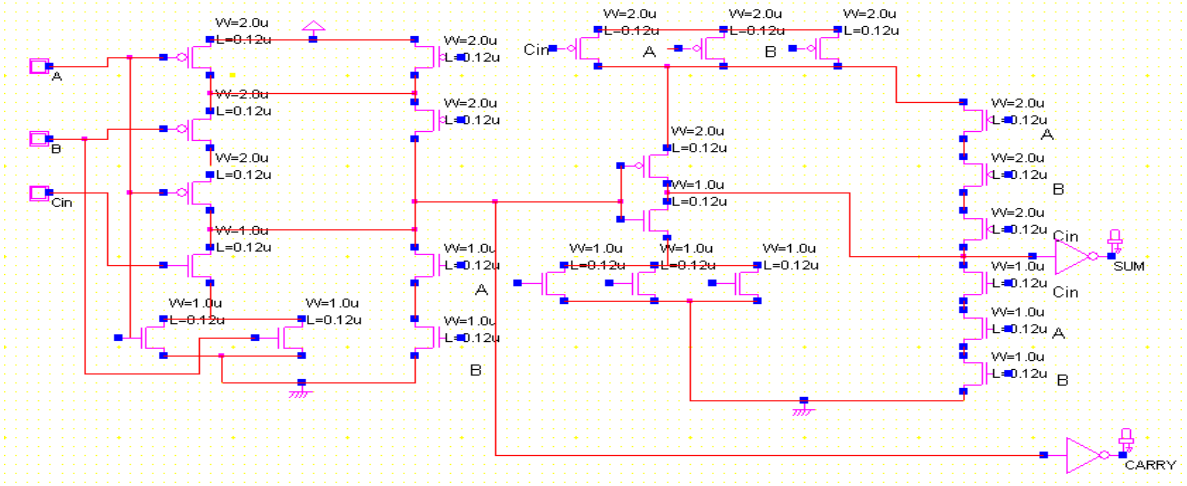

Figure 1. Conventional 28-T full adder

II. PREVIOUS WORK

A systematic approach to designing many 10-transistor full adders. This new 10-T adders also have the threshold-loss problem; however, the adders are useful in bigger circuits such as multipliers despite the threshold-loss problem.

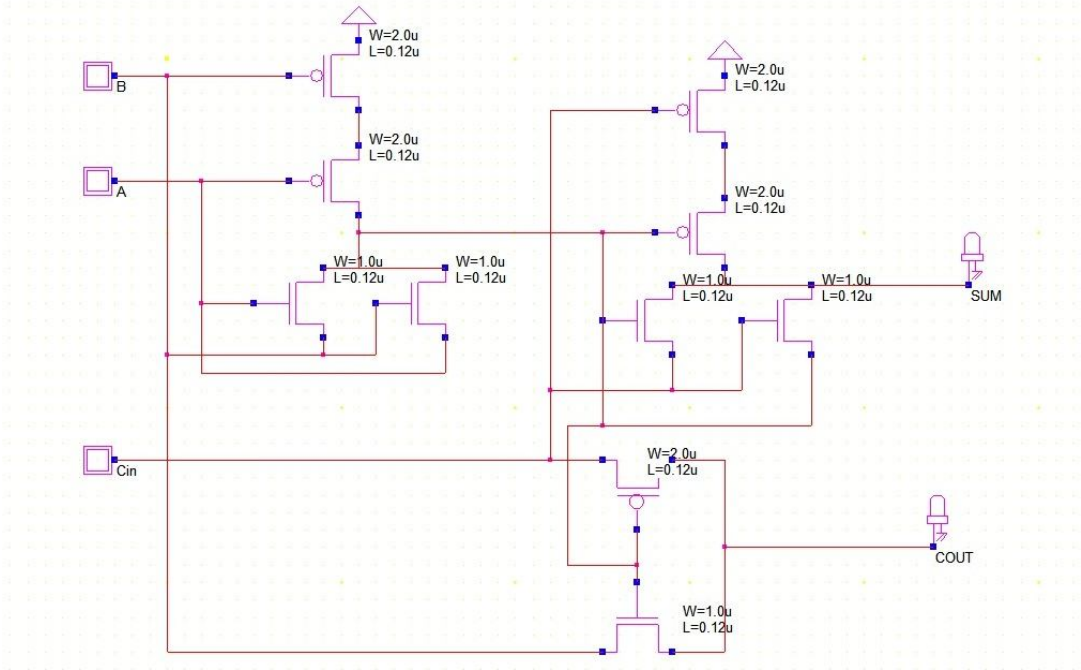

Fig. 2. SERF 10-Transistor adder.

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Using a novel set of XOR–XNOR gates in combination

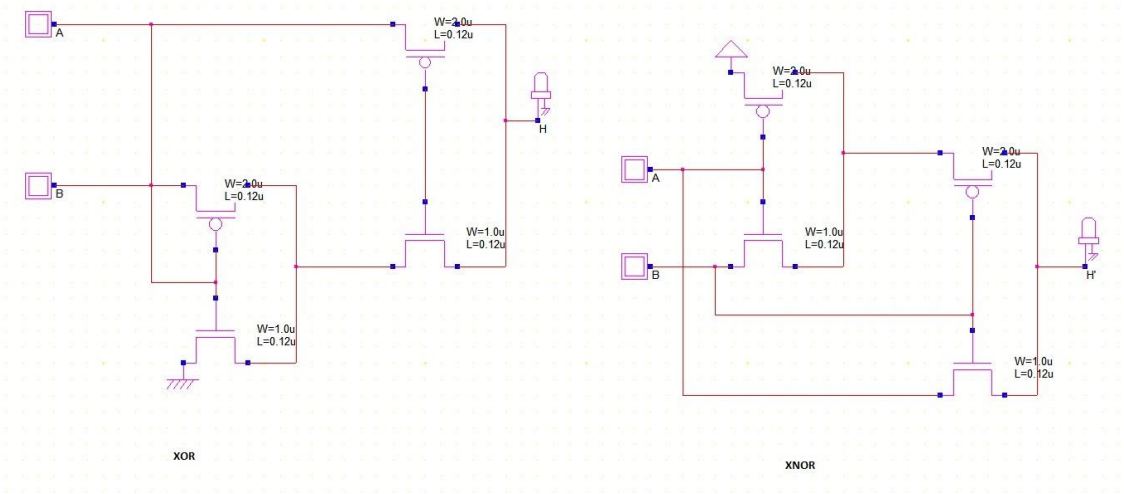

Figure 3 P-/G- XOR-XNOR Gates.

with existing ones, a total of 41 new 1-bit full-adders are created.
Before the presented 10 -T full adder, first proposed anew design XOR gate shown in figure 3. It resembles the inverter-based XOR shown in Fig. 4 but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Because the new XOR gate has no power supply, it is called *Powerless* XOR, or P-XOR. Similarly, we propose a new XNOR gate which is named *Groundless* XNOR, or G-XNOR, because there is no direct connection to the ground.

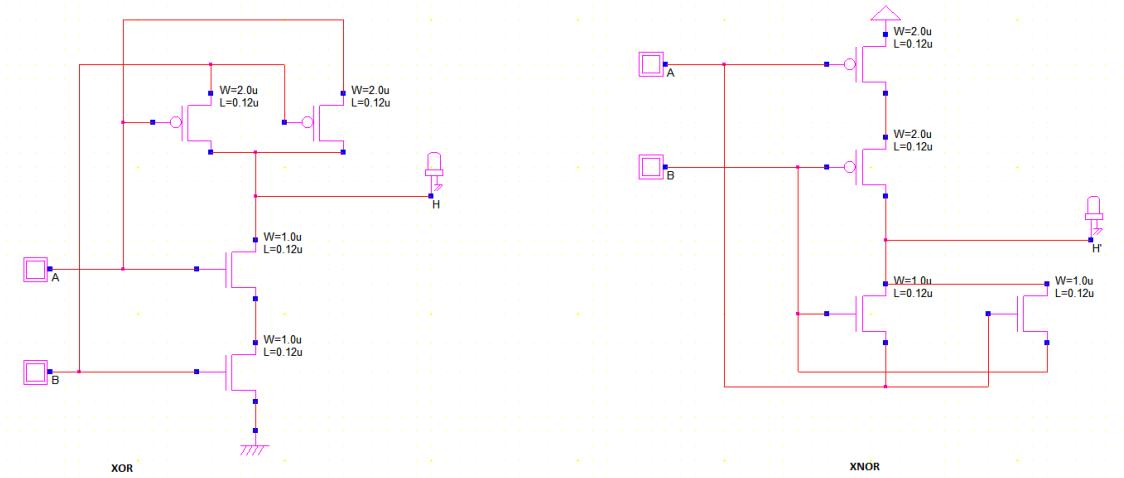

Figure 4. XOR-XNOR Gates.

Full Adder

In the previous work, full adder use three modules, shown in the figure 5. to implement the full adder based on (4) or (5) and (6). Module-1 and module-2 can be XOR or XNOR gates and module- can be a multiplexer, double PMOS or double NMOS transistors. The sum is generated by cascading module-1 and module-2. This implements (4) or (5). The function is implemented by module-1 and module- according to (6)

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A+B+Cin = 2*Cout+SUM……..(1)
Cout = (A∧B)∨((A∨B)∧Cin)…….(2)
SUM = (A∧B∧Cin)∨(A∨B∨Cin)∧(Cout')…….(3)
SUM = A exor B exor Cin……..(4)
SUM = A exnor B exnor Cin……(5)
Cout = (A∧(A exnor B)) ∨ (Cin ∧(A exor B))…….(6)

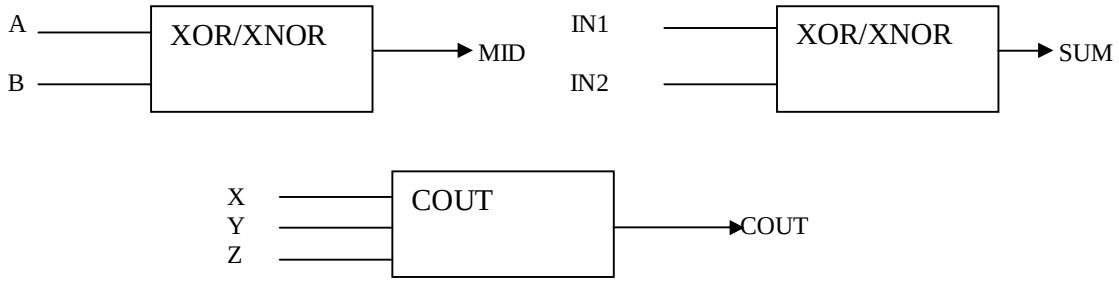

Figure 5 Adder Modules

In previous work, the first some full adders use the multiplexer as module COUT. In the previous paper we studied that we design a 42 different full adder circuit using this adder modules and the SERF adder is best in 42 adders..

III. NEW DESIGN FULL ADDER

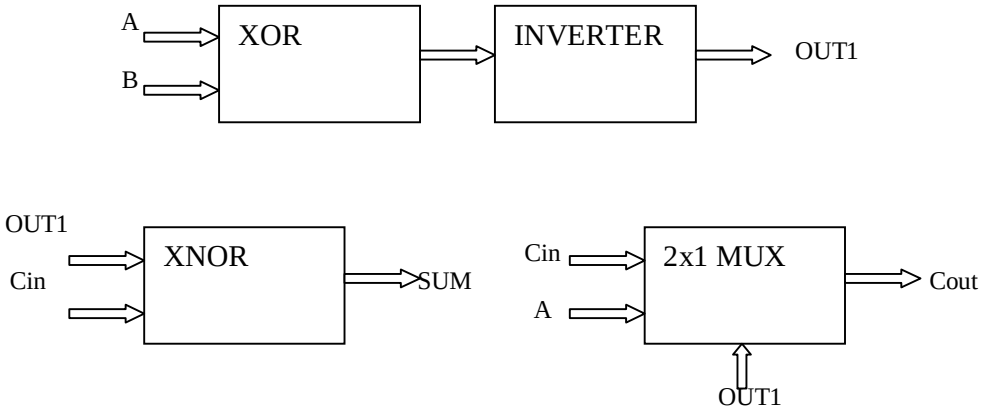

Figure. 6 Basic block diagram of 11-T full adder.

The figure 6 is shows the basic block diagram of the proposed new design 11-full adder circuit. The circuit diagram of proposed 11-T full adder is shown in the figure 7. In the figure 6 we see that the block diagram of 11-T full adder, in this one xor, one inverter, one xnor and one 2-T multiplexer gates. The output of the xnor gives the SUM and the output of the 2-T multiplexer is give the CARRY.

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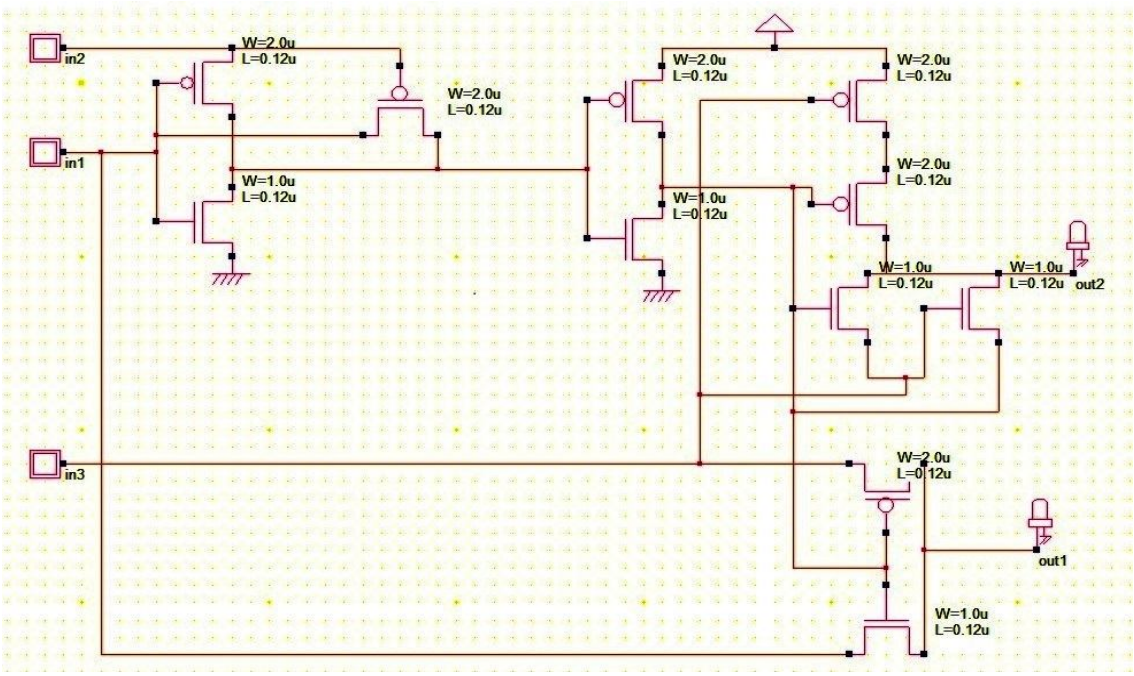

Figure 7. 11-T Full Adder

Figure 8 shows the input pattern of the circuit, the three input is shown in the figure 8. As we know three input is required for the full adder circuit. Its not necessary to use this pattern as a input for the 11- Transistor full adder, we can change the input.

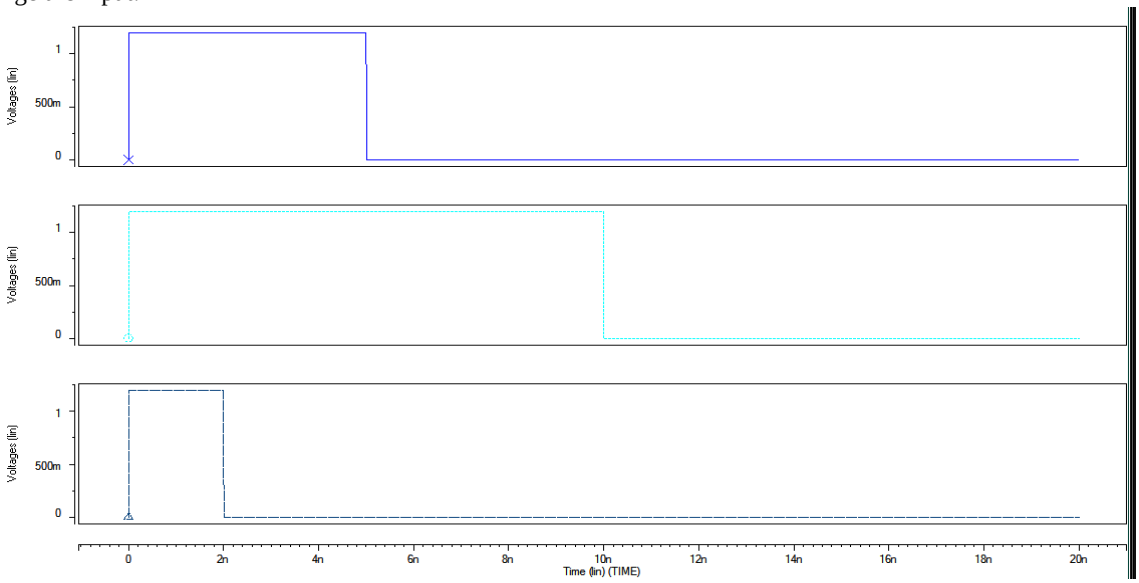

Figure 8. input waveform

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IV. EXPERIMENT DESCRIPTION AND THE RESULT

We have performed experiments on the newly designed 11 transistor full adders. The transistors have a channel length of 90nm and a channel width of 360nm using 0.9 V logic. Circuit is simulated with the same testing conditions. The netlists of those adders are extracted and simulated using HSPICE .

Table I
DESCRIPTION OF POWER DISSIPATION OF FULL ADDER CIRCUITS

Sl. No.	Full Adder	Power Dissipation (In P. Watt)
1.	10-Transistor	60.0120
2.	11-Transistor	49.0760

The above table I shows the value of power dissipation according to the W/L ratio(width/length). So from the table I we conclude that our new design 11-transistor full adder circuit dissipated less power compared to the other full adder circuits. Figure 9. shows the graph representation of full adder circuit performance. Figure shows the power dissipation values when the Channel width is 360n and channel length is 90n. We can also conclude our circuit performance from the graph. From the graph we can say that our circuit consume the less power.

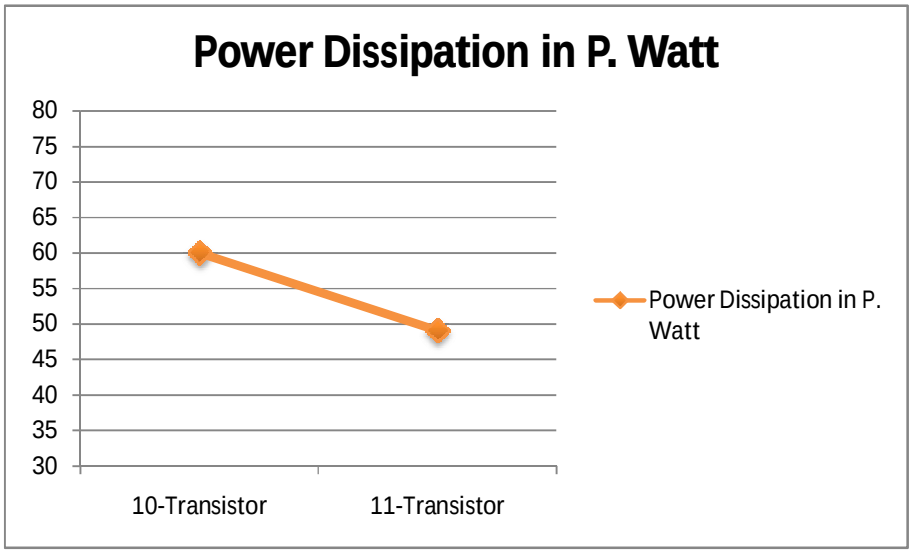

Figure. 9 Power dissipation of full adders.

VI. CONCLUSION

In this paper, we have presented a systematic approach to construct full adders using only eleven transistors. Based on our extensive simulations, we conclude that our circuit consume less power compared to the previous ten-

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transistor circuit. This circuit is simulated in HSPICE. New adders consume on average 18% less power compared to the previous ten-transistor adder.

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