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Design and Implementation of Morphological Operations Using Reconfigurable Processor

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ABSTRACT: In this paper, we present a novel approach to reconfigurable processor which has been applied for binary image processing. The processor's architecture is a combination of a reconfigurable binary processing module, input and output image control units, and peripheral circuits. The reconfigurable binary processing module, which consists of mixed-grained reconfigurable binary compute units and output control logic, performs binary image processing operations. Each Binary Compute unit performs different operations such as Median filtering, Dilation, Erosion and Binarization respectively. Each binary computational unit has unique operation implemented with related algorithm which can be used for different applications.

The simulation and experimental results demonstrate that the processor is suitable for real-time binary image processing applications. This processor is designed in VHDL language and implemented on Xilinx-Vertex 5 Field Programmable Gate Array.

KEYWORDS: Binary image processing, field-programmable gate array (FPGA), mathematical morphology, Structuring element, Binarization.

I. INTRODUCTION

Mathematical morphology is a powerful tool for geometrical shape analysis, description and extracting features from an image. Mathematical morphology uses the concept of mathematical set theory for extracting meaning from the image [7]. The main aim of this study is to transform the digital images into different forms. Image processing techniques are used with wide varieties of applications. The requirement is different for different applications. This study is mainly focused on how to transform the image using mathematical morphology so that it can be suitable for the respective applications. Mathematical morphology has been chosen to explain how images are used to illustrate mathematical set theoretic operations, such as union, intersection by means of morphological operations like median filtering, Dilation, Erosion and Binarization. There are numerous applications using different binary morphological operations e.g., object recognition, tracking, and region filling. The existing binary morphology employs the image processing with MATLAB simulation. Hence the synthesis could be done with FPGA architecture. Binary image processing is a powerful tool in many image and video applications. Hence a reconfigurable processor is presented for binary image processing in this method. Reconfigurable computing represents an intermediate approach between the extremes of Application Specific Integrated Circuits (ASICs) and general-purpose processors. A reconfigurable system generally has wider applicability than an ASIC [8]. Also, most general-purpose processors would very likely not satisfy the performance constraints for the entire application.

II. RELATED WORK

A chip with a 500-dpi cellular-logic processing array was implemented to enhance and verify fingerprint images [1]. A pointing device using a specialized algorithm was presented for motion detection in [9]. The MIPA4k, as presented in [2], was a 64 × 64 mixed-mode array processor for identifying local binary patterns. All the above-mentioned chips are designed for specific applications. The major drawback of application-specific chips is the lack of flexibility. The

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reconfigurable technique can bridge the gap between application-specific integrated circuits and flexibility. A programmable single instruction multiple data (SIMD) real time vision chip was presented to achieve high-speed target tracking [10]. In [11], a programmable binary morphology coprocessor was introduced to the visual content analysis engine of the chip used for visual surveillance. It has been a common practice to build application-specific chips for real-time binary image processing [1], [2]. However, such chips have a limited application range. On the other hand, the general-purpose binary image processing chips mentioned above have their own problems. Some of these chips are made of analog circuit [3], [4], and some are made up of an analog part and a digital part [10], [5]. When compared with the digital part, the analog part shows low robustness, accuracy, and scalability although it has a small area and low power consumption [5]. Other general-purpose chips have the architecture of a digital processor array, in which each digital processor handles one pixel. When large sized images are processed, the chips will become extremely large. Thus, further studies are needed to design a high performance, small size, and wide application range chip for real-time binary image processing. Reconfigurable systems are computing systems that combine a reconfigurable hardware processing unit with a software-programmable processor.

III. ARCHITECTURE

The processor has the merit of high speed, simple structure, and wide application range. The architecture of the proposed processor is shown in Figure1. A binary image processor that consists of a reconfigurable binary processing module, including reconfigurable binary compute units and output control logic, input and output image control units. The performance of the processor is enhanced by using the dynamic reconfiguration approach. Basic mathematical morphology operations and complicated algorithms can easily be implemented on it. The processor has the merit of high speed, simple structure, and wide application range.

The core of the processor is a reconfigurable binary processing module consisting of binary compute units and output control logic as shown in Figure.2. The processor also has Memory, the input and output control logic units, the process control unit. Reconfigurable binary processing module can be divided in to two main parts. First output control logic unit and the second part consists of several binary compute units. Each binary compute unit perform different operations such as median filtering, Dilation, Erosion and Binarization respectively.

The Block diagram consists of two parts. The first part is the output control logic ,which selects the output from all the binary compute unit outputs according to the given parameters. The second part consists of several binary compute units that perform binary logic and binary image operations at high speed. The binary image algorithms are realized by the operations in the individual binary compute units and the connection pattern of these units. Each binary compute unit perform different operations such as median filtering, Dilation, Erosion and Binarization respectively .The operation executed in a binary compute unit is decided by configurable registers, including logic operation parameters, image resolution parameters, mask sizes, input and output selection parameters.

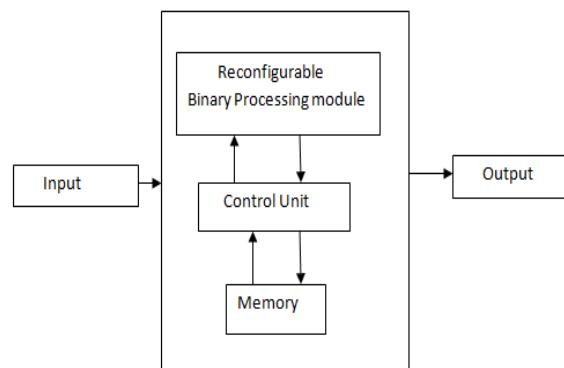


Figure.1: Binary image processor

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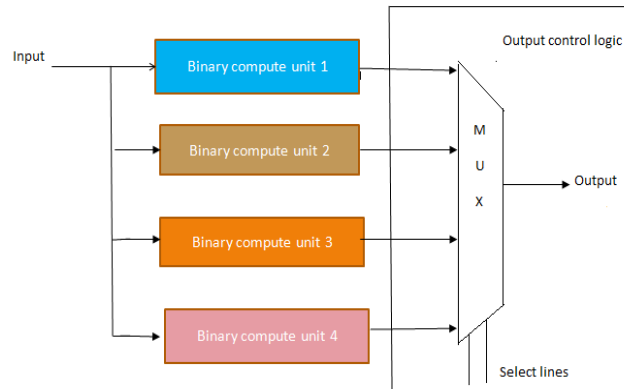


Figure.2 Diagram of the reconfigurable binary processing module

IV. BINARY COMPUTE UNITS

Binary compute units perform binary logic and binary image operations at a high speed. The binary image algorithms are realized by the operations in the individual binary compute units and the connection pattern of these units.

A. Binary compute unit1: Median Filtering using Sort Optimization.

Median filtering is a nonlinear method used to remove noise such as salt and pepper noise from images[6]. The median filter works by moving through the image pixel by pixel, replacing each value with the median value of neighboring pixels.

The formula of median filtering can be expressed as:

$$g(x,y) = \text{med} [f(x-i, y-i)]$$

where $g(x,y)$ - filtered image
 $f(x,y)$ - original image

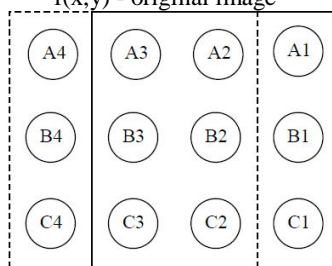


Figure.3sequence of image processing data

First, we must sort the data by column. We need to do 9 comparisons to get the following result, we assume the result is

$$\begin{aligned} A1 > B1 > C1 \\ A2 > B2 > C2 \\ A3 > B3 > C3 \end{aligned}$$

Secondly, we need to find the maxim data in C1, C2 and C3 by doing 2 comparisons, and find the minimum data in A1, A2 and A3 by doing 2 comparisons, and find the median data in B1, B2 and B3 by doing 3 comparisons. The formula is as follows

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$$A_{min} = \min(A_1, A_2, A_3)$$

$$B_{med} = \text{med}(B_1, B_2, B_3)$$

$$C_{max} = \max(C_1, C_2, C_3)$$

Lastly, we need to find the median data in A_{min} , B_{med} and C_{max} by doing 3 comparisons.

$$F_{med} = \text{med}(A_{min}, B_{med}, C_{max})$$

The resulted F_{med} is the final result. In the next circle, the comparison results of (A_2, B_2, C_2) and (A_3, B_3, C_3) have been obtained, we only need to seek the sorting of the updating data A_4, B_4, C_4 , and then use previous equations to calculate the required median. The processing element (PE) is the basic processing unit, which is designed for comparing 2 input data. D stands for D flip-flop, whose function is to make a single-circle delay. It is used for synchronizing the calculation here. Because the proposed algorithm needs to store two groups temporary data in current processing, we design two D flip-flops to realize this function.

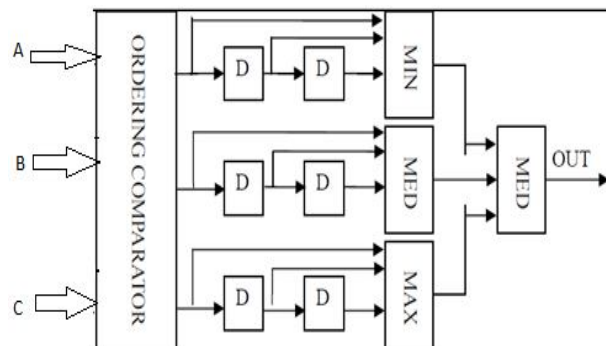


Figure.4 Hardware structure of median filter module [6]

The data in A, B and C will be sent to the ordering comparator for data ordering, and the results will be sent to next different comparators as shown in figure 4. Before the second comparing, the data need 2 circle delay to distinguish the circle order of input data by two D flip-flops. The second comparing results will be sent to the final median comparator to get the final result.

B. Binary Computational Unit-2 for Erosion:

Erosion is fundamental operator of mathematical morphology, a theory for the analysis of spatial structure. The methods of mathematical morphology make possible a large number of very powerful image analysis techniques and therefore these operators and their implementations are of great theoretical and practical interest to many involved in image processing and analysis. The principle of Erosion operation is that the value of the output pixel is the minimum value of all the pixels in the input pixels neighbourhood.

Erosion shrinks the connected sets of 1s in binary image. It can be used for Shrinking the shapes and Removing the bridges, branches and small protrusions.

C. Binary Computational Unit-3 for Dilation:

Dilation expands the connected sets of 1s of the binary image. It can be used for Expanding the shapes and Filling the holes, gaps and gulfs. The principle of Dilation operation is the value of the output pixel is the maximum value of all the pixels in the input pixels neighbourhood.

From the input image, (3×3) window is selected which contains 9 input pixels are sent to registers as shown in Figure-5 & 6 and this is compared in min/max comparator. The max value gives the dilation result and min value gives erosion result. Comparison is done for remaining input pixels in the same manner. Here we are not using structuring element which has to be convolved with input image and then its compared, by doing without using structuring element we can reduce the hardware resources.

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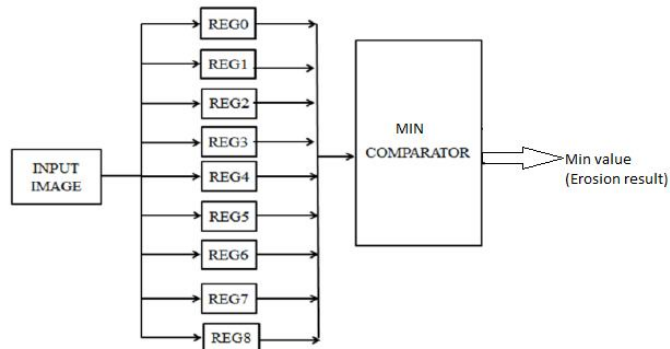


Figure.5 Block diagram of Erosion

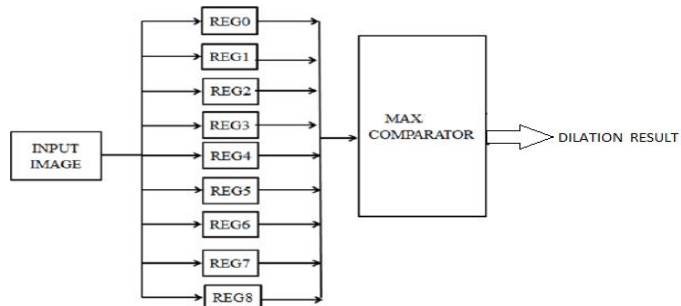


Figure.6 Block diagram of Dilation

D. Binary Computational unit-4: Binarization

Thresholding is a method to convert a Gray Scale Image into a Binary Image, so that objects of interest are separated from the background. For Binarization Fixed global thresholding method is used as shown in figure 7. Binarization or thresholding is the process that converts an image into black-and-white: a threshold value is defined and the colours above that value are converted into white, while the colours below it are converted into black. This is a very simple process in digital image processing when one has a document with black ink written on a white paper. Document image binarization is an important step in the document image analysis and recognition pipeline. The performance of a binarization technique directly affects the recognition analysis. In order to reduce storage requirements and to increase processing speed, it is often desirable to represent gray scale as binary images by picking a threshold value. Binarization algorithms are classified into global and local methods. The global algorithms calculate one threshold for the entire image. The pixels are separated into two classes, foreground and background. By selecting an adequate threshold value T , the gray level image can be converted to binary image. The binary image should contain all of the essential information about the position and shape of the objects of interest (foreground). This can be expressed as in the equation

$$I_b(x, y) = \begin{cases} \text{black} & \text{if } I_f(x, y) \leq Thr \\ \text{white} & \text{if } I_f(x, y) > Thr \end{cases}$$

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Figure.7 Global Thresholding method

V. SIMULATION RESULTS

In this paper Xilinx ISE and MATLAB is used as implementation tools .A mathematical morphology is used as a tool for extracting image components that are useful in the representation and description of region shape. Steps to be followed to perform Morphological operations.

Step 1: Generate the text file, respectively, from the input image (image to text conversion in MATLAB).

Step 2: Copy the text file in to source location.

Step 3: Perform the Morphological operations such as Median Filtering, Dilation, Erosion and Binarization according to the command (in Xilinx).

Step 4: Processed. text is generated in source location.

Step 5: Copy the processed file in to MAT LAB current folder.

Step 6: Generate the Processed image, respectively, from text file(text to image conversion in MATLAB).

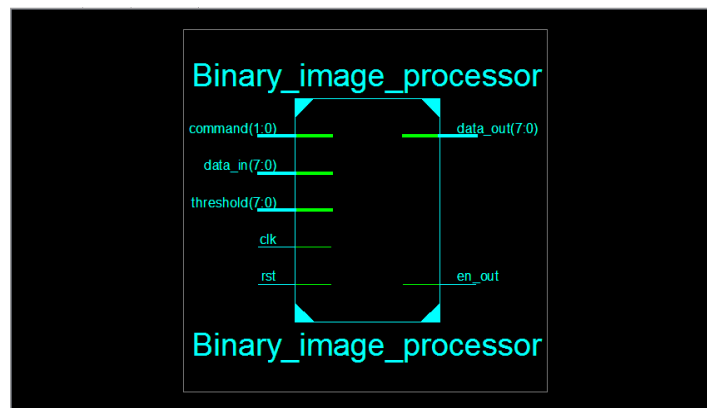


Figure.8 RTL Schematic of binary image processor

A. Device utilization summary of binary image processor

The below table shows the device utilization summary of binary image processing Table 1(a) shows the device utilization summary of the image and 7.3(b) shows timing analysis of the binary image processor. Selected device: XC5VLX110t

Number of Slices	9020 out of 69120	13%
Number of slice LUTs	24523 out of 69120	35%
Number of full used LUT-FFpairs	3575 out of 29968	11%

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Number of bonded IOBs	29 out of 640	4%
Number of BUFG/BUFGCTRLs	3 out of 32	9%

Table 1(a) Device utilization of Binary image processing

B. Timing analysis of Binary image processor

Minimum Period	No path
Speed grade	- 2
Minimum input arrival time before clock	2.581ns
Maximum output required time after clock	4.981ns

Table 1(b) Timing analysis of Binary image processor

VI.CONCLUSION

The proposed binary image processor consists of a reconfigurable binary processing module, including reconfigurable compute units and output control logic, input and output image control units. Hardware architecture of Morphological algorithms for implementing on field programmable gate array(FPGA) chips was proposed. The proposed architecture performs four operations such as median filtering, Dilation, Erosion, and Binarization. The reconfigurable binary processing module has a mixed-grained architecture with the characteristics of high efficiency and performance. The dynamic reconfiguration approach was used to increase the processor performance. Basic mathematical morphology operations and complicated algorithms can easily be implemented on it because of its simple structure. Simulation results and synthesis proposed binary image processor on Xilinx Vertex5 XC5VLX110t FPGA chip demonstrated the efficiency of proposed architecture for image processing of gray scale and binary 256x256 images for real time image processing applications. The processor was coded using VHDL and simulated using Modelsim 6.5.

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