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Design and Implementation of space Vector Modulated Three Level Inverter with Quasi-Z-Source Network

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ABSTRACT: A three level inverters with single quasi z-source neutral point clamped inverter using the space vector modulation technique is proposed in this paper. The proposed inverter has the main features in that the output voltage can be bucked or boosted and in-phase with the input voltage. The quasi z-source concept can be applied to all DC-AC, AC-DC and DC-DC power conversion whether two-level or multi-level. Previous publications have shown the control of a Z-source neutral point clamped inverter using the space vector modulation technique. A three level inverters with single quasi Z-source is proposed in this project. This gives a number of benefits, both in terms of implementation and harmonic performance. The experiment results verified that the inverter has the lower input current harmonics distortion, a high efficiency, as it makes possible to avoid voltage spikes on the switches.

KEYWORDS: Buck–boost, neutral point clamped inverter, space vector modulation (SVM), quasi Z-source inverter.

I. INTRODUCTION

Many industrial applications require higher power converters (inverters) which are now almost exclusively implemented using one of the multilevel types. Multilevel converters offer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters and operation at higher dc voltages using series connection of a basic switching cell of one type or another [1]–[2].Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter, the diode clamped inverter, and the capacitor clamped inverter. Among the three, the three level diode clamped also known as the neutral point clamped (NPC) inverter has become an established topology in medium voltage drives and is arguably the most popular certainly for three-level circuits. However, the NPC inverter is constrained by its inability to produce an output line-to-line voltage greater than the DC source voltage. For applications where the DC source is not always constant, such as a fuel cell, photovoltaic array, and during voltage sags, etc., A DC/DC boost converter is often needed to boost the DC voltage to meet the required output voltage or to allow the nominal operating point to be favorably located. This increases the system complexity and is desirable to eliminate if possible. The quasi Z-source inverter topology was proposed to overcome the above limitations in traditional inverters. The quasi Z-source concept can be applied to all DC-to-AC AC-to-DC , AC-to AC , and DC-to-DC , power conversion whether two-level or multilevel. The quasi Z-source concept was extended to the NPC inverter, where two additional Z-source networks were connected between two isolated DC sources and a traditional NPC inverter. In spite of its effectiveness in achieving voltage buck–boost conversion, the Z-source NPC inverter proposed in is expensive because it uses two Z-source networks, two isolated DC sources, and requires a complex modulator for balancing the boosting of each Z-source network. To overcome the cost and modulator complexity issues, the design and control of an NPC inverter using a single quasi Z-source network was presented. The REC Z-source NPC inverter is expected to find applications in grid connected distributed generation (DG) systems based on renewable energy sources such as photovoltaic systems, wind turbines, and fuel cell stacks [3]. Two DG systems can be connected to the grid with only one REC Z-source NPC inverter, thus reducing the volume and cost while increasing efficiency and facilitating control. The power quality of current injected to the grid is improved because of the three-level structure. It can also find use in adjustable speed drive systems in applications such as conveyor belts, fans, and water pumps [4].In [5], the modulation of the RECZ-source NPC inverter was described using the carrier-based approach. However, the space vector modulation (SVM) approach offers better harmonic performance[6] (compared with carrier-based pulse width modulation (PWM) strategy without zero-sequence voltage injection) and can more conveniently handle overall switching patterns and constraints [7], [8], and it is simple to implement using a DSP [9]. The contribution of this paper is, therefore, the

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development of a modified SVM algorithm for controlling the REC Z-source NPC inverter. The theoretical development is discussed in detail, and simulations as well as experimental results are used to verify the operation of the circuit and proposed SVM-based modulation.

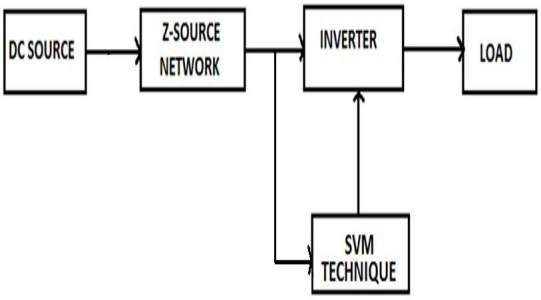

Fig. 1. Schematic of Z-Source inverter

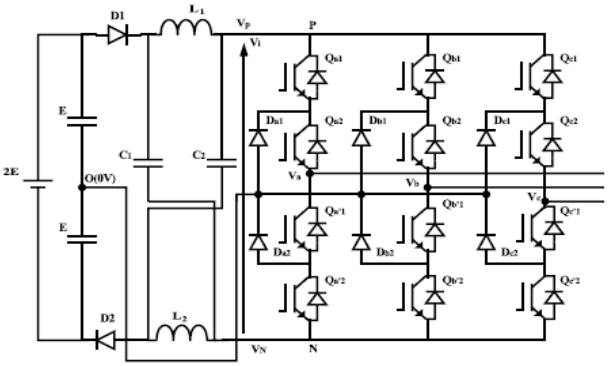

Fig. 2. Circuit of an REC Z source NPC inverter.

II. REVIEW OF QUASI Z-SOURCE CONCEPT

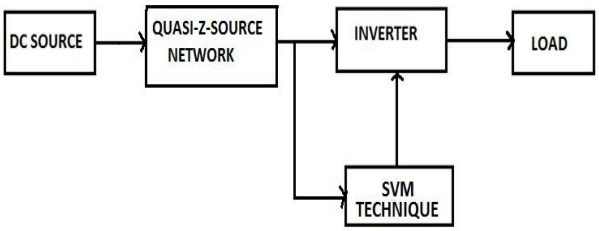

Fig. 3. Structure of the proposed quasi Z source inverter.

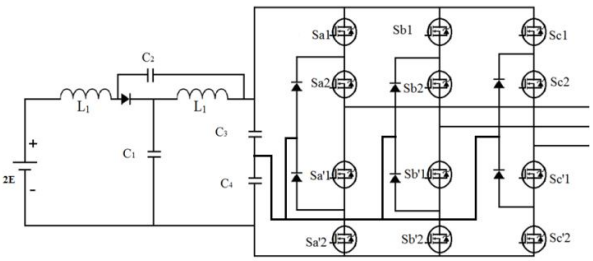

Fig. 4. Circuit of an quasi Z source NPC inverter

III. TOPOLOGY OF QUASI Z-SOURCE NPC INVERTER

To describe the operating principle of the quasi Z-source NPC inverter shown in Fig. 4, we concentrate initially on the operation of one phase leg. The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Switching state "P" denotes that the upper two switches in a phase leg are gated ON, "N" indicates that the lower two switches conduct, and "O" signifies that the inner two switches are gated ON.

However, each phase leg of the Z-source NPC inverter has three extra switching states which resemble the "O" state of the traditional NPC inverter. These extra switching states occur when all the four switches in any phase leg are gated ON [full-shoot-through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower shoot-through (LST)]. These shoot-through states are forbidden in the traditional NPC inverter because they would cause a short circuit of the dc-side capacitors. Again, the Z-source network makes these shoot-through states permissible and provides the means for boost operation.

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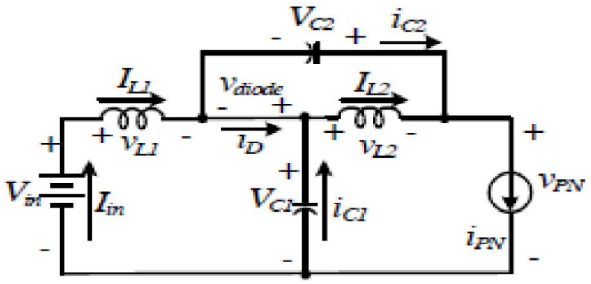

Fig. 5. Equivalent circuit of qZSI in active mode

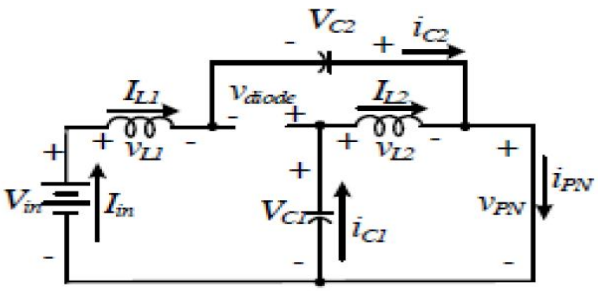

Fig. 6. Equivalent circuit of qZSI in shoot through mode

IV. OPERATING MODES OF QZSI

In the non-shoot through mode, the switching pattern for the qZSI is similar to that of a VSI. The inverter bridge, viewed from the DC side is equivalent to a current source the input DC voltage is available at the DC link voltage input to the inverter, which makes the qZSI behave similar to a VSI.In the shoot through mode, switches of the same phase in the inverter bridge are switched on simultaneously for a very short duration. The source however does not get short circuited when attempted to do so because of the presence LC network, while boosting the output voltage. The DC link voltage during the shoot through states, is boosted by a boost factor, whose value depends on the shoot through duty ratio for a given modulation indexSimilar to the existing qZSI operating principle [11], the system in Fig. 4 also has two operating modes in the continuous conduction mode (CCM).

1) Mode I: This mode will make the inverter short circuit via any one phase leg, combinations of any two phase legs, and all three phase legs in Fig. 4, which is referred to as the shoot through state [11]. As a result, the diode *Dz* is turned off due to the reverse-bias voltage. Its equivalent circuit is shown in Fig. 6. During this time interval, the circuit equations are presented as follows

$$C\frac{dVc1}{dt} = i_B - i_{L2} \quad (1)$$

$$C\frac{dVc2}{dt} = -i_{L1} \quad (2)$$

$$L\frac{diL1}{dt} = V_{in} + V_{C2} \quad (3)$$

$$L\frac{diL2}{dt} = V_{C1} \quad (4)$$

where *iL*1, *iL*2, and *iB* denote the currents of inductors *L*1 and *L*2 and the battery, respectively; *VC*1, *VC*2, and *V*in denote the voltages of capacitors *C*1 and *C*2 and the PV panel, respectively; *C* denotes the capacitance of capacitors *C*1 and *C*2; and *L* denotes the inductance of inductors *L*1 and *L*2.

2) Mode II: This mode will make the inverter operate in one of the six active states and two traditional zero states, which is referred to as the non-shoot-through state [11]. A continuous current flows through the diode *Dz*, and its equivalent circuit is shown in Fig. 6. During this time interval, the circuit equations are presented as follows:

$$C\frac{dVc1}{dt} = i_B + i_{L1} - i_d \quad (5)$$

$$C\frac{dVc2}{dt} = i_{L2} - i_d \quad (6)$$

$$L\frac{diL1}{dt} = V_{in} - V_{C1} \quad (7)$$

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$$L\frac{diL2}{dt} = -V_{C2} \quad (8)$$

where *id* is the load current going to the inverter.

A. Inverter System Model

We define *T*0 as the time interval for Mode I and *T*1 as the time interval for Mode II, with a switching cycle *T*. The shoot-through duty ratio is then defined as *D* = *T*0/*T* , and
T = *T*0 + *T*1.

TABLE 1
Comparison of Current Behavior for Two Inductors

Input and Output Power Relationship	Battery Power	Inductor Currents	
$P_{in}<P_{out}$	$P_B>0$	$i_{L2} < i_{L1}$	$i_{L2} > i_{L1}$
$P_{in}<P_{out}$	$P_B<0$	$i_{L2} > i_{L1}$	$i_{L2} < i_{L1}$
$P_{in}=P_{out}$	$P_B=0$	$i_{L2} = i_{L1}$	$i_{L2} = i_{L1}$

B. Analysis and Comparison

According to (1) and (13), in Fig. 2, the following can be observed.
1) If Pin < Pout, PB > 0, and iL2 > iL1, the battery is discharging.
2) If Pin > Pout, PB < 0, and iL2 < iL1, the battery is charging.
3) If Pin = Pout, PB = 0, and iL2 = iL1, the battery will not have energy exchange.
Fig. 1 shows significantly different performances because the average currents of its two inductors and battery have the following expression:

$$iL2 - iL1 = -iB. \quad (9)$$

Table I summarizes both circuits' current behaviors, which presents inverse current relationships for the two inductors when the battery charges and discharges. In addition, the new topology in Fig. 2 works in the CCM, if

$$iD = iL2 + iC1 - iB > 0 \quad (10)$$

during Mode II; otherwise, it works in the DCM if *iD* = 0 during Mode II.
In steady state, the average current of capacitor *C*1 is zero, and (10) will become

$$iB < iL2 \text{ or } iL1 > 0. \quad (11)$$

The power equation should satisfy the following inequality:

$$PB < Pout. \quad (12)$$

Table 2
Switching combination and switching states for a three level inverter (1 phase leg)

S_{1X}	ON	OFF	OFF
S_{2X}	ON	ON	OFF
S_{3X}	OFF	ON	ON
S_{4X}	OFF	OFF	ON
V_{XO}	$V_{DC}/2$	0	$-V_{DC}/2$
Switching state	P	O	N

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Among the three-level quasi Z-source power converter topologies reported to date, the quasi Z-source NPC inverter implemented using a single *LC* impedance network (see Fig. 4) is considered to be an optimized topology in terms of component count [12], [13]. Referring to Fig. 4, the quasi Z-source NPC inverter is supplied with a split dc source. The middle point *O* is taken as a reference. By controlling the switches of each phase leg according to the combinations presented in Table I, each output phase voltage Vxo (x_{a, b, c}) has three possibilities: Vi/2, 0, and −Vi/2. When the quasi Z-source NPC inverter is operated without any shoot-through states, then Vi is equivalent to 2E. As noted earlier, with this kind of operation, the maximum obtainable output line-to-line voltage cannot exceed the available dc source voltage (2E). Therefore, to obtain an output line-to-line voltage greater than 2E, shoot-through states are carefully inserted into selected phase legs to boost the input voltage to *Vi* > 2E before it is inverted by the NPC circuitry. Thus, the REC Z-source inverter can boost and buck the output line-to-line voltage with a single-stage structure. In [5], two new switching states namely the UST and LST states were identified, in addition to the FST state and the non shoot-through (NST) states (P, O, and N) that had been reported earlier in [10]. Although operation using the FST and NST states possible (termed the FST operating mode), it is generally preferable to use the UST and LST states in place of the FST states (termed the ULST operating mode). The ULST operating mode is preferred because it produces an output voltage with enhanced waveform quality. The simplest FST operating mode requires all four switches in a phase leg (see Table I) to be turned ON. This is not aminimal loss approach since, for example, switching phase A from +E through FST to 0 V would require switches {Sa1, Sa2, Sa'1,Sa'2} changing from {ON, ON, OFF, OFF} through {ON,ON, ON, ON} to {OFF, ON, ON, OFF}. An alternative FST operating mode which gives minimal loss uses two phase legs to create the shoot-through path. This requires, for example, synchronization of the turn ON instants of switches Sa1 from phase A and Sc'2 from phase C at the start of an FST state. Doing so creates a time interval during which switches {Qa1, Qa2, Qa'1} from phase A and {Sc2, Sc'1, Sc'2} from phase C are gated ON simultaneously to create a shoot-through path [35].

However, the output line-to-line voltage obtained using the minimal loss FST approach has higher harmonic distortion (compared to the ULST approach) in its output voltage waveform because the voltage levels produced do not have adjacent level switching [35]. Therefore, in this paper, the ULST operating mode is used for controlling the quasi Z-source NPC inverter. Assuming that the Z-source network is symmetrical (L1 = L2 = L and C1 = C2 = C), then VL1 = VL2 = VL and VC1 = VC2 = VC and the voltage expressions for the NST state are as follows:

NST

$$VL = 2E - VC \tag{13}$$

$$VP = +Vi/2, \quad VN = -Vi/2 \tag{14}$$

$$VI = 2(VC - E) \tag{15}$$

Similarly, the voltage expressions for the UST and LST states are as follows:

UST

$$VL1 = E \tag{16}$$

$$VP = 0\ V,\ VN = E - VC1 \tag{17}$$

LST

$$VL2 = E \tag{18}$$

$$VP = -E + VC2,\ VN = 0\ V \tag{19}$$

We denote the duration of the NST, UST, and LST states by T_N, T_U, and T_L, respectively, and the switching period by *T*. Also, we assume that *TU* and *TL* are equal (this is necessary to ensure symmetrical operation) and denote the total combined UST and LST duration by *T*ULST. At steady state, the average voltage across the inductors is zero; therefore, averaging the inductor voltage over one switching period, we have

$$\frac{(2E-Vc).TN + E.TU + E.TL}{T} = 0 \tag{20}$$

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$$T_N + T_U + T_L = T \quad (21)$$

Solving for *VC* using (20) and (21), we have

$$V_C = 2E \cdot \{ \frac{1-TULST/2T}{1-TULST/2T} \} \quad (22)$$

Substituting (22) into (15), we have the dc-link voltage *Vi* during the NST state as

$$V_{i\text{-}NST} = \{ \frac{2E}{1-TUST/T} \} \quad (23)$$

Similarly, when (22) is substituted into (17) and (19) and noting that Vi = VP − VN , we have the dc-link voltage during the UST and LST states as

$$V_{i\text{-}UST} = V_{i-LST} = \{ \frac{E}{1-TULST/T} \} \quad (24)$$

It is noted from (23) and (24) that the higher dc-link voltage is present during the NST states and it is twice the dc-link voltage available during the UST and LST states, as required.
The fundamental peak ac output voltage *Vxo* ($x_E\{a, b, c\}$) is given by

$$V_{X0} = \frac{M}{\sqrt{3}} . V_{i\text{-}NST} \quad (25)$$

$$V_{X0} = (\frac{1}{1-TULST/T}) \{ \frac{M}{\sqrt{3}}(2E) \} = B' \{ \frac{M}{\sqrt{3}}(2E) \} \quad (26)$$

Where $B \geq 1$ is the boost factor and all the other symbols have their usual meaning.

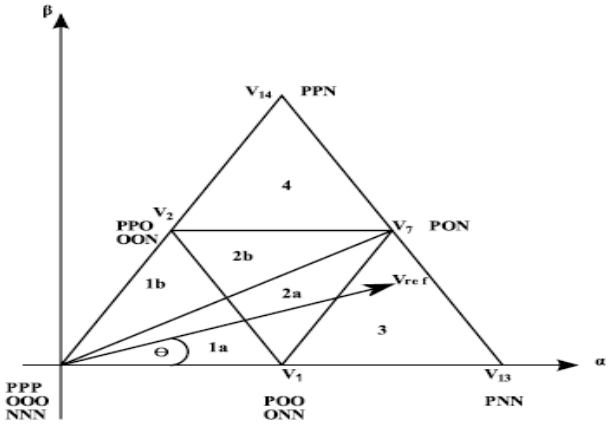

Fig. 7. Space vector diagram of a three-level inverter

V. MODIFIED SVM OF THE REC QUASI Z-SOURCE NPC INVERTER

A. Duty Cycle Calculation

The space vector diagram of a traditional NPC inverter for sector 1 is shown in Fig. 4. The reference vector $\vec{V}_{ref}$ can be expressed as

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$$V_{ref}(t) = \frac{2}{3}[v_{a0}(t)e^{j0} + V_{b0}(t)e^{\frac{j2\pi}{3}} + V_{C0}(t)e^{\frac{j4\pi}{3}} \quad (27)$$

$$d_1.\,\overline{v}_1 + d_2.\,\overline{v}_7 + d_3.\overline{v}_{13} = \overline{v}_{ref} \quad (28)$$

$$d_1 + d_2 + d_3 = 1 \quad (29)$$

$$\overline{v}_1 = \frac{1}{3}.\,(2E) \quad (30)$$

$$\overline{v}_7 = \frac{\sqrt{3}}{3}.\,e^{\frac{j\pi}{6}}.\,(2E) \quad (31)$$

$$\overline{v}_{13} = \frac{2}{3}.\,(2E) \quad (32)$$

$$\overline{v}_{ref} = V_{ref}.\,e^{j\Theta} \quad (33)$$

Substituting (19) into (18), the duty ratios of the nearest three voltage vectors are given by (20), where *M* is the modulation index and $0 \leq \theta \leq \pi/3$

$$d_1 = 2 - 2M \sin\left(\frac{\pi}{3} + \Theta\right)$$

$$d_2 = 2 - 2M \sin \Theta$$

$$d_3 = 2M \sin\left(\frac{\pi}{3} - \Theta\right) \quad (34)$$

A similar procedure is used for calculating the duty ratios of the selected voltage vectors in all the other triangles. To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence. Ideally, a switching sequence is formed in such a way that a high quality output waveform is obtained with minimum number of switching transitions.

VI. SIMULATION RESULTS

The simulation for the space vector modulated three level inverter with Quasi z-source inverter has been done by using the MATLAB/SIMULINK. The conventional Z-source inverter output waveform is shown in Fig. 8.. The input voltage is 150V. The space vector modulated three level inverter with a single Z-source inverter boosted the 170V of the output waveform. It has high total harmonic distortion. The input voltage of the inverter is Fig. 10, Constant 150V is given to the Quasi Z source inverter. The Quasi Z Source inverter is boost the input voltage. qZSI output voltage is shown in Fig. 11.

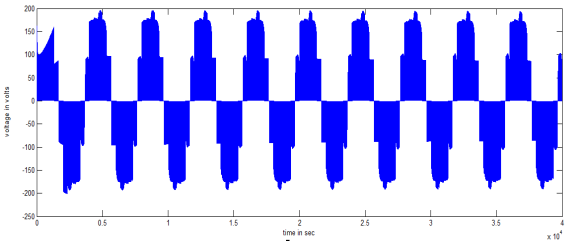

Fig. 8. conventional Z - source output voltage waveform

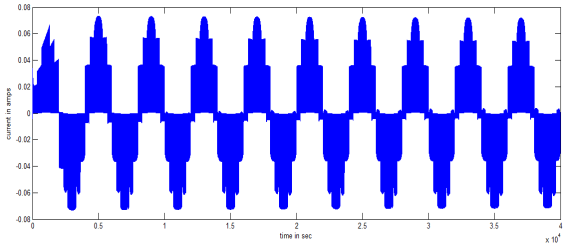

Fig. 9. conventional Z - source output current waveform

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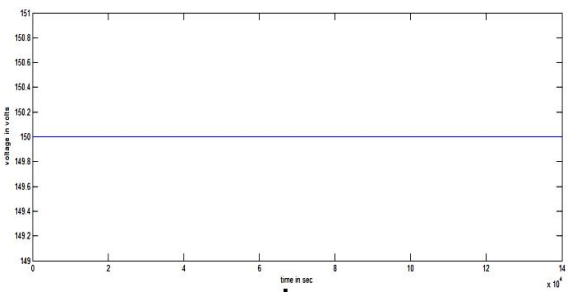

Fig. 10. Input Voltage Waveform

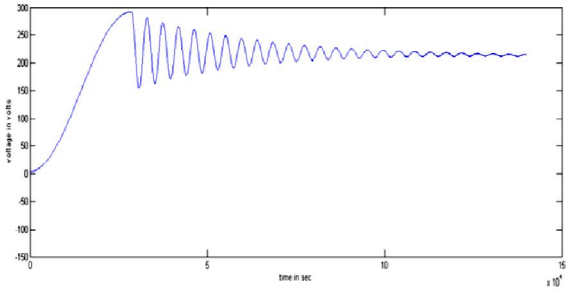

Fig. 11. Quasi Z-Source Inverter Output Voltage

The Quasi Z-source inverter output waveform is shown in Fig. 12. The input voltage is 150V. The space vector modulated three level inverter with Quasi Z-source inverter boosted the 210V of the output waveform. It improves the current and voltage gain. The qZSI current waveform is shown in Fig. 13.

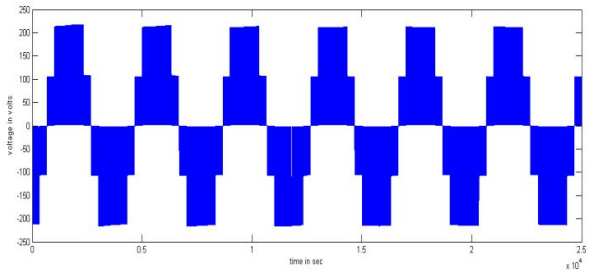

Fig. 12. Quasi Z source inverter output voltage waveform

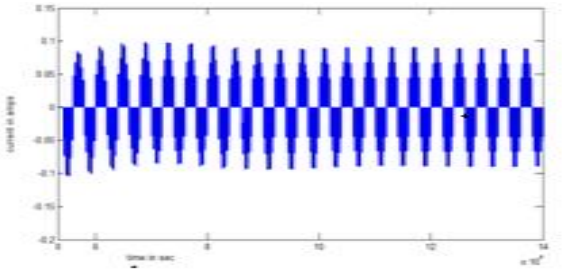

Fig. 13. Quasi Z source inverter output current waveform

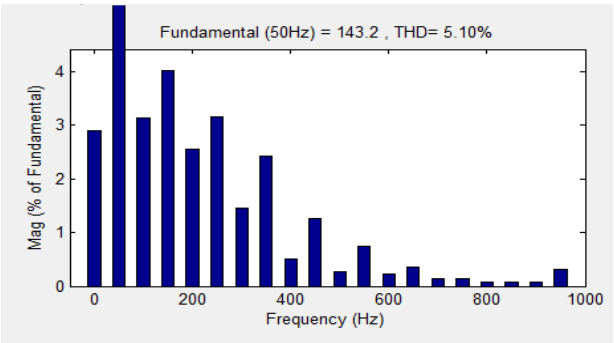

Fig.14. THD waveform

Fig. 14, shows the harmonics present in the output THD value is 5.10%. The harmonic reduction is achieved by selecting the appropriate switching angles. The space vector modulated three level inverter with Quasi Z-source inverter reduces the total harmonic distortion.

VI. CONCLUSION

In this paper, a modified SVM for a quasi Z-source NPC inverter is presented. Using carefully inserted UST and LST states in the traditional NPC inverter state sequence, the quasi Z-Source NPC inverter functions with the correct volt–

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second average and voltage boosting capability regardless of the angular position of the reference vector. The insertion of the shoot- through states was such that the number of device commutations was kept at a minimum of six per sampling period, similar to that needed by a traditional NPC inverter. The presented concepts have been verified in simulations and validated experimentally using a three-phase quasi Z-source NPC inverter prototype.

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