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Design and Implementation of VLSI Fuzzy Classifier for Biomedical Application

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Abstract— In this world diabetes has become one of the greatest deadly diseases. An estimated 347 million people were affected due to this. With numerous problems diabetes also produces epilepsy. It is a brain disorder in which cluster of brain nerve cells signal abnormally. This worst condition leads to identify the precise classifier for the diabetic epilepsy risk level classification. For the classifier reliable fuzzy rule model is used. In the two input rule model heterogeneous fuzzy system and homogeneous fuzzy system have been analysed. With the simplified single input rule model SIRM fuzzy system is proposed. Both the fuzzy system has been individually tested for all the cerebral blood flow (CBF) level through the FPGA which can act as a Reconfigurable computing. The CBF, EEG signal features and aggregation operators are taken as an input parameter. The fuzzy processor is tested for the 200 cases of known diabetic patients and validated for 100 cases. All these were first analysed in matlab, then coded and simulated in VHDL after that synthesized in FPGA. Quality value and performance index has been calculated individually to select the better fuzzy classifier. Simulation and synthesis has been performed in windows and Open source environment. For all the CBF value with minimized false level this system has been checked for the various device families like Spartan and Virtex. The area, power and timing analysis of a fuzzy classifier has been checked out. The FPGA results were compared with matlab results. This result indicates FPGA output closely follows the matlab results. The tuned SIRM with five rules is selected which has the highest performance among all the system with 98.58% and quality value of 36.56. The average performance obtained for the VLSI system is 98.28.

Keywords— Fuzzy processor, simulation, synthesis**.**

I. INTRODUCTION

Fuzzy system provides the technique to deal with uncertainty and granularity. Fuzziness describes the ambiguity of an event and randomness describes the uncertainty in the occurance of an event. It is a nonlinear mapping of inputs to outputs. Fuzzy if then rules is a scheme for capturing knowledge that involves imprecision. The no of rules increases exponentially with the dimension of the input space (no of system variable). This rule explosion is called principle of dimensionality and is a general problem for mathematical models [27]. This problem can be effectively handled by the single input rule model (SIRM). Generally in fuzzy IF THEN ELSE conditions were used. In complex problem no of precedents are ANDed to deal the tough situations. But the no of rules to be used is increased exponentially. Based on no of trials rule model can be reduced to smaller. In this fuzzy processor measured CBF and derived CBF are the two input parameters. Based on the truth value fuzzy variables may take the range of value from 0 to 1. Instead of numeric input values fuzzy system always uses membership function abbreviated as MF [5]. To deal with the crisp input the fuzzy system must convert it into fuzzified quantity. For this purpose fuzzification interface is used[31]. For applying fuzzy rules a rule base block is incorporated [7]. But to provide the results to the outside world defuzzification unit performs the FUZZY to CRISP conversion [2]. To make correct decision the decision making block is added. This is shown in Figure1.

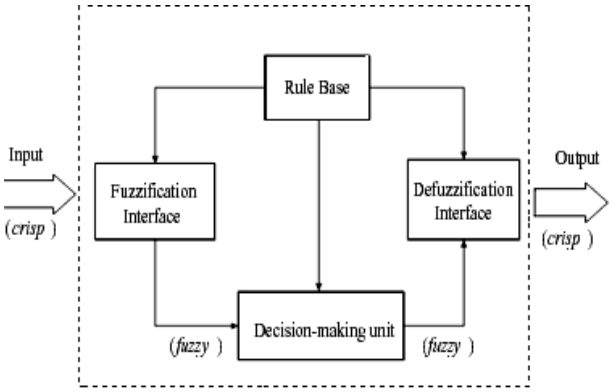

Fig. 1Basic steps in fuzzy system

After simulating the fuzzy processor code it is synthesized through FPGA [29].

II. FUZZY PROCESSOR

Methodology of a fuzzy processor

The fuzzy processor inputs are cerebral blood flow (CBF), Electroencephalogram (EEG) signal. This system consists of various membership functions which includes bell membership function also. To find the slope of the bell MF aggregation operators were used. The results obtained from one hundred clinically well defined test cases are used for the system training. The purpose of the work is to simulate and synthesis a fuzzy processor for a biomedical application. Specifically in risk level classification of diabetic patients. Since this risk level leads to epilepsy or brain disorder[15]. Energy, peaks and spikes and sharp waves and events are extracted from the EEG signal are denoted as y1,y2,y3,y4,y5. The parameters such as index of convulsions, seizure timings and total body fatigue are the variable X. For the raw data EEG signal bipolar channels of the count 16 were used. 200hz is fixed for the sampling rate. The 17 test conditionas were clustered by the R. Yager's ordered weighted aggregation (OWA) method [1]. The measured CBF will have five linguistic levels such as Very low, Low, Medium, High, Very high [10].

Fuzzy processor input membership function

Based on the CBF mechanism as CBF increases to 70%, the oxygen concentration on the blood stream reduced by 30%. This epileptic convulsion risk is increased in diabetic patients [3]. EEG can easily detect the oxygen delivery and utilization in brain [4]. This indicates correlation between CBF and EEG signals.

The linguistic fuzzy membership functions for the heterogeneous system [26] are illustrated with the Figures. Figure 2 shows the Input membership function (measured CBF). Figure 3 shows the Input membership function (derived CBF). Figure 4 shows the Output membership function (epilepsy risk level). In all these membership function X axis denotes CBF level and Y axis denotes the membership grade.

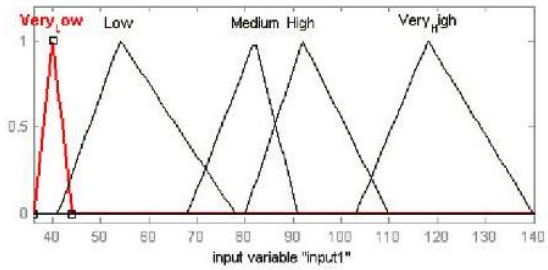

Fig. 2 Input membership function (Measured epilepsy CBF)

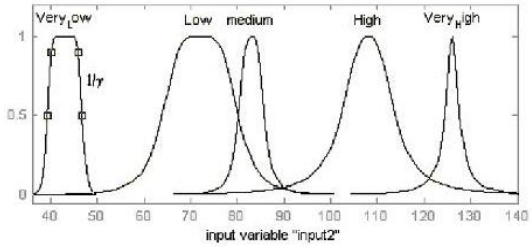

Fig. 3 Input membership function (derived epilepsy CBF)

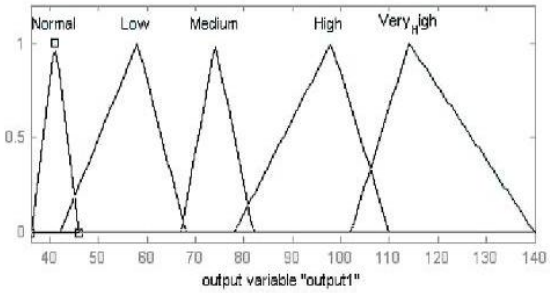

Fig. 4 Output membership function (epilepsy risk level)

Heterogeneous fuzzy rules

Mamdani type system with two inputs and one output is the basic for this fuzzy processor [13]. After processing the fuzzy Rules output must be converted into corresponding numeric values. COG (Centre of gravity) defuzzification is used here. The measured CBF input is fuzzified with five linguistic variables like very low, low, medium, high, very high using triangular membership functions [18]. The other input is from EEG signal with the bell shape membership function. Here aggregation operators are used as conditioning tools. Those are used for deriving slope of the bell shape MF. This fuzzy system performs well with the following five Fuzzy Rules (Fr) in the rule base such as [6]

Fr1: *IF CBF is very low AND epilepsy CBF is very low, THEN output epilepsy risk level is normal*

Fr2: *IF CBF is low AND epilepsy CBF is low, THEN output epilepsy risk level is low risk*

Fr3: *IF CBF is medium AND epilepsy CBF is medium, THEN output epilepsy risk level is medium risk*

Fr4: *IF CBF is high AND epilepsy CBF is high, THEN output epilepsy risk level is high risk*

Fr5: *IF CBF is very high AND epilepsy CBF is very high, THEN output epilepsy risk level is very high risk*

III. SIRM FUZZY PROCESSOR

A. Single Input Rule Model

The conventional fuzzy inference model which puts all the input items into the antecedent part of fuzzy rule, causes the total number of possible fuzzy rules to increase exponentially with the number of the input items and has difficulty in setting up each rule [12]. The SIRM's dynamically connected fuzzy inference model is applied, to over come these problems. The SIRM fuzzy processor is given in Fig. 5.

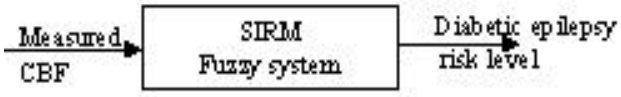

Fig. 5 SIRM fuzzy system

The applied SIRM fuzzy system is designed with five rules in the rule base and measured CBF as the only input.

SFR 1) *IF CBF is very low THEN output epilepsy risk is normal*

SFR 2) *IF CBF is low THEN output epilepsy risk is low risk*

SFR 3) *IF CBF is medium THEN output epilepsy risk is medium risk*

SFR 4) *IF CBF is high THEN output epilepsy risk is high risk*

SFR 5) *IF CBF is very high THEN output epilepsy risk is very high risk*

The membership function of measured CBF is bell shaped and slopes function (1/γ) is embedded with EEG signal information . The output epilepsy risk level of this system uses triangular membership function. The input membership function of the SIRM fuzzy system is shown in Fig. 6.

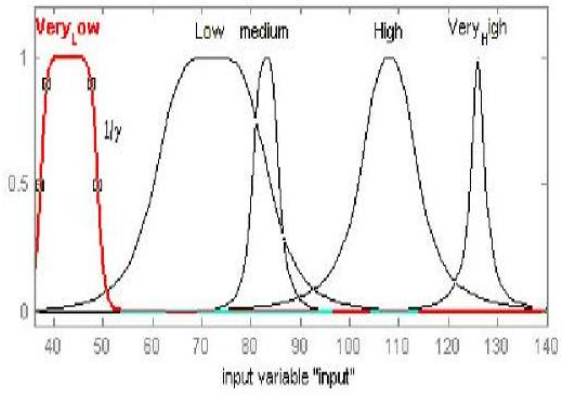

Fig. 6 SIRM input membership function

B. Literature survey

This VLSI fuzzy processor has been involved in various application like medical diagnosis, High Energy Physics Environment (HEPE), Biomedical application.

A review on VLSI based fuzzy processor is explained in the paper. Here all the fuzzy processor which uses VLSI for its coding and implementation were discussed in detail [25]. In those discussion application may different. But all those uses both fuzzy and VHDL tool.

VLSI fuzzy processor which is capable of dealing with complex fuzzy inference systems is proposed in this paper [8]. Inference includes the rule chaining process also. Processor is made up of a no of pipelined stages. Its performance is in the order of 2 MFLIPS with 256 rules, eight inputs, two chained variables, and four outputs and 5.2 MFLIPS with 32 rules, three inputs, and one output with a clock frequency of 66 MHZ. Hardware description languages with a predefined function library is utilized in VHDL modeling of fuzzy system. A generic field-programmable logic device (FPLD) based fuzzy logic system aimed at high-speed applications is focused in this paper [5]. It can be easily customized practically for any application [21].

This fuzzy processor is initially implemented in mat lab and performance analysis like quality value and performance index has been done. A diabetic neuropathy –A case study is discussed in this paper [11]. They simulated the numeric values and checked with the previous results [20]. Fuzzy processor condition is simulated with reduced false level [12]. Author pioneered fuzzy processor diagnosis purpose to find BMI, Glucose, Urea, Creatinine, Systolic and diastolic blood pressure [19]. The generalized trapezoidal membership function used here for the neural network tool analysis [24].

To deal with the great amount of information fuzzy processor exploits the parallism inherent in fuzzy inference which is described in paper [22]. Floating point arithmetic approach fuzzy processor is explained by this author which follows the basic steps in fuzzy system [23]. A review on all the fuzzy processor based on VLSI is described in the paper [25].

This work emphasis on heterogeneous and homogeneous fuzzy processor. The simulation and synthesis condition in windows and FOSS environment. For a convenience only the heterogeneous system is discussed.

This work also describe about design statistics, device utilization summary, power

C. Simulation windows in XP

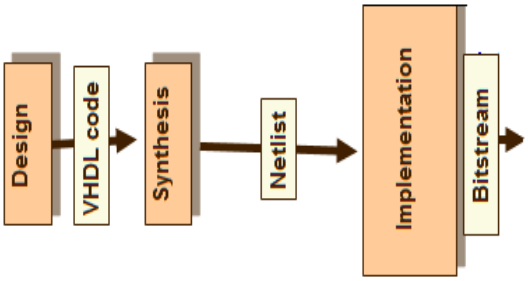

Fig. 7 VHDL design steps

FPGA's are the perfect rapid prototyping of digital circuits. These are used to implement the required logic in a chip. Basic steps in VHDL design steps are coding, synthesis, netlist generation and implementation [32]. Those process are shown in figure 7. Here logic synthesis used to convert VHDL description into netlist. Once the design is implemented a file must be created that FPGA can understand. That is termed as bitstream. The bit file can be downloaded directly to the FPGA. Fuzzy system is simulated in VHDL and synthesized for various CBF levels.

Here the membership function is checked for continuous range of CBF levels. For an example in bell MF if the input CBF is 81 then the fuzzy systems has to identify under which linguistic the CBF falls. If the input CBF falls under more than one linguistic it will be calculating all the function values based upon the aggregation operator and output is produced. Here maximum operator is used for the final function value fixation. In Figure 8 lower CBF value has been applied.

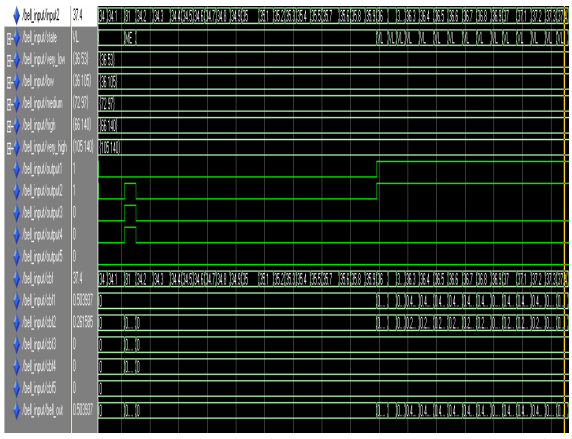

Fig. 8. Fuzzy system simulation window for lower Values of CBF in XP

The fuzzy system performance has been evaluated for all the linguistic levels with maximum values. For a set of random CBF value simulation window has been displayed in Fig. 9.

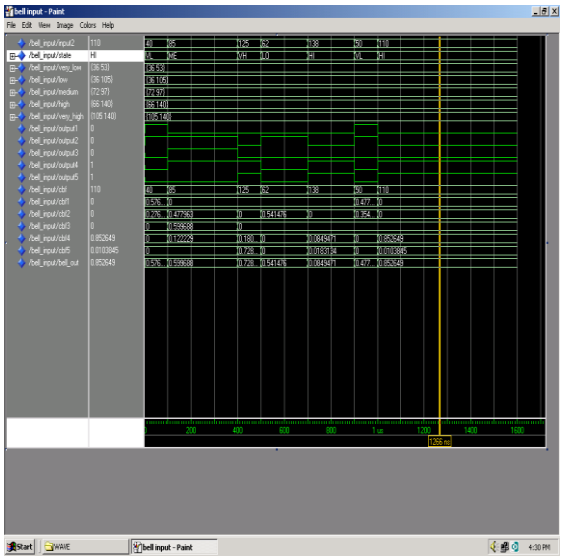

Fig. 9 Fuzzy system simulation window for random Values of CBF in XP

Figure 10 shows the internal diagram of FPGA. It consists of number of CLB 's which can be easily programmed.

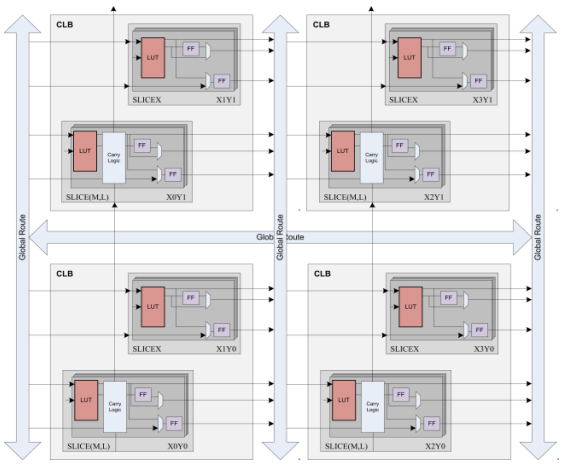

Fig.10. Internal block of FPGA

Each CLB contains two sets of the 4 input LUT, any 4 I/P logic function or (16bitx1) synchronous RAM (SLICEM)only carry and control, Fast arithmetic logic Multiplier and multiplexer logic, Storage element, Latch or Flip Flop, Set or reset, True or inverted input. Each LUT can implement any function of 4 input.

Once the fuzzy system VHDL code gets simulated, it is synthesized through Xilinx ise 9.1i tool. If this process is successful Spartan device gives the impact window as a result. It is given in Fig 11.

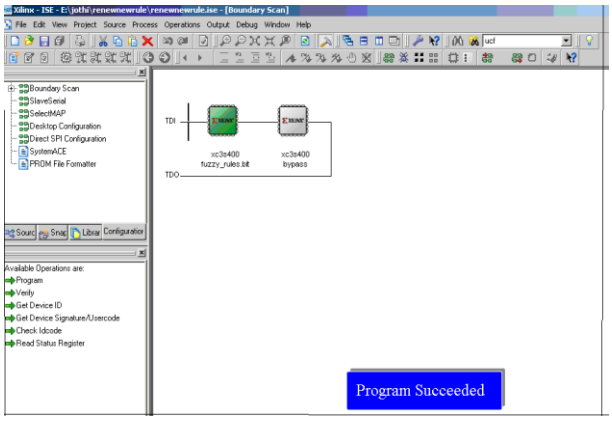

Fig.11. Impact window for the fuzzy processor

D. Simulation and Synthesis windows in FOSS

This same VHDL code was simulated and synthesized through xilinx ise 9.1i in FOSS (Free and Open Source Software) is shown in Fig. 12. It is liberally licensed software to grant the the source code access. Its installation also becomes easier with virus free condition. All the fuzzy system homogeneous and heterogeneous were first simulated.

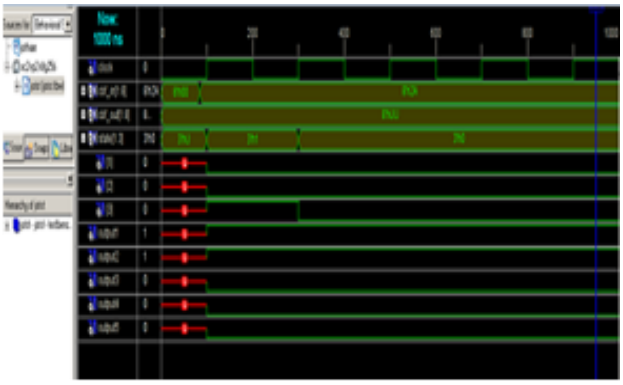

Fig. 12. Synthesis window in FOSS

After synthesizing we can obtain two types of schematics. Those are RTL and technology schematics. The technology schematic (Tech schematic) gives in depth information about the function implemented through that logic. Net list generated by the Xilinx Synthesis Tool is available in technology view. It also gives karnaugh map with the related truth table. Configurable logic blocks (CLB) constitute the main resource for implementing synchronous as well as combinational circuits [16]. Each CLB contains four slices and each slice contains two LUTs to implement the logic [28]. That is given in Fig. 13.

The graphic representation of the design is denoted by RTL schematic (Register transfer level). Derivation of main logic construction is given in RTL view. It is a schematic representation of the pre optimized design in terms of generic symbols like adder, multiplier, counter independent of Xilinx device. Where schematic denotes a hierarchical design representing a design in terms of user and library components.

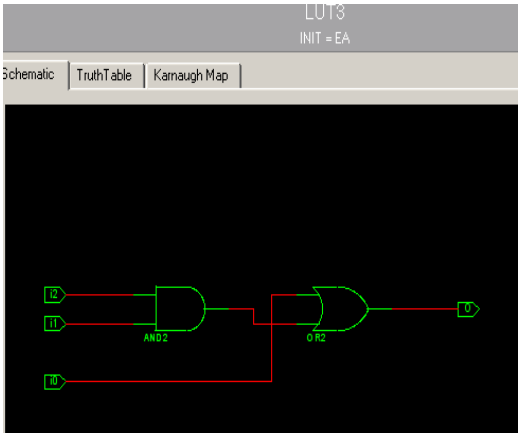

Fig.13. Schematic of a LUT

The karnaugh map for the one of the logic in fuzzy system is shown in Fig. 14.

The INIT attribute with an appropriate number of inputs must be attached to LUT to specify its function. Instead of normal input, the hexadecimal equivalent is used here.

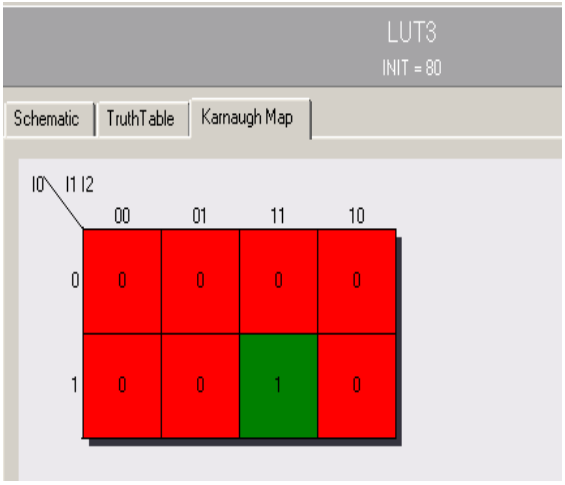

Fig. 14. K map of the fuzzy system

During this step, XST tries to recognize as many basic macros as possible to create a technology specific implementation.

IV. RESULTS AND DISCUSSION

A. HDL Synthesis macro statistics :

During this step, XST performs advanced macro recognition and inference like recognizing dynamic shift registers, implementing pipelined multipliers, coding state machines etc. HDL synthesis macro statistics is given in TABLE. 1

TABLE. 1. HDL SYNTHESIS MACRO STATISTICS

Macro statistics	Bell MF	Tri MF	Fuzzy system
#REGISTERS	13	7	20
1 bit register	10	5	15
3 bit register	1	1	2
32 bit register	1	0	2
8 bit register	1	1	1
#COMPARATOR	15	10	25
8 bit comp or equal	5	5	10
8 bit comp less equal	5	5	10
32 bit comp	5	0	5

Advanced HDL synthesis macro statistics is given in table 2.

TABLE. 2. ADVANCED HDL SYNTHESIS MACRO STATISTICS

Macro statistics	Bell MF	Tri MF	Fuzzy system
#Registers	5	15	20
FF	5	15	20
#Comparator	10	15	25
8 bit comp or equal	5	5	10
8 bit comp less equal	5	5	10
32 bit comp	0	5	5

Design Statistics for fuzzy system
IOs : 25

Cell Usage :
BELS : 22
GND : 1
LUT2 : 1
LUT3 : 5
LUT4 : 12
MUXF5 : 2
VCC : 1
FlipFlops/Latches : 5
FDR : 5
Clock Buffers : 1
BUFGP : 1
IO Buffers : 24
IBUF : 8
OBUF : 16

Design Statistics for bell MF
IOs : 18

Cell Usage :
BELS :34
GND :1
INV : 5
LUT3 :8
LUT3_L : 1
LUT4 :15
MUXF5 :3
VCC :1
FlipFlops/Latches:14
FD : 1
FDR : 12
FDS : 1
Clock Buffers : 1
BUFGP : 1
IO Buffers : 17
IBUF : 8
OBUF : 9

BEL denotes Basic Elements that make up a CLB, IOB, Block RAM, FF. Here LUT2 denotes 2 bit LUT with general output. LUT3 specifies 3 bit LUT with general output. LUT3_L notifies the 3 bit LUT with local output. MUXF5 mentions the primitive 2 to1 LUT multiplexer with general output. Where FD denotes D FF [14], FDR for D FF with Reset. Buf GP is Global clock buffer. Table III shows the power report for the implementation of fuzzy system. Total power is 80.98mw. Here Vccint is the main power supply for the FPGA'S internal logic. To optimize the FPGA function Vccaux is used.

B. Quality value

The quality value Q_v is defined as [10]

.....(1)

Where C is the scaling constant.

R_{fa} is the number of false alarm per set

T_{dly} is the average delay of the onset classification in seconds

P_{dct} is the percentage of perfect classification

P_{msd} is the percentage of perfect risk level missed

0.2- constant

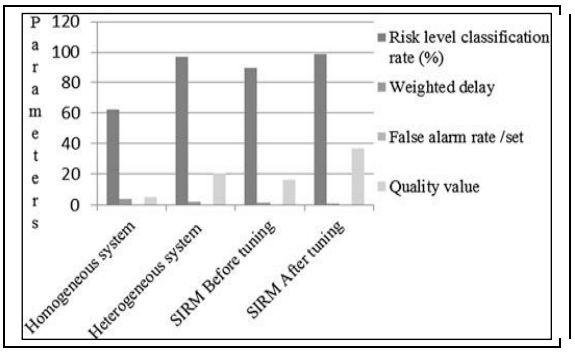

Fig.15. Performance of fuzzy system

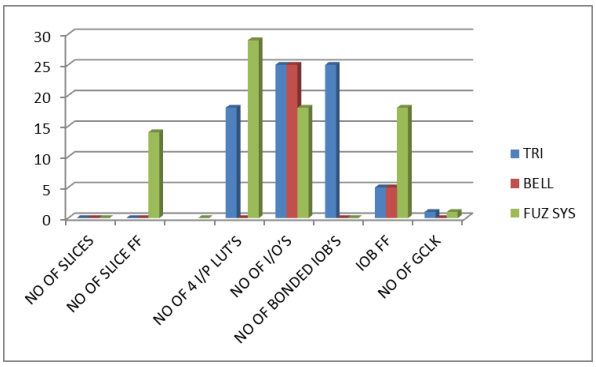

Fig.16. Device utilization

It is observed from the Fig. 15 that the two input fuzzy techniques are inherited with maximum weighted delay and they are slow in their classification response. The tuned SIRM fuzzy system is the best one based on the lowest delay, higher performance and higher the quality value of all the four fuzzy systems used for epilepsy risk level classifications.

TABLE. 3. FUZZY SYSTEM PERFORMANCE IN TERMS OF AREA, PERIOD, SPEED

Device family: Spartan Target Device: Xc3s500 E Package: FG320	Membership Function	Area [LUT]	Minimum Period (ns)	Speed (MHZ)
	Triangular	18	-	-
	Bell	29	2.787	358.815
	Fuzzy system	25	2.739	365.050

In TABLE. 3. Area utilized by the fuzzy system is mentioned in terms of LUT's. And the speed is given in MHZ [30].

Schematic, K Map, Truth table has been obtained for the homogeneous system, heterogeneous system which includes triangular MF, bell MF. It shows that only few parts of the resources were used to implement the logic. Device utilization has been analyzed not only for fuzzy system but also for triangular membership function and bell membership function. Since in SIRM only one MF will be used. Here slices contains LUT's and storage element [20,28].

Fig. 16 shows the diagrammatic representation of the device utilization. Where TRI denotes the Triangular membership function and FUZ SYS represents the fuzzy system. BELL denotes bell membership function.

V CONCLUSION

The heterogeneous and homogeneous fuzzy system is simulated and synthesized for the input CBF values using Spartan3E device XC3S500E target device FG320 package in Xilinx ise 9.1i UBUNTU 10.1 open source environment. This performance results closely follows the previous MATLAB results. Using synthesis process RTL view and technology view has been analyzed with the power reports and Device utilization summary. FPGA synthesis closely follows the previous results. The methodology proposed and FPGA results will aid in ASIC design of the fuzzy processor. Based on the area, power, speed reports a fine tuning can be given to the fuzzy processor design to obtain minimum power, smaller area and higher speed. Further focus on this work is to design optimized fuzzy processor using GA, NN tool.

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