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Design of Double Tail Comparator for High Speed ADC

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ABSTRACT-The demand for high speed comparators will increase the efficient operations of ADC architectures. The double tail comparator is a newly proposed that operates with reduced delay in 65-nm CMOS technology with a power supply of 0.248mW and with a clock frequency of 540Mhz.The layout simulation in Microwind software 3.1 confirm the analysis results of double tail comparator. The major objective of the paper aims at analyzing the efficiency of Successive Approximation Register as it is the slowest Analog-to-Digital comparator by implementing the double tail comparator in it. This analysis aims at reducing the delay of SAR.

KEYWORDS-analog to digital comparator, double tail comparator, Successive approximation Register.

I. INTRODUCTION

Comparator plays an important role in most of the ADC. Many high speed ADC, such as flash ADC require high speed, low power comparator with small chip area. The amplifier of high-impedance differential input stage is designed where the figure of merit of 0.7 V_{DD} input dc level is optimal regarding speed and yield. The supply voltage also decreased up to 70% in 130nm CMOS technology with offset voltage decrease from 19 to 8.5mv without affecting the delay(1). Some ADC architectures uses a positive feedback which results in the voltage variations disturbing the input voltage which is kickback noise(2). Insertion of sampling switched and asynchronous reset of sampled input voltages are the two techniques involved in it for the rectification purpose. A new linear type back-to-back inverter architecture is developed to eradicate the mismatch occur in latch comparator offset due to load capacitor and analyzed in 0.18µm CMOS technology by using HSPICE simulation(3). The sampled rate of the comparator is increased to 40Gb/s by a supply voltage of 1.2V and implemented in 0.11µm CMOS technology. By the new building block which consists of front-end sampler, regenerative stage and clock amplifier the sample rate is increased with reducing the bit error rate less than 10^{-12}(4). Noise in comparator circuit affects the efficiency of the comparator. A time analysis is proposed that accounts for noise analyses. The results are validated by comparison with electrical simulation and measurement of ADC prototypes based on the reference comparator architecture implemented in 0.18µm and 90nm CMOS technology(5). The offset occurs due to the mismatch of µcox and Vth and also by parasitic capacitances. By the analytical expression and simulation through BSIM3 and SPICE level 1 it is reduced(6).

By using simulation algorithm of RF circuit simulation the sampling and decision operation of clock comparator random decision errors are removed. LPTV system are involved in reducing RDE and analyzed in 0.73Vrms for dc inputs(7). Comparator delay is reduced with a supply voltage of 0.65V by positive feedback. The high impedance input, rail to rail output swing, no static power consumption are followed to achieve the low delay and achieve a bit error rate of 10^{-9} at 1.2V. (8).

The rest of the paper is as follows. Section II involves in analyzing the operation of conventional comparator in Microwind software. Section III follows the operation of proposed double tail comparator and section IV describes about the SAR. Finally Section V describes the future work of the project.

II. CONVENTIONAL DYNAMIC COMPARATOR

Most of the A/D converters uses the comparator with high input impedance, rail to rail output swing and no static power consumption. Figure 1 shows the schematic diagram of conventional dynamic comparator. The operation

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of the conventional dynamic comparator occurs in two phases .i.e., reset phase and comparison phase. During the reset phase when the C_{LK}=0, the transistors M_7 and M_8 is on where M_{tail} is off. So the output nodes out_n and out_p are charged to V_{DD}. During the comparison phase when the C_{LK}=1, the transistors M_7 and M_8 are off condition and M_{tail} is on. Output voltages which has been precharged to VDD starts discharging according to the input provided (V_{INN} and V_{INP}). If V_{INP}>V_{INN}, out_p discharges faster than out_n, hence when out_p falls down to V_{DD}-$|V_{th}|$ before out_n, the corresponding pmos transistor M_5 will turn on initiating the latch regeneration caused by back to back inverters. Thus out_n pulls to V_{DD} and out_p discharges to ground. If V_{INP}<V_{INN}, the circuits works vice versa.
The two types of which accounts for the operation of the comparator are capacitor delay (t_0) and latch delay (t_{latch}).
The delay t_0 of the capacitance C_L occur until the first
p-channel transistor(M_5/M_6).

The delay of load capacitance is given by

$$to=\frac{CL|VTHP|}{I2}$$

$$=2\frac{CL|VTHP|}{Itail} \qquad (1)$$

Where

$$I2=Itail/2 +Iin$$

$$= Itail/2 +gm1,2\ Vin$$

for small differential input(V_{in}), I_2 can be approximated to be constant and equal to the half of the tail current.

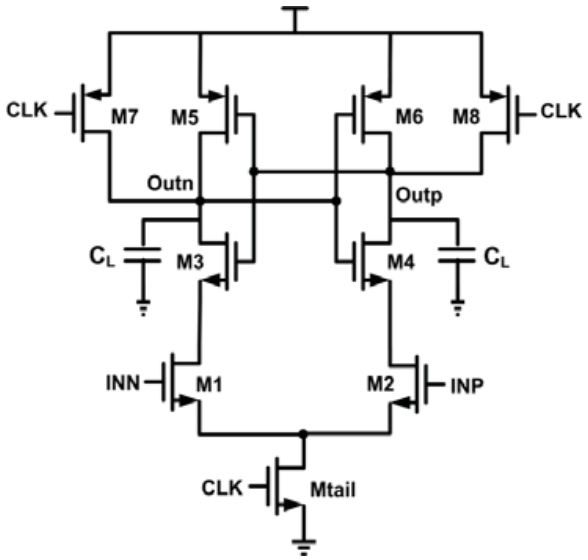

Fig.1.Schematic Diagram of Conventional Dynamic Comparator.

In order to find the delay of the latched (t_{latch}), it is assumed that a voltage swing of Vout=V_{DD}/2. Half of the power supply is considered to be the threshold voltage of the comparator.

$$t_{latch} = \frac{CL}{gm,eff}.\ln(\frac{\Delta vout}{\Delta vo})$$

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$$= \frac{CL}{gm,eff} . \ln(\frac{VDD/2}{\Delta V0}) \quad (2)$$

Where $g_{m,eff}$ is the effective transconductance of the back to back inverters. The initial voltage difference (Δ_{V0}) can be calculated by

$$\Delta_{V0}=|Voutp(t=t_0) - Voutn(t=t_0)|$$

$$=|Vthp|- \frac{I2\ to}{CL}$$

$$=|Vthp|(1- \frac{I2}{I1}) \quad (3)$$

The current difference is Iin=$|I_1-I_2|$, between the drains of different nodes.

$$\Delta_{V0}=|V_{thp}| \frac{\Delta Iin}{I1}$$

$$=2|V_{thp}| \frac{\Delta Iin}{Itail}$$

$$=2|V_{thp}| \frac{\sqrt{\beta 1,2 Itail}}{Itail}.\Delta Vin$$

$$=2|V_{thp}|\frac{\sqrt{\beta 1,2}}{\sqrt{Itail}} . \Delta Vin \quad (4)$$

In this $\beta_{1,2}$ is the input transistor current factor and I_{tail} is a function of input common-mode voltage(V_{cm} and V_{DD}). The total delay is addition of delay occur due to the load capacitance and delay during the latch regeneration.

$t_{delay} = t_0 + t_{latch}$

$$=2\frac{CL|Vthp|}{Itail} + \frac{CL}{gm,eff} . \ln(\frac{VDD}{4|Vthp|\Delta Vin} . \frac{\sqrt{Itail}}{\beta 1,2}) \quad (5)$$

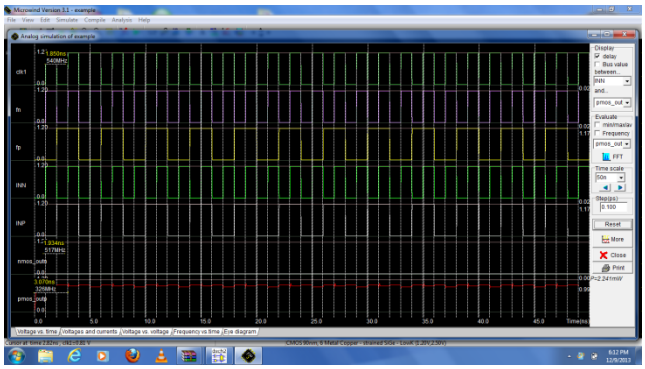

Fig.2.Simulation Result of Conventional Dynamic Comparator using Microwind.

The figure.2 shows the simulation result of conventional dynamic comparator using Microwind. The total delay is directly proportional to the comparator load capacitance C_L and inversely proportional to the input difference voltage(Vin). Simulation results show that the power consumption has reduced to 50% and speed and yield of the comparator is improved.

The advantages of the conventional dynamic comparator are high input impedance, rail to rail output swing and no static power consumption. The comparator also suffers from serious disadvantages that stacked transistor

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consume high supply voltage for proper delay. Also that it consists of only one tail which is the current path Mtail, which defines the current for both differential amplifier and the latch. So it leads to some delay in the passage current from one latch to another latch or from one node to ground.

III. DOUBLE TAIL COMPARATOR

The double tail comparator architecture is used in low voltage applications because of its better performance in delay reduction. The main idea of the double tail comparator is to increase Δ_{V0} which will also increase $V_{fn/fp}$. So the control transistors M_{c1} and M_{c2} are added to the first stage in parallel to M_3 and M_4 but in cross coupled manner.

A.OPERATION OF THE DOUBLE TAIL COMPARATOR:

Figure 3 shows the schematic diagram of double tail comparator. The operation of the double tail comparator occurs in two phase which are reset phase and decision making phase. During reset phase C_{LK}=0, M_{tail1} and M_{tail2} are in off state, M_3 and M_4 are in on state which pulls both the nodes fn and fp to V_{DD}. so according to the input suppose $V_{inp}>V_{inn}$, then fn drops faster than fp. As long as fn continues falling, the corresponding pmos control transistor starts to turn on, pulling fp node back to V_{DD}. So another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. The control transistor M_{c1} is on when M_{c2} is grounded which results in static power consumption so two more switches(M_{sw1} and M_{sw2}) are added.

During the decision making phase the nodes fn and fp are precharged to V_{DD} and it starts its different discharging. As soon as the comparator detects that one of the fn/fp is discharging faster, control transistor will help to increase the voltage difference. In other words, the operation of the control transistors with the switches emulates the operation of the latches

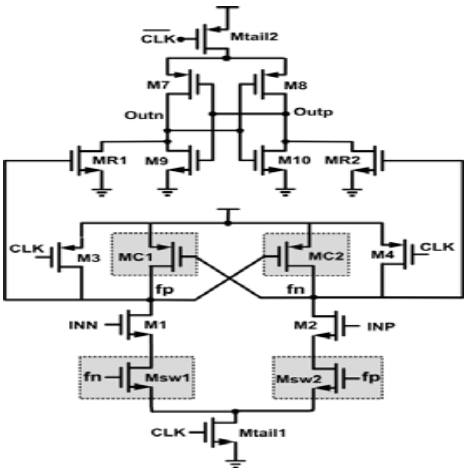

Fig.3.Schematic Diagram of Double Tail Comparator

B.DELAY ANALYSIS:

Delay of the double tail comparator is low comparator to conventional dynamic comparator. The two major factors that makes the comparator are improvement in the initial output voltage difference(v0) at the initiation of the operation and enhancement in the effective transconductance (g_{meff}) of the latch.

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1.INCREASING OF ΔV_0:

Δ_{V0} denotes the initial voltage difference between two latches. It is desirable to have biggerΔ_{V0} results in less regeneration time. The value of output voltage difference is given by

$$\Delta V_0 = Vthn\frac{\Delta Ilatch}{IB1}$$

$$= 2Vthn\frac{\Delta Ilatch}{Itail\,2}$$

$$= 2Vthn\frac{gmR\,1,2}{Itail\,2}.\Delta\frac{Vfn}{Vfp} \qquad (6)$$

Vfn/fp at t=t0 is given by

$$\frac{\Delta Vfn}{\Delta Vfp} = \Delta Vfn(p)0\exp(AV-1)\,t/\tau \qquad (7)$$

On substituting (7) in (6)

$$\Delta V0 = 4Vthn|Vthp|\frac{gmR\,1,2\;gm\,1,2\Delta Vin}{Itail\,2.Itail\,1}\exp(\frac{Gm,eff\,1,t0}{CL,fn(p)})$$

2.INCREASING OF EFFECTIVE TRANSCONDUCTANCE

In this comparator, the first stage output nodes (fn/fp) will charge up back to V_{DD} at the beginning of the decision making phase, will on one of the intermediate stage transistor, making transconductance increased. The equation of latch is as follows,

$$t_{latch} = \frac{CLout}{Gm,eff+gmR\,1,2}.\ln(\frac{VDD/2}{\Delta V0}) \qquad (8)$$

Finally, by including both effects , the total delay of the comparator is

$t_{delay} = t_o + t_{latch}$

$$= 2\frac{VthnCLout}{Itail\,2} + \frac{CLout}{gm,eff+gmr\,1,2}.\ln(\frac{VDD/2}{\Delta V0})$$

$$= 2\frac{VthnCLout}{Itail\,2} + \frac{CLout}{gm,eff+gmr\,1,2}$$

$$X\ln(\frac{VDD/2}{4Vthn|Vthp|\frac{gmR\,1,2\;gm\,1,2\Delta Vin}{Itail\,2\,Itail\,1}\exp(\frac{Gm,eff\,1.t0}{CL,fn\,(P)})}) \qquad (9)$$

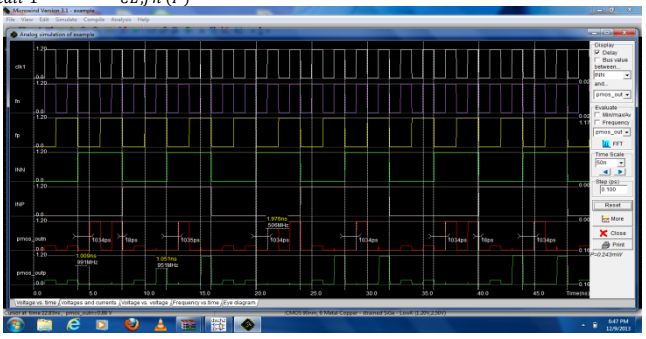

Fig.4. Simulation of Double Tail Comparator

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Figure 4 shows the simulation result of double tail comparator. By comparing the expressions the double tail comparator takes an advantage of an inner positive feedback in double tail comparator operation, strengthen the whole latch regeneration. The speed improvement is even more obvious in lower supply voltages.

On comparing with the conventional dynamic comparator, it consists of two M_{tail} which is the path way for current and so passage of current can faster and need not depends on the other latch. The capacitance effect is also highly reduced in double tail comparator compared to the previous one.

IV. SUCCESSIVE APPROXIMATION REGISTER

The conversion time is maintained constant in SAR type A/D converter, and it is proportional to the number of bits in the digital output, unlike the other converters. The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value trying one bit at a time, beginning with the MSB.
This type of A/D converter operates by successively dividing the voltage range by half, as explained in the following steps:

(i) The MSB is initially set to 1 with the remaining three bits 0. The digital equivalent is compared with the unknown analog input voltage.

(ii) If the input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and he second MSB is set to 1.

(iii) Comparison is made as given in step1 to decide whether to retain or reset the second MSB. The third MSB is set to 1 and the operation is repeated down to the LSB and by this time, the converted digital value is available in SAR.

This method uses a very efficient search strategy to complete an n-bit conversion in just n-clock periods. Therefore, for an 8-bit successive approximation type A/D converter, the conversion requires only 8 cycles, irrespective of the amplitude of analog input voltage. The circuit employs the a SAR which finds the required value of each successive bit by trial and error method. The analog output equivalent of the D/A converter is applied to the noninverting input of the comparator, while the other input of the comparator is connected with the unknown analog input voltage V_i under conversion. The comparator output is used to activate the successive approximation logic of SAR.

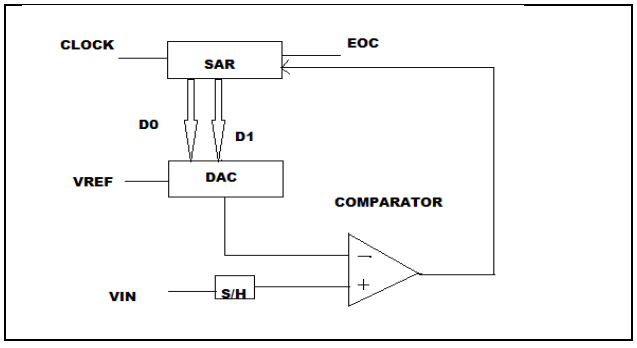

Fig.5.Successive Approximation Register

When the START command is applied, the SAR sets the MSB of the digital signal, while the other bits are made zero, so that the trial code becomes 1 followed by zeros. For example, for an 8-bit A/D converter the trial code is 10000000. The output of the SAR is converted into analog equivalent V_r and gets compared with the input voltage V_i. If V_i is greater than that of the D/A converter output , then the trial code 10000000 is less than the correct digital value. The MSB is retained as 1 and the lower significant bit is made as 1 and the testing is repeated. If the analog input V_i is now less than the D/A converter output, then the value 11000000 is greater than the exact digital equivalent. Therefore, the comparator resets the second MSB to zero and proceeds to the next most significant bit. This process is repeated for all the remaining lower bits in sequence until all the bits positions tested. The EOC signal is sent out when all the bits are scanned and the value of D/A converter output just crosses V_i.

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TABLE 1
Example Output of SAR

Correct digital representation	SAR output at different stages	Comparator output
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

V. FUTURE WORK

As SAR is the slowest ADC we have planned to implement the double tail comparator in the SAR, and analyze the delay, speed and yield range of the analog to digital converter. If the circuit enhancement is obtained then it can be used in all ADC using devices.

REFERENCES

[1]. Bernhard Wicht, *Member, IEEE*, Thomas Nirschl, and Doris Schmitt-Landsiedel, *Member, IEEE,"* Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier".
[2].Pedro M. Figueiredo, *Member, IEEE*, and João C. Vital, *Member, IEEE*,"Kickback Noise Reduction Techniques for CMOS Latched Comparators".
[3].Amin Nikoozadeh, *Student Member, IEEE*, and Boris Murmann, *Member, IEEE*,"An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch".
[4].Yusuke Okaniwa, Hirotaka Tamura, *Member, IEEE*, Masaya Kibune, Daisuke Yamazaki, Tsz-Shing Cheung, Junji Ogawa, *Member, IEEE*, Nestoras Tzartzanis, *Member, IEEE*, William W. Walker, *Member, IEEE*, and Tadahiro Kuroda, *Senior Member, IEEE,"* A 40-Gb/s CMOS Clocked Comparator With Bandwidth Modulation Technique"
[5]. Pierluigi Nuzzo, *Student Member, IEEE*, Fernando De Bernardinis, Pierangelo Terreni, and Geert Van der Plas, *Member, IEEE* ,"Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures".
[6].Jun He, Sanyi Zhan, Degang Chen, *Senior Member, IEEE*, and Randall L. Geiger, *Fellow, IEEE,"* Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators".
[7]. Jaeha Kim, *Member, IEEE*, Brian S. Leibowitz, *Member, IEEE*, Jihong Ren, *Member, IEEE*, and Chris J. Madden, *Member, IEEE,"* Simulation and Analysis of Random Decision Errorsin Clocked Comparators"
[8]. Bernhard Goll, *Member, IEEE*, and Horst Zimmermann, *Senior Member, IEEE,"* A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V".