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Design of Error Compensation for High Performance Fixed -Width Multiplier

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ABSTRACT: A modern approach to design a new error compensation circuit by using the dual group minor input correction vector to lower input correction vector compensation error. By utilizing the symmetric property of the minor input correction vector, the hardware complexity of the error compensation circuit can be lowered. By constructing the error compensation circuit mainly from the "outer" partial products, the hardware complexity only increases slightly as the multiplier input bits increase. In the proposed 16 X 16 bits fixed-width multiplier (Baugh Wooley), the truncation error can be lowered by 91% as compared with the direct-truncated multiplier and the transistor count can be reduced by 53% as compared with the full-length multiplier. As compared with the state-of-the-art design, the proposed fixed-width multiplier performs not only with lower compensation error but also with lower hardware complexity and power consumption, especially as multiplier input bits increase. The proposed error compensation circuit is designed in VHDL and implemented in XILINX FPGA

KEYWORDS: Fixed-width multiplier, Dual MIC, low-error, correction vector, input correction.

I. INTRODUCTION

The increase of portable communication and computing devices and the advance in mobile multimedia systems has made power consumption critical to optimize in the design of digital signal processing architectures Advances in VLSI technology have been a decisive factor in the growth of Digital Signal Processors (DSP), enabling the implementation of complex algorithms in portable systems. The energy challenge derived from scaling beyond sub-micron limits has modified the rules of digital design leading to new approaches to classic electronic design. The importance of energy and power efficiency in both, high performance and portable devices, and the need to reduce the energy expenditure in our current society are some of the main drivers that initiated this research.

Multipliers play a key role in the definition and design of Digital Signal Processing (DSP) systems. Not only are they a basic requirement in many algorithms, but they also shape and constrain precision, area and timing. On top of that, they are a main contributor in the overall power figures, hence the implementation of efficient parallel multipliers is desirable to achieve low-power arithmetic systems. Techniques that trade power consumption for system performance in multipliers are studied and compared in this thesis, with the main focus on the efficient implementation of DSP units by optimizing the power and accuracy performance of their multipliers. Truncated multipliers are thoroughly reviewed and com- pared to a novel proposed approach for adaptive power consumption where the power/accuracy operation point can be modified at run-time. Such a multiplier, the first approach to a column-based truncation control in the literature, is described, synthesized, simulated and tested in a custom-designed chip where the benefits of programmable truncation can be explored and are exploited in several typical arithmetic routines commonly used in signal processing units.

Fault-tolerant techniques are also studied from an energy efficiency point of view. The application of such techniques to the proposed DSP architecture shows, not only a combination of power reductions from both truncated multiplication and fault tolerance can be achieved, but the existence of synergies between both techniques to obtain further power reductions for DSP architectures.

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II. PROPOSED WORK

Baugh Wooley Algorithm

Rather than do a subtraction operation, we can obtain the two's compliment of the last two term and add all terms to get the final product the last two terms are n-1 bits each that extend in binary weight from position 2^{n-1} up to 2^{2n-3}.on the other hand, the final product is 2n bits and extends in binary weight from 2^0 up to 2^{2n-1}. We pad each of the last two terms with zeroes to obtain 2n-bit number to be able to add them to the other terms. The padded terms extend in binary weight from 2^0 up to 2^{2n-1} Assuming x is one of the last two terms we can represent it with zero padding as

$$X = -0*2^{2n-1} + 0*2^{2n-2} + 2^{n-1}\sum_{i=0}^{n-2} x_i 2^i + \sum_{j=0}^{n-2} 0*2^j \quad \text{-- (1)}$$

The above equation gives the value of X due to the fact that a negative value is associated with the MSB. When we store X in a register, the negative sign at MSB is not used since X is stored as a binary pattern. The two's compliment of x is obtained by complimenting all bits in the equations and adding '1' at the LSB.
The'1' pattern at MSB transforms into,

Bit position	2n-1	2n-2
	1	1
+	1	1
	1	0

Where overflow is ignored. Similarly, the '1' pattern at position n-1 becomes

Bit position	n	n-1
		1
+		1
	1	0

The final product P=a x b becomes

$$P = a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} + 2^{n-1}\sum_{i=0}^{n-2} \bar{b}_{n-1}\bar{a}_i 2^i + 2^{n-1}\sum_{j=0}^{n-2} \bar{a}_{n-1}\bar{b}_j 2^j + -2^{2n-1} + 2^n \quad \text{-- (2)}$$

Let us assume that a and b are 4-bit binary numbers, then the product p=a x b is 8-bits long and is given by

$$P = a_3 b_3 2^6 + \sum_{i=0}^{2}\sum_{j=0}^{2} a_i b_j 2^{i+j} + 2^3\sum_{i=0}^{2} \bar{b}_3\bar{a}_i 2^i + 2^3\sum_{j=0}^{2} \bar{a}_3\bar{b}_i 2^j + -2^7 + 2^4 \quad \text{-- (3)}$$

Error compensation Using DUAL MIC

We consider the impact of truncated products with the second most significant bits on the error compensation, but with lower hardware complexity. We propose a new error compensation circuit by using the dual group minor input correction (MIC) vector to further lower IC vector compensation error. By utilizing the symmetric property of MIC, fan-in can be reduced to half and hardware in up-MIC and down-MIC can be shared. Therefore, the hardware complexity of error compensation circuit can be lowered. Moreover, the hardware complexity just increases slightly as the multiplier input bits increase because we construct the proposed error compensation circuit mainly by the "outer" partial products. As compared with previous design, the proposed fixed-width multiplier not only performs with lower compensation error but also with lower hardware complexity, especially as multiplier input bits increase.

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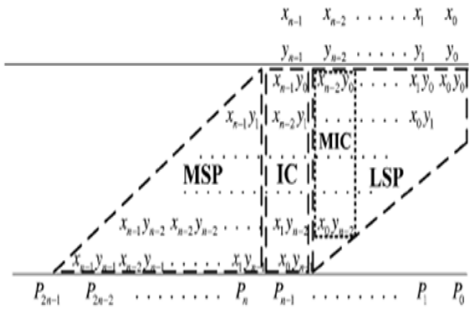

Fig.1. Block Diagram of DUAL MIC

Baugh-Wooley array multiplier with two unsigned n-bit inputs of X and Y, which are shown as

$$X = \sum_{i=0}^{n-1} x_i.2^i, \quad Y = \sum_{j=0}^{n-1} y_j.2^j. \text{-- (4)}$$

The multiplication result P is the summation of partial products of x_i and y_j, which is shown as

$$P = \sum_{k=0}^{2n-1} pk\ .2^k = \sum_{j=0}^{n-1}\sum_{i=0}^{n-1} x_i y_j .2^{i+j}. \text{-- (5)}$$

The full-length n-bit unsigned Baugh-Wooley partial product array can be divided into three subsets of most significant part (MSP), IC vector and less significant part (LSP) as shown in Fig.1. To evaluate the accuracy of a fixed-width multiplier, we can exploit the difference between the n-bit fixed-width multiplier output and the 2n-bit full-length multiplier output, which is expressed as

$$\varepsilon = P - P_L \qquad \text{-- (6)}$$

Where P is the output of the complete multiplier, and Pt is the output of the fixed-width multiplier. P_t can be expressed

$$P_i = \sum_{j=1}^{n-1} y_j.2^j \sum_{i=n-j}^{n-1} x_i 2^i + f(x_0 y_{n-1}, x_1 y_{n-2}, ..., x_{n-2} y_1, x_{n-1} y_0) \text{-- (7)}$$

$$= \sum_{j=1}^{n-1} y_j 2^j \sum_{i=n-j}^{n-1} x_i 2^i + f(IC). \text{-- (8)}$$

Where f(IC) is the error compensation function. The error compensation function f(IC) is approximated as the sum of input correction vector with corresponding weight. To realize f(IC), the error compensation vector is divided into two disjoined sets and uses two addition trees to compute the error compensation. The error compensation algorithm is developed as

$$f(IC) = \begin{cases} 0, if\ \beta = 0 \\ \beta, if\ (x_{n-1}y_0 + x_{n-2}y_1 + x_1 y_{n-2} + x_0 y_{n-1} = 0,1) \\ \beta - 1, if\ ((x_{n-1}y_0 + x_{n-2}y_1 + x_1 y_{n-2} + x_0 y_{n-1} = 2,3) \\ \beta - 2, if\ ((x_{n-1}y_0 + x_{n-2}y_1 + x_1 y_{n-2} + x_0 y_{n-1} = 4) \end{cases} \text{--(9)}$$

Where β is the summation of all partial product terms in the input correction vector.

The first addition tree, which is devoted to lower weight partial products, is a standard one-counter constructed by using full adders and half adders. The lower weight partial products of IC include the most external four partial products, which are x_5y_0, x_4y_1, x_1y_4, and x_0y_5 in the 6-bit multiplier, having a weight of 2^n in error compensation.

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As for the second addition tree, it utilizes modified half-adders (mHAs) to take into account the contribution of partial products with higher weights. The higher weight partial products of IC include the other internal partial products, which are x_3y_2 and x_2y_3 in the 6-bit multiplier, having a weight of 2^{n-1} in error compensation. The difference between mHA and standard HA is that when inputs of A and B are both 1, sum=1 and Cout=1 in mHA instead of Sum=0 and Cout=1 in standard HA.

Proposed Error Compensation Method

The compensation errors can be divided into two categories: the first type is caused by insufficient error compensation, in which output P_t is smaller than ideal value P. In this case, $\varepsilon = P-P_t > 0$.On the other hand, the second type is due to over error compensation, in which output is larger than ideal value. In this case $\varepsilon = P-P_t < 0$. To consider both approximation error and circuit complexity, we mainly aim at dealing with the case of $|\varepsilon|>2^{n-1}$in this paper. The weight of IC compensation circuit is 2^n. We cannot correct all the cases of $|\varepsilon|>2^{n-1}$ effectively if we only apply the partial product terms in IC to construct the error compensation function. Therefore, in this paper we adopt IC together with MIC, where MIC is the partial product vector with the most significant bits of LSP, to amend the error compensation value of f(IC). In this way, the cases of $\varepsilon = P-P_t > 0$ can be reduced effectively.

IC compensation circuit is constructed by dual IC compensation trees, which are the "inner" partial products with higher compensation weight and the "outer" partial products with lower compensation weight. According to the relation of IC and Savg (IC) in Table I, we can find out that the average compensation errors in the outer part and inner part are nearly the same, where the average compensation error is 0.0285 in the outer part and it is 0.0300 in the inner part. Here Savg (IC) is the average value of sum of the IC and LSP partial products. However, the number of partial product items with higher weight will increase with the number of bits, while the number of partial product items with lower weight is fixed. Therefore, we only analyze the error compensation tree with lower weight to find out the cases of $|\varepsilon|>2^{n-1}$. Then we combine IC with MIC to adjust the function of f(IC) to make the compensation error lower than 2^{n-1}.

In this way, the error compensation circuit can be relatively simple and the compensation error can be lowered more efficiently. To find out a precise error correction vector, we analyze the sum of total errors in the cases of $|\varepsilon|>2^{n-1}$and $|\varepsilon|<2^{n-1}$in under various β. In order to achieve an efficient error correction, we only amend the error compensation function f(IC) under the cases that the total error summation value of $|\varepsilon|>2^{n-1}$ is larger than that of $|\varepsilon|<2^{n-1}$. The analysis results are listed in Table II. By comparing the error summation value of $|\varepsilon|>2^{n-1}$ with that of $|\varepsilon|<2^{n-1}$in Table II, it can be observed that some under-compensated errors occur when β=2 and β=4. As a result, we combine IC with MIC to correct the under-compensated situations under the cases of β=2 and β=4. As for the case of β=1, there exists some over compensation errors. However, the total error summation value of $|\varepsilon|>2^{n-1}$ is about the same with that of $|\varepsilon|<2^{n-1}$.

We combine IC with MIC to correct the over compensation situations under the case of β=1 and $S_{ICh} \neq 0$ instead of the case of β=1 only since in such case the error summation value of $|\varepsilon|<2^{n-1}$ is much lower. Here S_{ICh} is the summation of IC that with higher weight, which can be written as

$$S_{ICh} = x_n - 3y_2 + x_n - 4y_3 + ... + x_3y_{n-4} + x_2y_{n-3}. \text{-- (10)}$$

The lower unit with the second most significant bits of truncated partial products is adopted as minor input correction (MIC) vector to reduce the compensation error, which is defined as TABLE I

TABLE I

SYMMETRIC RELATION BETWEEN IC AND SAVG (IC),

Row	IC	S_{avg} (IC)
1	(1,0,0,0,0,0,0,0)	0.944
2	(0,1,0,0,0,0,0,0)	0.999
3	(0,0,1,0,0,0,0,0)	1.025
4	(0,0,0,1,0,0,0,0)	1.035
5	(0,0,0,0,1,0,0,0)	1.035
6	(0,0,0,0,0,1,0,0)	1.025
7	(0,0,0,0,0,0,1,0)	0.999
8	(0,0,0,0,0,0,0,1)	0.944

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TABLE II
ANALYSIS FOR THE SUM OF TOTAL ERRORS IN THE CASES OF $|\varepsilon|>2^{n-1}$ AND $|\varepsilon|<2^{n-1}$ UNDER VARIOUS β VALUES IN ACCORDANCE WITH THECOMPENSATION ALGORITHM

Under-Compensated Case(The Summation Value of total error is positive)		
	e>32	0<e<32
β =0	7002	8662
β =1	366	3496
β =2	17042	8065
β =3	1268	1680
β =4	1040	0
Under-Compensated Case(The Summation Value of total error is negative)		
β =0	-1056	-4081
β =1	-14370	-14550
β =2	0	-337
β =3	0	-388
β =4	0	0
β =1 and $S_{ICH}\neq 0$	-14370	-6661

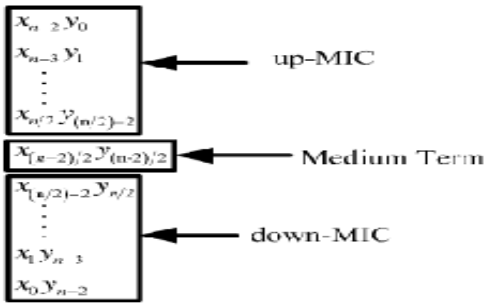

Fig. 2.MIC is divided into up-MIC, medium term and down-MIC

$$MIC = (x_{n-2}y_0, x_{n-3}y_1, ..., x_1y_{n-3}, x_0y_{n-2}). \text{-- (11)}$$

Proposed Error Compensation Design Circuit

The error compensation circuit we proposed is modified from the dual-tree design. To further reduce the compensation errors, we combine IC with MIC to correct the f(IC) under under-compensatedand over-compensated cases. The proposed design is illustrated in Fig. 2. The compensation function from C_1 to C_{n-2} is the same as fixed-width multiplier. To reduce hardware complexity, the HA through $C_3$to C_{n-2} is removed. In the under compensation cases of β =2,4and over compensation case of β=1, we modify the compensation function in C_{n-1} and C_n. The Boolean function of C_{n-1} and C_n is expressed as

$$C_{n-1} = [(S_1C_1)(OR_{ICh})(NOR_{MIC})(C_1 + C_2)']'$$
$$C_n = (S_1C_1)'(OR_{up-MIC})(OR_{down-MIC})(C_1 + C_2). \text{-- (12)}$$

Here $S_{IC1}$is the summation of IC that with lower weight, OR_{ICH} is the OR result of all IC terms that with higher weight, NOR_{ICH} is the NOR result of all MIC terms, and $OR_{UP\text{-}MIC}$/ $OR_{DOWN\text{-}MIC}$ are the OR result of all up-MIC/down-MIC terms, respectively.

In order to further reduce the circuit complexity, we apply De-Morgan's law to simplify the proposed error compensation circuit in C_{n-1} and C_n. After simplifying through DeMorgan's law and hardware sharing, the transistor

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count in our proposed error compensation circuit can be reduced from 62 to 40. Finally, the Dual MIC fixed-width multiplier with error compensation circuit is illustrated in Fig. 2.

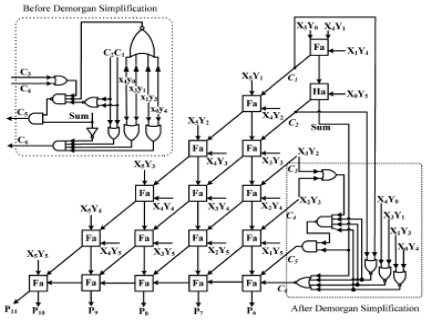

Fig.3.Dual MIC error compensation Circuit

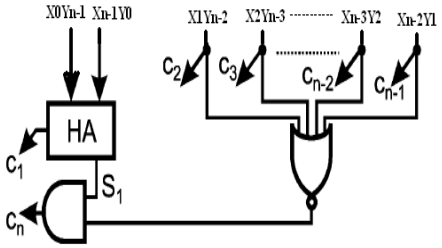

Fig.4.Proposed error Compensation Circuit

Performance Comparisons

In this section, we compare the proposed fixed-width multiplier with other literature designs to analyze their approximation error and hardware complexity, respectively. All performance comparisons are evaluated from 8-, 12-, to 16-bit. To analyze the compensation error, we inject all possible input patterns into the fixed-width multiplier. Then we compare the truncated output with their corresponding full-length multiplier output. By exploiting the difference between the n-bit fixed-width multiplier output and the 2n bit full-length multiplier output, we can obtain each error term. For truncation error comparison, we define the index of mean square error ε_{ms} as

$$\varepsilon_{ms,\%} = \frac{\varepsilon_{ms}}{\varepsilon_{ms}(Truncated)} X100\% \qquad \text{-- (13)}$$

The smaller value of ε_{ms} represents the more precise error correction. The precision analysis results of various fixed-width multipliers are illustrated in Table III. In the previous literature designs, can perform the lower mean square errors because multiple-input error compensation vector designs are adopted in error correction. Especially in [8]–[10], they further take different weights of input correction partial products into account; as a result, the mean square errors can be lowered to 2.37% and 2.35% in the 16-bit fixed-width multiplier, respectively. In [6], the 2-D conditional estimation method can be more precise; however, their design is too complex. Similarly, a variable correction to include the more partial products columns of LSB part is proposed in [10] to enhance error compensation precision; however, the hardware complexity will increase accordingly. In our proposed design, we adopt the dual-group MIC vector to further lower the compensation errors in [8] with lower hardware complexity. Most cases of $|\varepsilon|>2^{n-1}$ in [8] can be removed; as a result, the mean square error is further lowered to 2.30% in the proposed 16-bit fixed-width multiplier. The comparison index of R% is defined as the transistor count of fixed-width multiplier divided by the transistor count of full-length multiplier, which can be defined as

$$R\% = \frac{N_{Truncated}}{N_{standard}} X100\% \qquad \text{-- (14)}$$

As illustrated in Table IV, the transistor count in the proposed design are more in the fixed-width multiplier with small width _ as compared with other literature designs [4], [7]–[10]. However, in the fixed-width multiplier with large width _, the transistor count in the proposed design are less as compared with literature designs in [4], [7]–[10]. To consolidate the comparison results in Tables III and IV, we compare the compensation error and transistor count together in Fig. 6. As illustrated in Fig. 6, the proposed design performs the lowest mean square error; moreover, its transistor count can be lower than the design in [7]–[10] in the 16-bit fixed-width multiplier. In general, to achieve lower compensation error needs more complex compensation algorithm and more complicated circuit hardware. In this paper, we combine IC with MIC to adjust the function of f(IC) to lower the compensation error. We also analyze the error compensation tree only with lower weight to find out the cases of $\boldsymbol{\varepsilon|>2^{n-1}}$ in our proposed design. Therefore, circuit complexity in the most error compensation circuit is fixed, which will not increase along with input bit number.

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As a result, the error compensation circuit can be relatively simple, especially as the input bit number increases. As illustrated in Fig. 7, the slope of transistor count increasing as the fixed-width multiplier input number increases is gentler in our proposed design. Though in our proposed design we must spend more transistor count in the 8-bit fixed-width multiplier, we spend less transistor count in the cases of input bit number are larger than eight. The superiority in area-efficiency in our design is more obvious as input number increases. Finally, we implement the proposed 16-bit low-error, area-efficient fixed-width multiplier in TSMC 0.18-µm process as illustrated in Fig. 8. The silicon chip area of the proposed fixed-width multiplier circuit is 109.8 µm by 106.8 µm. As compared with [8], the critical paths in both our design and [8] are located in the path of propagation. In both designs the circuit delay are nearly the same under various timing constraints, which all are faster than the conventional ripple designs. The circuit layout area and power consumption in the proposed design is slightly lower than that of [8] since lower transistor count and less wire connection in the error compensation circuit even though our design is more irregular.

TABLE III
COMPARISON OF MEAN SQUARE ERROR (ε_{ms}%) UNDER VARIOUS FIXED-WIDTH MULTIPLIER DESIGNS

Multiplier	N=8	N=12	N=16
D.Truncated Structure	100% (4.018)	100% (9.098)	100% (16.18)
J.M.Jou	14.89%	8.58%	5.59%
S.J.Jou	6.56%	3.82%	2.66%
F.Curticapean	5.82%	3.66%	2.62%
A.G.M.Strollo(Type-I)	5.86%	3.85%	2.78%
A.G.M.Strollo(Type-II)	5.38%	3.30%	2.37%
S.R.Kuang	5.31%	3.26%	2.35%
Y.C.Loao	5.01%	3.14%	2.27%
I-Chyn Wey and Chun-Chien Wang	4.46%	3.04%	2.30%
Proposed New Design	4.06%	2.86%	2.03%

TABLE IV
COMPARISON OF TRANSISTOR COUNT UNDER VARIOUS FIXED-WIDTH MULTIPLIER DESIGNS

Multiplier	N=8	N=12	N=16
D.Truncated Structure	100% (2184)	100% (5280)	100% (9720)
J.M.Jou	53.85%	52.50%	51.85%
S.J.Jou	57.42%	54.89%	53.64%
F.Curticapean	53.85%	52.50%	51.85%
A.G.M.Strollo(Type-I)	57.42%	54.89%	53.64%
A.G.M.Strollo(Type-II)	57.51%	54.92%	53.66%
S.R.Kuang	57.42%	54.89%	53.64%
Y.C.Luao	56.85%	54.49%	53.34%
I-Chyn Wey and Chun-Chien Wang	57.97%	54.51%	53.11%
Proposed New Design	52.79%	49.34%	47.94%

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III. SOFTWARE REQUIREMENT

MODELSIM 6.3f

ModelSim is an easy-to-use yet versatile VHDL/ (System) Verilog/SystemC simulator by Mentor Graphics. It supports behavioral, register transfer level, and gate-level modeling. ModelSim supports all platforms used here at the Institute of Digital and Computer Systems (`i.e.` Linux, Solaris and Windows) and many others too. On Linux and Solaris platforms ModelSim can be found preinstalled on Institute's computers. Windows users, however, must install it by themself. It introduces you with the basic flow how to set up ModelSim simulator, compile your designs and the simulation basics with ModelSim SE. The example used in this tutorial is a small design written in VHDL and only the most basic commands will be covered in this tutorial. This tutorial was made by using version 6.3f of ModelSim SE on Linux.

IV. CONCLUSION

In conclusion, a low-error and efficient area fixed-width multiplier by using the dual group minor input correction vector is presented. As compared with the previous error compensation circuit, the proposed fixed-width multiplier performs not only with lower compensation error but also with lower hardware complexity, especially as multiplier input bits increase. The proposed 16-bit fixed-width multiplier circuit is implemented in TSMC 0.18-µm process and the silicon area is 11726.64 μm^2. The mean square error in the proposed design is lowered to 2.30%. The transistor counts in the proposed design are only 53% of the full-length multiplier. The power consumption is lowered to 7.2%.

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