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Design of Low Power Combinational Circuits Using Reversible Logic and Realization in Quantum Cellular Automata

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Abstract— In modern VLSI systems, power dissipation is very high due to rapid switching of internal signals. Landauer showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits. Information is lost when the input vectors cannot be recovered from circuit's output vectors. To overcome the above drawback reversible logic is introduced where the number of output vectors are equal to the number of input vectors. In this paper the basic reversible gates are realized using the tanner tool. The Half adder using CMOS logic is compared with the reversible logic and the corresponding power are measured using T-Spice.

Keywords— Reversible Logic, Basic Reversible Gates, Power measurement

The paper is organized as follows: the section one gives the overall introduction about the reversible logic. Section two gives information about the basic reversible logic gates. In the section three simulation of the half adder using CMOS logic and by using reversible logic is done using S-Edit. At last the power measured using CMOS logic is compared with the reversible logic and the corresponding results are elaborated.

I. INTRODUCTION

1.1 IRREVERSIBLE LOGIC:

A gate is considered to be irreversible if the input and output vectors are not uniquely retrievable. Due to this there will be a rapid internal power dissipation. It was proved by Landauer [1] that the computer must dissipate at least KTln2 of energy for each bit of information it writes or erases. An example of an irreversible gate is show in Fig. 1.

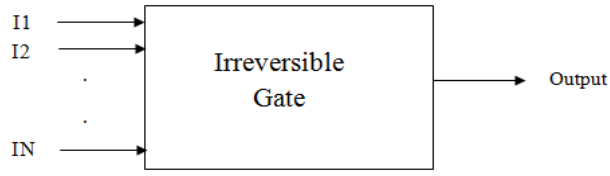

Fig. 1 Irreversible Gate

The input to the irreversible gate are I1,I2 …. IN. The output of the gate is output. Since the number of input vectors cannot be recovered from output vector the information will be lost.

1.2 REVERSIBLE LOGIC:

In order to overcome the above drawback said by Landauer, Bennet [2] proposed a logic called Reversible logic where the input and output vectors are uniquely retrievable. Reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is one to one correspondence between the input and the output vectors.

An example of the reversible gate is shown in the Fig. 2.

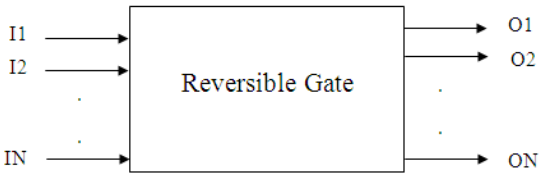

Fig. 2 Reversible Gate

The reversible logic solution may be especially important in low-voltage designs of mobile systems, where both power saving and overheating are very important due to the need for light weight and independent power supply. One of the application of the reversible logic is quantum cellular automata.

1.3 GARBAGE OUTPUT:

To obtain a bijective function i.e. one to one mapping a garbage output is introduced. The output of the particular gate which is not further going to be used in the proceeding gates are referred to as garbage output. An example of the garbage output is shown in the Fig. 3.

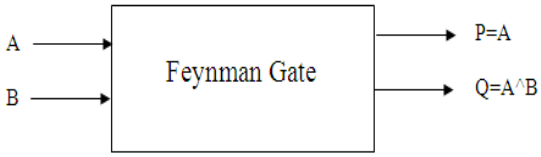

Fig. 3 Garbage output

In the above example the output P=A refers to the garbage output. These outputs are needed to maintain the reversiblity.

II. BASIC REVERSIBLE GATES:

2.1. FEYNMAN GATE:

The Fig. 4 shows the reversible implementation of reversible XOR gate using Feynman gate [8].

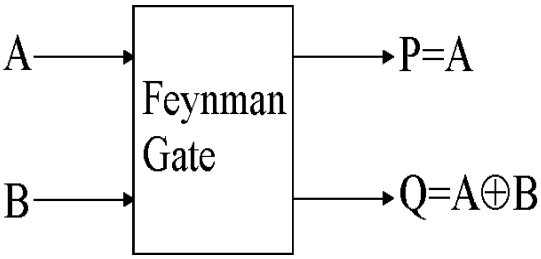

Fig. 4. Feynman Gate

In Feynman gate, one of the input bits act as control signal (A). That is, if A= 0 then the output Q follows the input B. If A = 1 then the input B is flipped at the output Q. So it is called as controlled NOT (C-NOT). This gate is one-through gate which means that one input variable is also output. Feynman gate acts as copying gate when the second input is zero by duplicating the first input at the output.

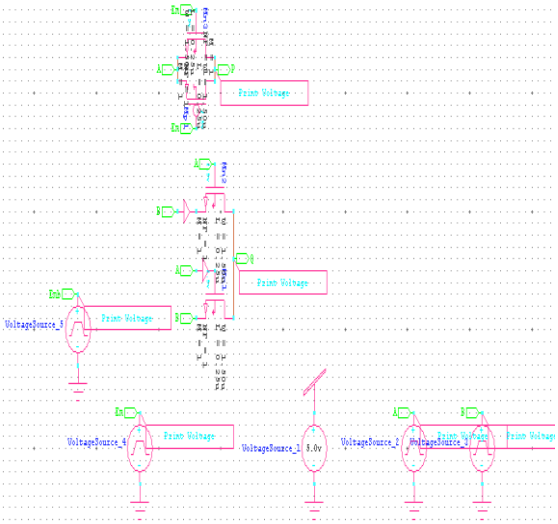

Figure 5 Schematic of Feynman gate

The above figure represents the schematic of the Feyman gate and the corresponding simulation results obtained are shown in the Fig. 6

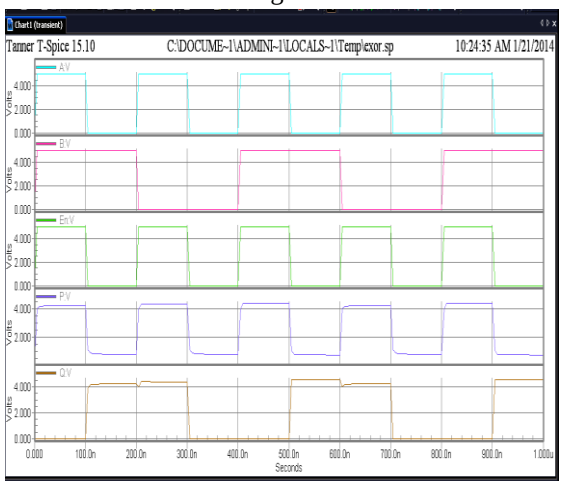

Fig. 6 Simulation Result of Feynman gate

2.2 FREDKIN GATE:

The Fredkin gate [7] swaps the last two bits, if the first bit is set. It works as a controlled swap. It is a 1-through gate, i.e one input is directly generated as output, and two other outputs can generate two different Boolean functions.

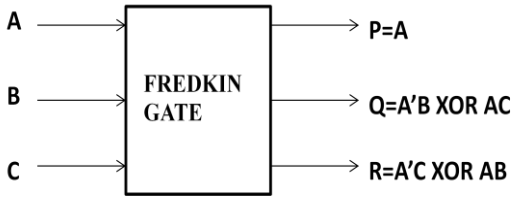

Fig. 7 Fredkin Gate

Fredkin gate (FRG), also known as controlled Permutation gate. The Fig. 7 shows the Fredkin gate.

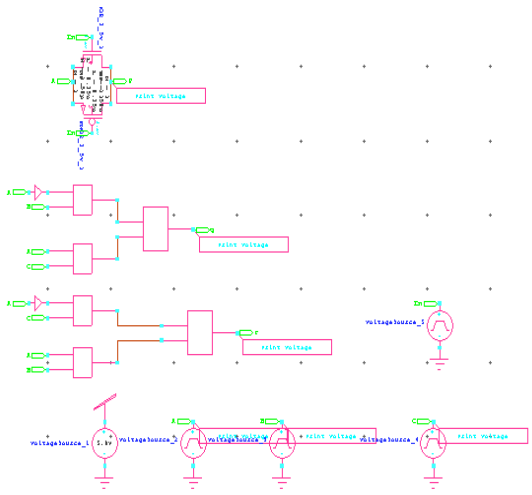

Fig. 8 Schematic of Fredkin gate

The above figure represents the schematic of the Fredkin gate and the corresponding simulation results obtained are shown in the Fig. 9

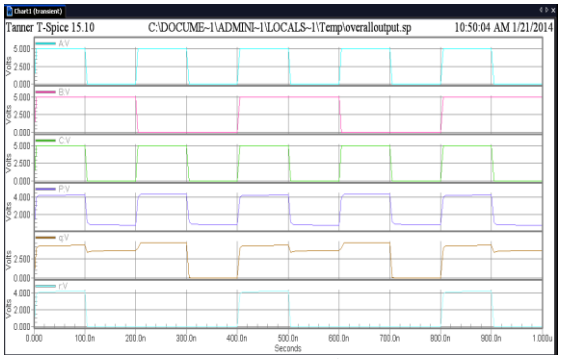

Fig. 9 Simulation Result of Fredkin gate

2.3 PERES GATE:

The only cheapest quantum realization of a complete (universal) 3*3 reversible gate is Peres gate [10] and its cost is 4.

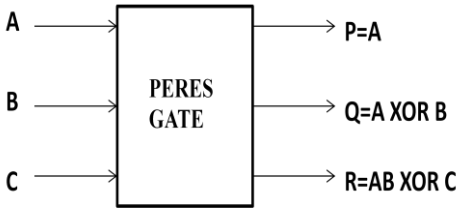

Fig. 10 Peres Gate

Peres gate (PG) is also known as New Toffoli Gate (NTG), combining Toffoli Gate and Feynman Gate.

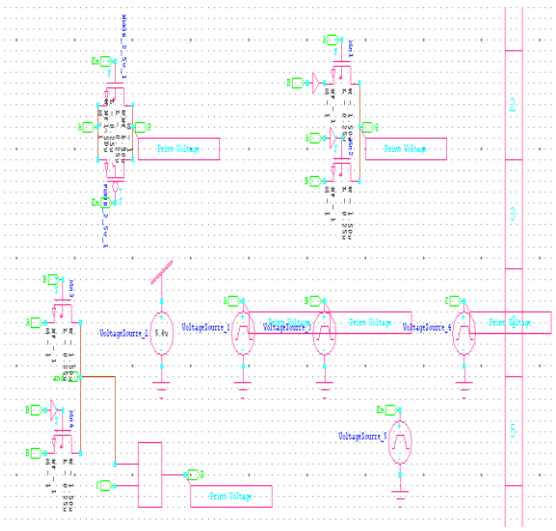

Fig. 11 Schematic of Peres gate

The above figure represents the schematic of the Peres gate and the corresponding simulation results obtained are shown in the Fig. 12.

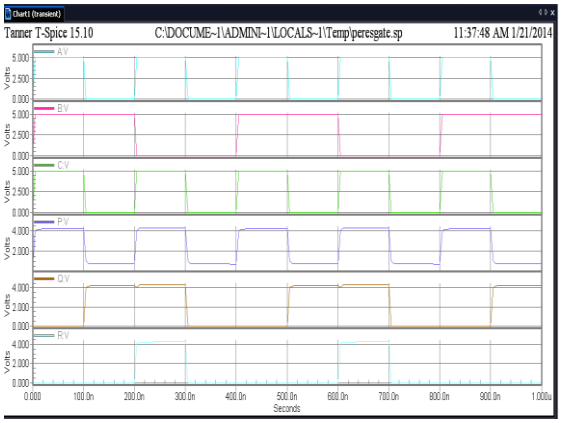

Fig. 12 Simulation Result of Peres gate

2.4 NEW GATE:

The New gate [7] is a 3-input 3-output reversible gate as shown in the Fig. 13.

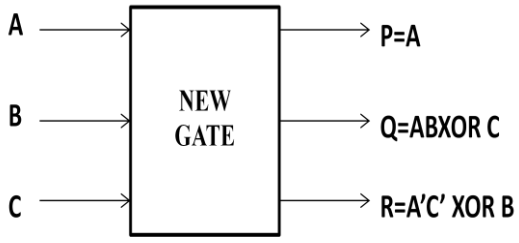

Fig. 13 New gate

It is used to realize the NAND, NOR, and OR gates.

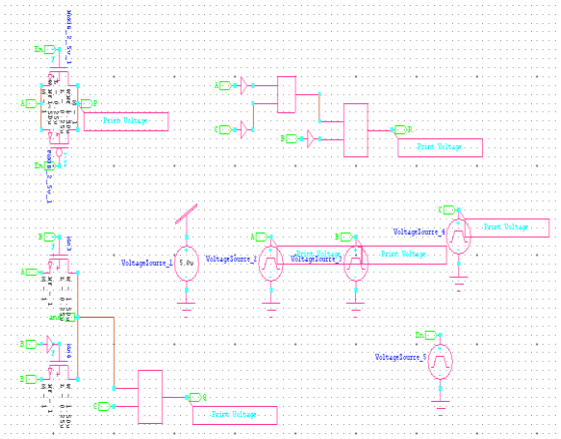

Fig. 14 Schematic of New gate

The above figure represents the schematic of the New gate and the corresponding simulation results obtained are shown in the Fig. 15.

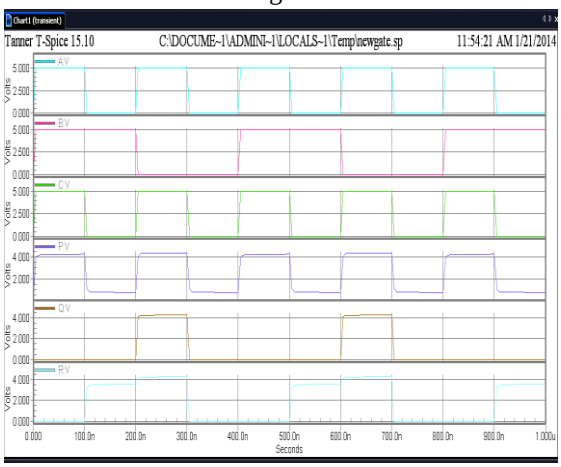

Fig. 15 Simulation Result of New gate

2.5 HNG GATE:

The HNG gate is a 4*4 reversible gate. It can be used as a full adder. As shown in the Fig. 16, the first and second outputs are through outputs.

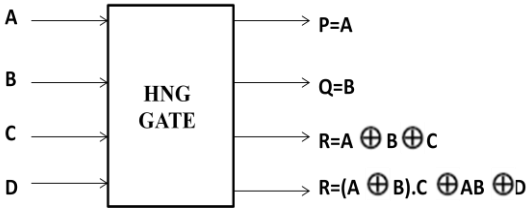

Fig. 16 HNG gate

The third and fourth outputs give the sum and carry of the full adder respectively. It is used in the multiplier design to add the partial products.

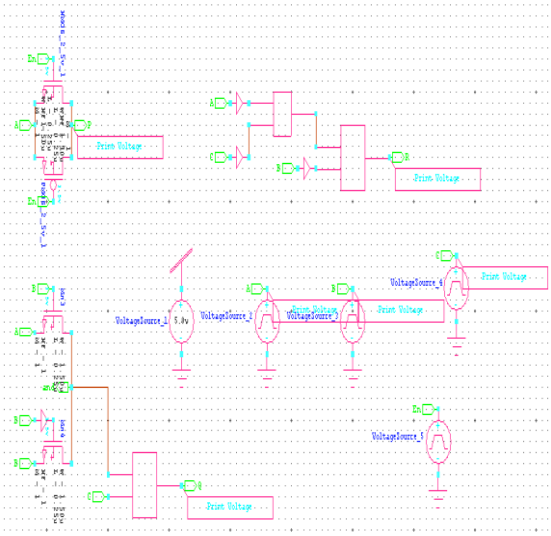

Fig. 17 Schematic of HNG gate

The above figure represents the schematic of the HNG gate and the corresponding simulation results obtained are shown in the Fig. 18.

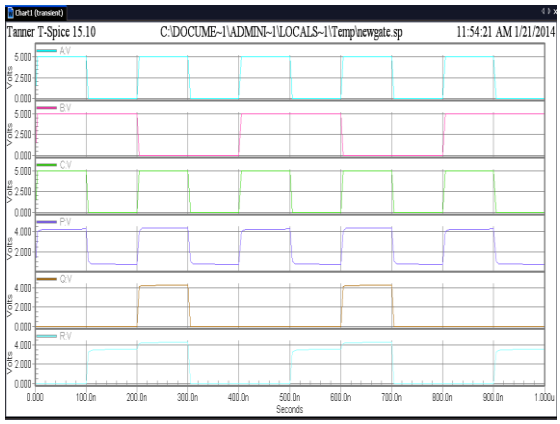

Fig. 18 Simulation Result of HNG gate

III. HALF ADDER:

A. HALF ADDER:

The Half adder is a combinational circuit that performs addition of two bits. It is designed conventionally by EXOR and AND gates. When two inputs A and B are added, the Sum and Carry outputs are produced according to the truth table.

The logic function for half-Adder is given below:

Sum = A'B+AB' (1)

Carry = AB (2)

The corresponding circuit diagram for half adder is shown in the Fig. 19

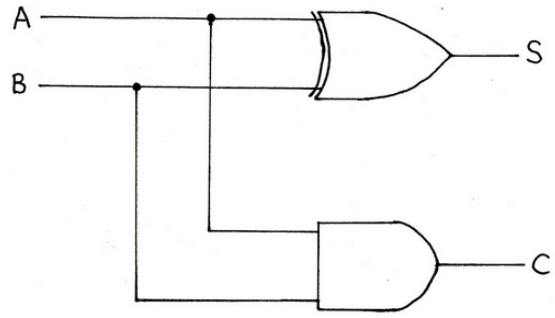

Fig. 19 Half Adder

By applying the CMOS logic for Equation (1) and (2) the schematic and simulation result obtained are shown in the Fig. 20 and 21 respectively.

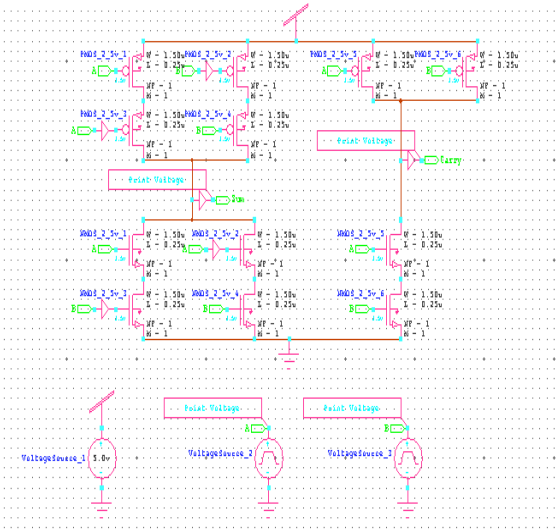

Fig. 20 Schematic of Half Adder using CMOS

The above figure represents the schematic of the Half adder and the corresponding simulation results obtained are shown in the Fig. 21.

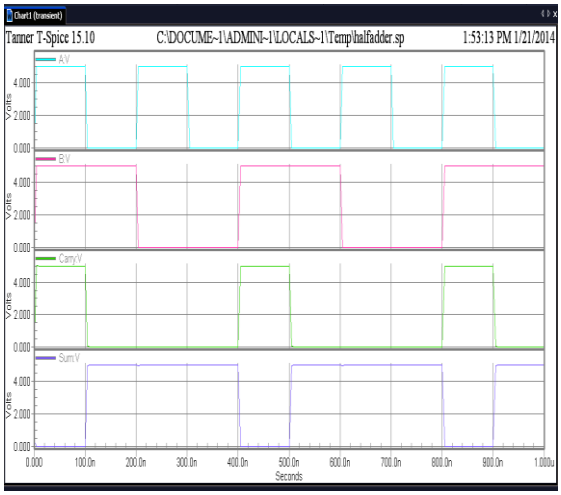

Fig. 21 Simulation Result of Half Adder using CMOS

The Half adder in terms of Reversible Logic is given by

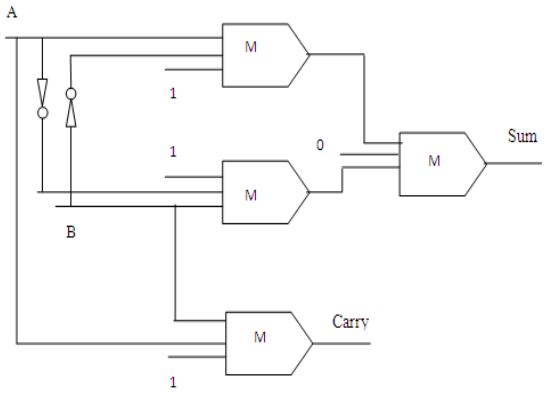

Fig. 22 Half Adder using Reversible Logic

The symbol M in the first stage represents the three input AND gate and the symbol M in the second stage represents the three input OR gate. The schematic of the Half adder using Reversible logic is shown in the Fig. 23.

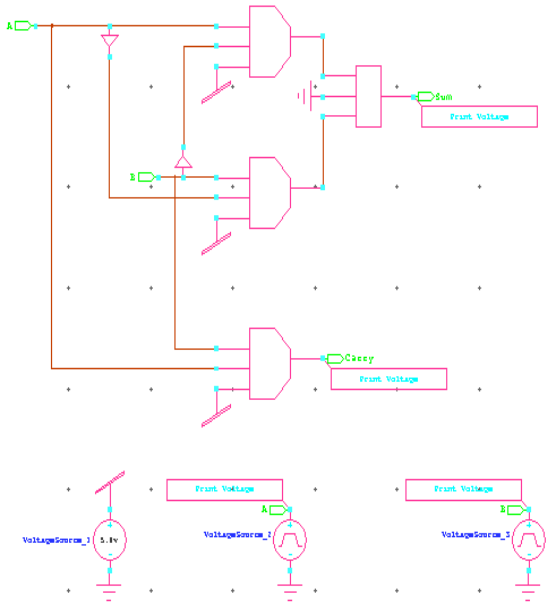

Fig. 23 Schematic of Half Adder using Reversible Logic

The corresponding simulation result obtained is shown in the Fig. 24.

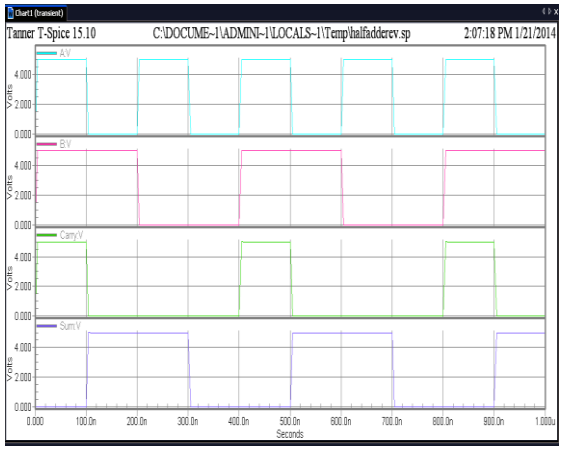

Fig. 24 Simulation Result of Half Adder using Reversible logic

IV. FULL ADDER:

An alternative approach for the addition of two *n*-bit numbers is to use a separate circuit for each corresponding pair of bits. Such a circuit would accept the 2 bits to be added, together with the carry resulting from adding the less significant bits. It would yield as outputs the 1-bit sum and the 1-bit carry out to the more significant bit. Such a circuit is called a *full adder*. The 2 bits to be added are *xi* and *yi* , and the *carry in* is C_i. The outputs are the *sum Si* and the *carry out* C_{i+1}.

When it is simulated by using the tanner tool the corresponding schematic and layout is shown in Fig.25.

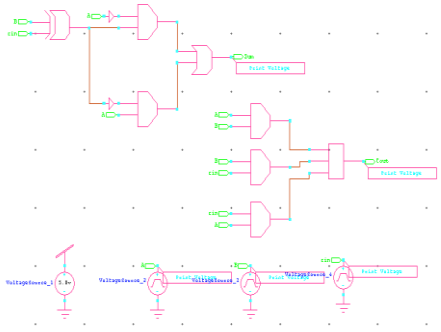

Fig. 25. Schematic of Full Adder using CMOS

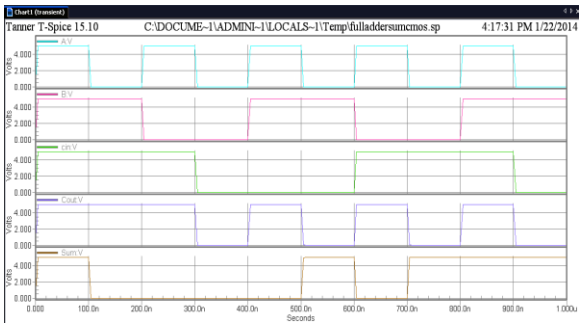

Fig. 26 Simulation Result of Full Adder using CMOS

Fig. 25 and Fig. 26 represents the full adder using the CMOS logic. When the same full adder is simulated using the reversible logic the results obtained are shown in the Fig. 27 and Fig. 28.

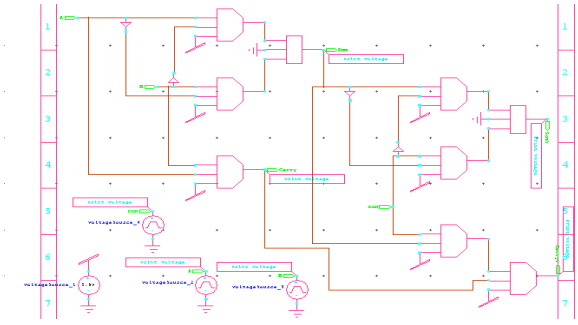

Fig. 27 Schematic of Full Adder using Reversible Logic

The corresponding simulation result obtained is shown in the Fig. 27

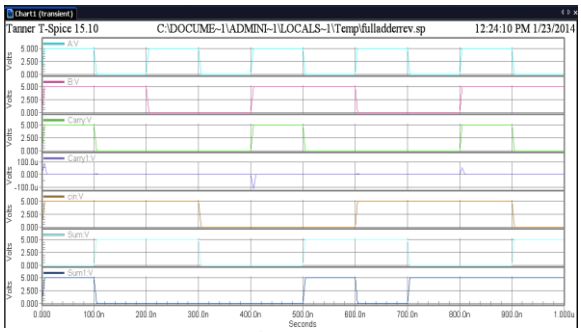

Fig. 28 Simulation Result of Full Adder using Reversible logic

V. CARRY SHIFT MULTIPLICATION (CSM):

Let (Ai,Bi) be the multiplicand and multiplier pair and pi be the product sum of the bit position i. The implementation can be done in two ways. Equations (4) and (5) represent the two alternatives.

$$(S_{ij}, C_{ij}) = \text{Add}\,(b_j\, z^{-7/4j}\, a_i,\ z^{-3/4}\, S_{i(j-1)},\ z^{-1/4} c_{i(j+1)})$$

$$= \text{Add}\,(b_j\, a_{i-7/4j},\ S_{(i-3/4)\,(j-1)},\ c_{(i-1/4)\,(j+1)}) \qquad (3)$$

$$(S_{ij}, C_{ij}) = \text{Add}\,(b_j\, z^{-3/2j}\, a_i,\ z^{-1/2}\, S_{i(j-1)},\ z^{-1} c_{ij})$$

$$= \text{Add}\,(b_j\, a_{i-3/2j},\ S_{(i-1/2)\,(j-1)},\ c_{(i-1)\,(j)}) \qquad (4)$$

Equation (3) sends the carry-out in a backward direction with minimum delay. Instead, Equation (4) uses a feedback loop to the adder itself using a one clock delay unit. Both handle the carry-out correctly carrying it to the higher bit calculation. Call them a carry shift multiplication (CSM) and a carry delay multiplication (CDM), respectively.

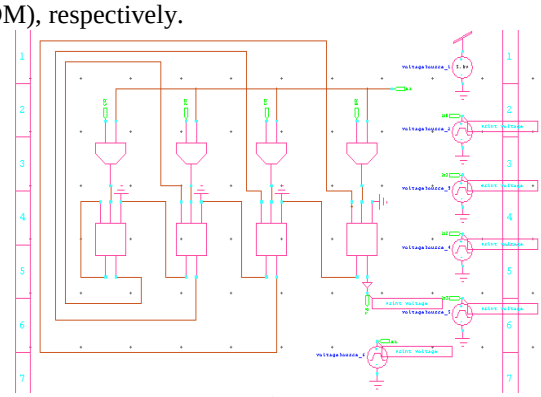

Fig. 29 Schematic of CSM using CMOS

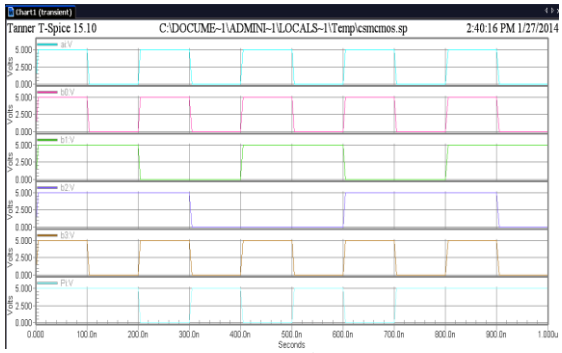

Fig. 30 Simulation Result of CSM using CMOS

Fig. 28 and Fig. 29 represents the CSM using the CMOS logic. When the same full adder is simulated using the reversible logic the results obtained are shown in the Fig. 30 and Fig. 31.

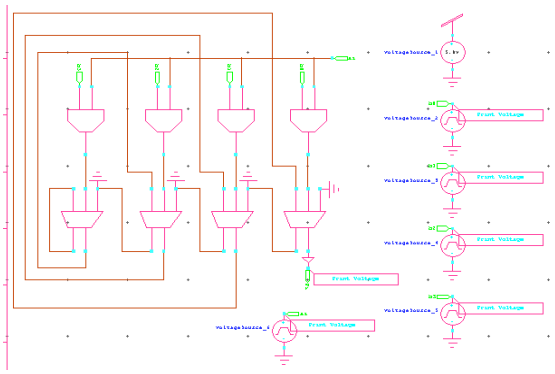

Fig. 31 Schematic of CSM using Reversible Logic

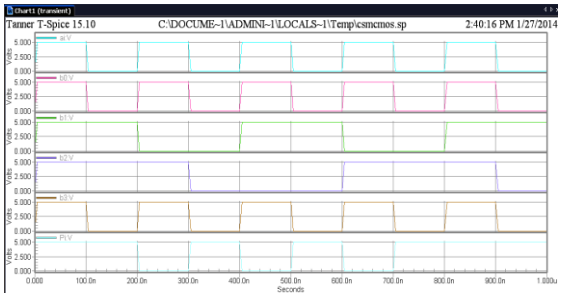

Fig. 32 Simulation result of CSM using Reversible Logic

VI. Power Measurement:

The power is measured by using T-Spice. When compared with the results obtained in figure 21 and 24, 26 and 29, 30 and 32 power savings obtained in combinational circuits using Reversible logic is more when compared with the half adder using CMOS. The Table 1 represents the results obtained using CMOS and Reversible Logic.

Table I: Comparisons of power using the CMOS and Reversible Logic

The Table I represents the comparisons of power results obtained for Half adder using CMOS and Reversible Logic

Table I Comparisons of Power Results for Half Adder using CMOS and Reversible Logic

Voltage Source	**Average Power in watts using Reversible Logic**	**Average Power in watts using CMOS**	**% of Power savings**
VVoltageSource_1	1.963090e^{-004}	2.360161e^{-004}	16.94%
VVoltageSource_2	4.954632e^{-007}	6.175865e^{-007}	19.77%
VVoltageSource_3	4.358825e^{-007}	6.203697e^{-007}	29.83%

The Table II represents the comparisons of power results obtained for Full adder using CMOS and Reversible Logic

Table II Comparisons of Power Results for Full Adder using CMOS and Reversible Logic

Voltage Source	**Average Power in watts using Reversible Logic**	**Average Power in watts using CMOS**	**% of Power savings**
VVoltageSource_1	2.754098e-^{004}	4.364584e-^{004}	36.92%
VVoltageSource_2	5.013920e-^{007}	5.853922e-^{007}	14.35%
VVoltageSource_3	4.789355e-^{007}	6.578020e-^{007}	27.24%
VVoltageSource_4	1.767430e-^{007}	2.838557e-^{007}	37.80%

The Table III represents the comparisons of power results obtained for CSM using CMOS and Reversible Logic

Table III Comparisons of Power Results for CSM using CMOS and Reversible Logic

Voltage Source	**Average Power in watts using Reversible Logic**	**Average Power in watts using CMOS**	**% of Power savings**
VVoltageSource_1	1.170291e-^{002}	4.836119e-^{003}	75.77%
VVoltageSource_2	1.314035e-^{007}	8.100696e-^{009}	83.82%
VVoltageSource_3	1.115675e-^{007}	8.756538e-^{008}	87.31%
VVoltageSource_4	4.448981e-^{008}	5.336381e-^{009}	16.69%
VVoltageSource_5	1.314094e-^{007}	8.108605e-^{009}	83.82%
VVoltageSource_6	2.444666e-^{008}	5.049112e-^{007}	51.58%

VII. Results And Discussion:

The below table represents the average power consumed for CMOS and reversible logic.

Table III Comparisons of Power Results for Combinational Circuits using CMOS and Reversible Logic

Combinational Circuits	**Average Power in watts using Reversible Logic**	**Average Power in watts using CMOS**	**% of Power savings**
Half Adder	$1.963090e^{-004}$	$2.360161e^{-004}$	16.94%
Full Adder	$2.754098e^{004}$	$4.364584e^{-004}$	36.92%
CSM	$1.170291e^{-002}$	$4.836119e^{-003}$	75.77%

It is clear that the average power using Reversible logic has better power savings when compared with the CMOS. As the power is reduced in Reversible logic the area minimization can be achieved. Thus it can be used in the applications like low-voltage designs of mobile systems, where both power saving and overheating are very important due to the need for light weight and independent power supply.

VII. Conclusion And Future Work:

Reversible logic is an emerging technology with promising applications because of the low power dissipation. In this project, a novel architecture of basic Reversible logic gates are designed and realized. The important combinational circuits like half adder are designed using CMOS and Reversible Logic and the corresponding power saving are calculated.

In future, this design can be extended to combinational circuits like serial adder, multipliers like carry delay multipliers and Wallace tree multipliers.

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