



# Designing and Simulating a New Full Adder with Low Power Consumption

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**ABSTRACT:** A full adder circuit, regarding its ability to operate the Elementary Arithmetic, i.e. addition, subtraction, multiplication, and division, is considered as one the most important and applicable parts of digital processors in designing integrated circuits. Hence, the present paper tries to introduce a new full adder cell by the use of carbon Nano-tube transistors technology for achieving a circuit with optimal performance and low power consumption. The proposed design consists of 12 CNTFET transistors which have been connected through the passing transistor logic. Carbon Nano-tube transistors show remarkable advantage over MOSFET transistors in consumption power and performance speed. The simulation of the proposed design was conducted based on CNTFET model and by using HSPICE software with the applying voltage of 0.65V and in three different values of frequency, temperature, and capacitor load. The results revealed that the proposed design bears some advantages over the same circuits presented in previous literature.

**KEYWORDS:** Carbon Nano-tube Transistors, Full Adder Cell, Carbon Nano-tube, Designing Large-scale Integrated Circuits.

## I.INTRODUCTION

Since 1960s, calculations have come to the Electronics world. Since then, computational operations have been done by digital systems. Developments in different fields of science have intensified the need of access to information and storage them as well. The increase in the size of data necessitates the maximum computation power with the lowest consumption rate. At first, scientists intended to do so by increasing the operating power of processors and expanding the size of memories. This caused the human society to be faced with the problem of massive size of digital systems. Hence, researchers considered not only the improvements to processors, but also the reduction of the size of circuits. In 1965, Gordon Moore, former senior Deputy in Intel Co., proposed a theory based on this procedure that 18 transistors which are implemented in a chipset be duplicated and their size be reduced to the half each month.

The need to size reduction and high speeds has led the revolution of transistors from BJT to CNTFT. However, changes in the architecture of transistors could not fully satisfy the need for speed. Researchers then attempted to change the circuit structure. The fact that all four basic mathematical operations can be conducted with the help of a full adder circuit has offered a fundamental role to adder circuit in designing computational processors, and its performance is considered as a proper standard against which processors can be evaluated and compared. During past decades, so, researchers have done much to improve the performance of adders. In recent decades, different methods such as dynamic and static methods have been introduced for implementing a full adder. However, all circuits follow a common equation. Designers try to best operate the equation (1) in which A, B, and C are the circuit inputs and Sum and Carry are the outputs [1].

$$\begin{aligned} Sum &= A \oplus B \oplus C \\ Carry &= AB + AC + BC \end{aligned} \quad (1)$$

Considering the afore-mentioned points and using the Pass Transistor Logic, in this paper we aim to introduce an adder with optimal PDP and performance compared to previously designed circuits. In the following section, several



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previously designed adders are being introduced and after that, the proposed circuit is being presented. The output results from implementation process are then mentioned and finally the conclusion part follows.

## II. RELATED WORK

The period beginning from 1994 up to now can be considered as two dream decades for adder circuits and their designers. During the past 20 years, adder circuits have been experiencing much of evolutions and changes. One of the primary designing methods is Pass Transistor method[2][3][4]. In 1996, Abu-Khater and his colleagues designed one of the oldest circuits of this method. Transistor N experienced a voltage drop when it was up to pass the resource voltage; transistor P caused a voltage rise when it passed the zero voltage; so, this method was not able to initiate the following levels. Designers then could not connect the circuit output which was designed with pass transistor to next-level transistors gate. Reviewing the recent literature such as that of Reddy et al (2013), it can be concluded that in spite of the problems with the Pass transistor method, it is still considered as one the most common designing methods regarding its ability in omitting transistors and decreasing the volume of circuits.

C-CMOS (Complementary CMOS) is another method. The most well-known circuit from this method is called Mirror Adder which was introduced by Zimmemann et al in 1997 [5]. One main problem of this method was the huge number of pull up and pull down transistors used to form ordered structures. In fact, to construct such circuits equal number of N and P transistors operate complementarily with each other. From the other hand, it should be noted that the order/discipline existing throughout this method makes it as one of the most convenient methods for designing digital circuits. Considering such order, Navi et al (2008) introduced a full adder by using 24 transistors [6].

From the very beginning of changes in designing of adders, many dynamic circuits were introduced. For example, the circuit proposed by Mirzaei et al (2010) is considered as one of the most remarkable research efforts in this field [7]. By using the clock pulses method and charging and discharging the capacitor load, they reduced the number of 2N transistors of C-CMOS method to N+2. Since the half-length interval of processing time is merely devoted to capacitor charging or discharging in Dynamic logic, and many direct routes from VDD to the earth are omitted, the power consumption is remarkably being reduced. The main problems with this method are the common load and the invalidity of outputs in the half of processing interval.

In recent decade, a new method called the “Majority Function” was introduced. In this method, an odd number of transistors which are connected to each other in a parallel order designs a circuit in which the logical level with the highest rate of repeating would be transferred to the output. In other words, in Boolean logic the majority function is a function with N inputs to one output. The value of operator would be Zero if the 50% or more of arguments are zero, and vice versa. Table (1) demonstrates that the equation No.2 is effective.

Table (1): The integrity of operation of full adder

A	B	Cin	$\overline{Carry}$	$\overline{Carry}$	Sum
0	0	0	1	1	0
0	1	0	1	1	1
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	1

$$Sum = \text{majority}(A, B, C, \overline{Carry}, \overline{Carry}) \quad (2)$$

$$Carry = \text{majority}(A, B, C)$$

Many researchers used this principle and introduced a great number of full adders [8] [9][10]. Alizadeh et al (2011) presented six adder circuits and prepared a fine collection for other researchers [10]. Majority Function method has so



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many capacitors, so it necessitates a given time for charging and discharging each capacitor; this would increase the circuit performance delay to an unwanted extent. However, the designing size has been hugely decreased using this method. Hence, when the reduction of circuit face is the matter, majority function method stands as a desirable candidate.

Another designing method recently proposed is Hybrid or Mixed-mode Method. In this methodology, one part of the circuit is implemented by the Current mode circuits and the rest part by voltage mode circuits. This made the circuit enjoy some features of current mode circuits such as speed rise and decrease in transistors number. However, the high power consumption rate of current mode circuits is undeniable. The hybrid circuits have high power consumption rate which causes no remarkable improvement to PDP in spite of increasing the processing speed. Among circuits constructed based on this method, the fulladder Wairya proposed in 2011 may be noted [11].

According to the society's need to reduce the size of computational circuits, increase the performance speed, and drop the power consumption, the size of CMOS transistors was being reduced until it reached the size of 22nm. By the transistors entered to the realm below that size, they experienced some problems in their manufacturing process and performance. Carriers tunneling through the small channel, carriers tunneling through the thin Oxide of gate, very thin nonconductor coating, current leakage, power consumption rise, and limited subthreshold slope are some major problems with which Field Effect Transistors will be faced in Nano scale. To overcome such problems, some adjustments should be made in the existing structure of MOSFET. Also, new materials and technologies can be replaced with the Silicon used in Field Effect Transistors.

In 1991, Iijima introduced a new structure for carbon molecules called Multi Wall Carbon Nano Tube (MWCNT)[12]. In 1993, Iijima and his colleagues solved the problems with MOSFET by introducing Single Wall Carbon Nano Tube (SWCNT)[13]. Nano-tubes are created by rolling a Graphene sheet over a vector. By changing the size and the direction of that vector, also, the motion of carbon atoms around the Nano-tube axis, Nano-tube diameter would change. Nano-tube diameter is derived from equation (3) in which n and m are the two indexes of the mentioned vector, a is the distance between 2 carbon atoms, and D is the Nano-tube diameter [14].

$$D = \frac{a}{\pi} \sqrt{n^2 + m^2 + nm} \quad (3)$$

Changing the diameter would make the Nano-tube have different chemical features at different diameters. For example: when  $n-m \neq 3i$ , Nano-tube shows semi-conductive characteristic. Hence, this material can be considered as a proper alternative for transistor channel and for creating transistors with sizes smaller than 22nm. Flawless performance in scales smaller than 22nm, very high speed regarding the Ballistic feature throughout the channel, low power consumption due to miniature-scale size, producing high electrical current, adjusting threshold current by changing Nano-tube diameter, high electron motion, better control over channel forming, geometry, and same dimensions of n and p are some advantages with carbon Nano-tubes. A new window was opened to the researchers of full adder circuit designing field by creating such transistors, and they have been able to introduce great number of studies and researches in recent years [15]-[24]. These sort of transistors were used along with Majority function method to produce full adder circuits at first [15]-[19]. The circuit proposed by Navi et al (2010) is an example of mentioned procedure [16].

Amongst the different characteristics of carbon Nano-tubes, changing threshold voltage feature has gained the focus of attention. Equation (4) shows that transistor threshold voltage has an opposite relationship with Nano-tube diameter. Since the Nano-tube diameter is changeable, the threshold voltage can be changed too [14].

$$V_{th} = \frac{\sqrt{3}aV\pi}{3e.D} \quad (4)$$

Here, D is the Nano-tube diameter, "a" is the distance between 2 carbon atoms, V is the bound energy of Carbon, "e" is the charge value of the electron, and  $V_{th}$  is the threshold voltage of transistor. The use of this feature has been much of help for introducing various circuits [16],[17],[19]. Bagherzadeh et al (2011) tried to reduce the number of capacitors of the Majority Function to a possible minimum by taking advantage of mentioned feature [19]. Their effort caused the number of capacitors to fall to its minimum, but the problems with Majority Function method were still hanged on.

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In the recent year, excluding the capacitor from circuits have drawn the researchers' attention. Papers and researches conducted through C-CMOS method by Ghorbani and his colleagues in 2012 and 2013 are some fine examples [23],[24]. As it was mentioned before, C-CMOS method necessitates so many transistors; this causes the linear resistance rises, so reducing the number of transistors is as necessary as omitting the capacitor from circuit.

When carbon Nano-tube transistors, which enjoyed the characteristic of changeable  $V_{th}$  stepped into the Electronics world, researchers minimalized the voltage drop in P transistors, as well as N transistors. Regarding this, the use of Pass transistors method seemed to be a good choice when the reducing the number of transistors and increasing the processing speed were mattered. It should be noted that the performance of this method is very much like the Full-Swing method; so, when the reliability matters, this method is not recommended. Sharifi et al (2011) is one of the newest papers from this method which was introduced by the use of Pass transistors [21].

According to the importance of optimal performance of processors and the superiority of the characteristics of Nano-tubes over MOSFET, the second part of the present paper is devoted to introduce a full adder circuit with proper performance which takes advantage of carbon Nano-tubes technology. In the third part, designing and implementing procedure with HSPICE software will be discussed in detail. Also, drawing a comparison between the proposed circuit and other designs regarding the power consumption shows the performance delay and PDP delay in the latters. At the final part, the conclusion of the present study will be stated.

### III.THE PROPOSED CIRCUIT

Resistor and Capacitor are two main destructive agents which spoil the performance optimization process. Most of previously designed circuits in the literature were implemented by carbon Nanto-tube technology and Majority Function method. Hence, the existence of capacitors has caused the rise of power consumption and performance delay in such circuits. Having too much transistors in circuit design would increase the total resistance. So, in this study the aim was to reduce the number of transistors and, consequently, the total resistance by taking advantage of Pass Transistors. In addition, there is no capacitor in the proposed circuit, Fig. 1, due to ignoring the Majority Function method.

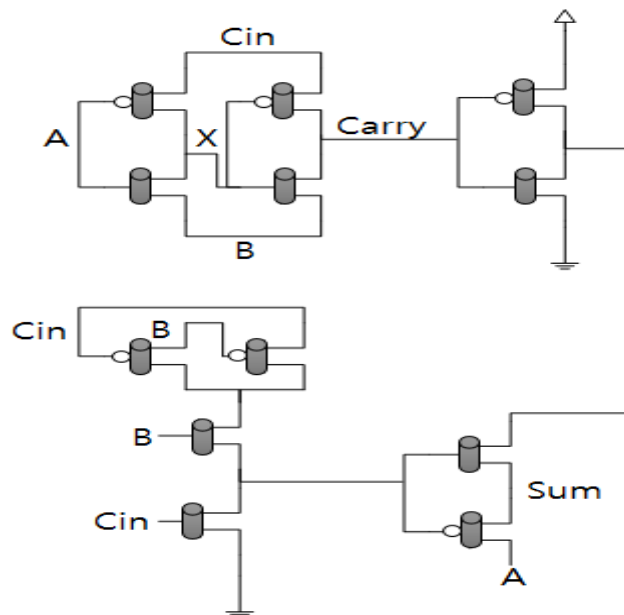


Figure 1: The proposed circuit schema



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The proposed circuit introduced a new style in implementing Carry function: it just used four Carbon Nano-tube transistors and simultaneously presented the Carry output producing part and Sum output producing part of the circuit in two levels, without using any capacitor or resistor.

Table (2) shows that Carry follows the equation No. 5:

$$\begin{aligned}
 A = 0 \ \& \ C_{in} = 0 \Rightarrow \text{Carry} = C \\
 A = 0 \ \& \ C_{in} = 1 \Rightarrow \text{Carry} = B \\
 A = 1 \ \& \ B = 0 \Rightarrow \text{Carry} = C \\
 A = 1 \ \& \ B = 1 \Rightarrow \text{Carry} = B
 \end{aligned}
 \tag{5}$$

Table (2): the integrity of performance for full adders

A	B	Cin	Carry
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Whenever A=0, P transistor gets on, and point X=Cin; now, whenever Cin=0, P transistor transfers Cin value to the Carry output; if Cin=1, N transistor transfers the value of B to the Carry, and the first 2 conditions are met. Also, when A=1, then X=B, i.e. whenever B=0, the circuit output would be Cin with the help of P transistor. When B=1, N transistor helps the circuit output to be equal to signal B, as a result, two last conditions will be satisfied as well. The proposed circuit introduced a new style in implementing Carry function: it just used four Carbon Nano-tube transistors and simultaneously presented the Carry output producing part and Sum output producing part of the circuit in two levels, without using any capacitor or resistor.

Since in multi-bit adders the speed of creating of Carry bits is of great importance, it was aimed to improve the Carry at first. The Sum producing part, but, has a remarkable role, so in the proposed circuit a new designing style has been introduced for Sum part. Equation (6) is then derived from Table (2).

$$\begin{aligned}
 \text{IF } (B \oplus C_{IN} = 0) \\
 \text{SUM} &= A \\
 \text{ELES} \\
 \text{SUM} &= \text{CARRY}
 \end{aligned}
 \tag{6}$$

As you can see in Fig.1, by connecting the output of XOR circuit to the gate of a P-type transistor, B+CIN=0 and then the output of SUM will be equal to CARRY. By connecting the output of XOR circuit to the gate of an N-type transistor, B+CIN=1 and then the output of SUM will be equal to A. as it was mentioned earlier, researchers have been trying to clean destructive factors such as capacitors out of circuits in recent years. But, omitting capacitors causes the number of transistors to be increased. According to the majority of books on VLSI, transistor is a linear resistor increase of which would increase the linear resistance in circuit. In other words, in spite of the drop which has been made to the number of capacitors in circuits, another destructive factor has been injected into it. The presence of each one of these spoiling factors would behold the performance of circuit. Hence, the aim has been to not to use a capacitor and to use a minimum number of transistors in the proposed design.

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It is anticipated that the proposed circuit enjoys more speed compare to the circuit illustrated in Fig.2 which has been designed by seven transistors and with Majority Function method in 2009 by Tavi et al[15].

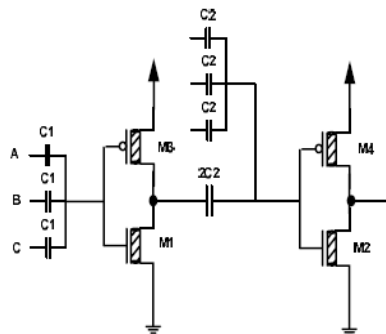


Figure 2: the Schema of the full adder circuit proposed in Tavi et al (2009)[15]

On the other side, equation (6) is used for computing the power consumption of digital circuits. In this equation,  $F_{clk}$  shows the system clock frequency,  $V_{i\ swing}$  is the Swing voltage at the  $i^{th}$  loop (in ideal mode  $V_{dd}$ ),  $C_{i\ load}$  is the load capacitor at  $i^{th}$  loop,  $\alpha_i$  is the activation coefficient at  $i^{th}$  loop,  $I_{isc}$  is the short circuit current, and  $I_l$  is the leakage current from  $i^{th}$  loop[1].

$$\begin{aligned}
 P_{total} &= P_{dynamic} + P_{shortcircuit} + P_{static} \\
 &= V_{dd} F_{clk} \sum_i V_{iswing} C_{iload} \alpha_i \quad (7) \\
 &+ V_{dd} \sum_i I_{isc} + V_{dd} I_l
 \end{aligned}$$

Taking the above equation into consideration, it seems that the proposed circuit can reduce the static power consumption since it has minimized the direct routes from VDD to the earth.

The proposed circuit not only reduce the number of capacitors compared to the circuit illustrated in Fig.3, but also drop the number of transistors to four[18]. It seems that the proposed design has better power and PDP performance compared to below circuit.

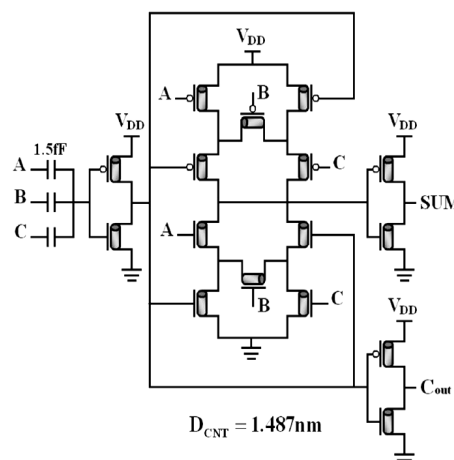


Figure 3: the Schema of the adder circuit introduced in Navi et al (2011)[18]

Khatir et al (2012) introduced an adder circuit which is illustrated in Fig. 4 [18]. This is a three-capacitor circuit, like previous circuits. This circuit has been implemented by 14 carbon Nano-tubes which is 2 times bigger than the number



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used in our proposed design. It is predicted that the proposed circuit has better power consumption and speed over the mentioned circuit.

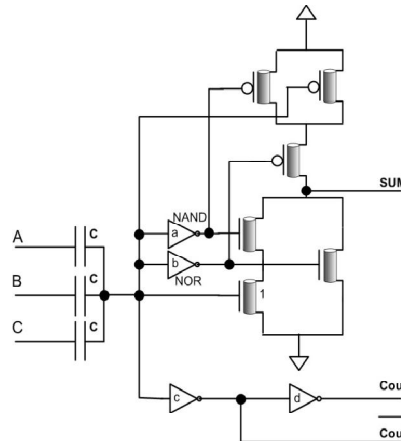


Figure 4: the Schema of the adder circuit introduced in Khatir et al (2012)[17]

As equation (6) shows, increasing the value of load capacitor would increase the power consumption. Another factor that plays an important role in power consumption rate is the direct routes from VDD to the earth. For this reason, in the proposed design the static routes are omitted by the use of Pass Transistors method. The possible minimum number of transistors in the proposed circuit is considered as another advantage over other designs. This would improve the power consumption to a great extent.

## IV. DISCUSSION AND COMPARISON

Description of tests will be presented in four distinctive sections. The first section explains the details on how the proposed circuit was implemented by HSPICE software. The second and third sections evaluate the performance integrity of the circuit and compare the results of the simulation of the proposed design and previous circuits by the help of the HSPICE software in same conditions.

## V. TEST CONDITIONS DESCRIPTION

The proposed circuit in this study has been implemented based on 23nm technology, by HSPICE software, and considering the parameters mentioned in Table (3).

Table (3): Parameters of carbon Nano-tube Model

Parameter	Value
Lch	32nm
Lgeff	100nm
Lss	32nm
Ldd	32nm
Kgate	16
Tox	4nm
Csub	40pF/m
Efi	6eV
Tubes	3

In analyzing the speed of the proposed circuit, three different values (1.4FF, 2FF, and 2.4FF) for load capacitor were used at temperature of 27 degree of C and frequency of 31.25MHz. Also, different frequencies of 62.5 MHz, 6.41MHz, and 31.25MHz have been considered for analyzing power consumption at temperature of 27 degree of C and load

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capacitor value of 1.4FF. The applying voltage was constant for all simulation moods and set to be 0.65 V. The analyze type is Transient analysis.

## VLEVALUATIONOF PERFORMANCE INTEGRITYOF THE CIRCUIT

In evaluating the performance integrity of circuits two main points should be taken into account. First, it should be evaluated that whether outputs obey a correct logic in relation to inputs. As it goes, the matter of Full Swing comes into scene. Form the viewpoint of Reliability, if a circuit experiences voltage drop or voltage rise at its output, the smallest noise may have the correct logic gone and, as a result, circuit reliability would decrease. To consider such points, the proposed circuit was implemented by HSPICE software, at load capacitor value of 1.4FF, at temperature of 27 degree of C, and Frequency of 25.31MHz.

Applying eight needed patterns for A, B, and C inputs, SUM and CARRY outputs have been calculated as in Fig. 5. Fig.5 shows that the proposed circuit enjoys integrated performance for all eight patterns.

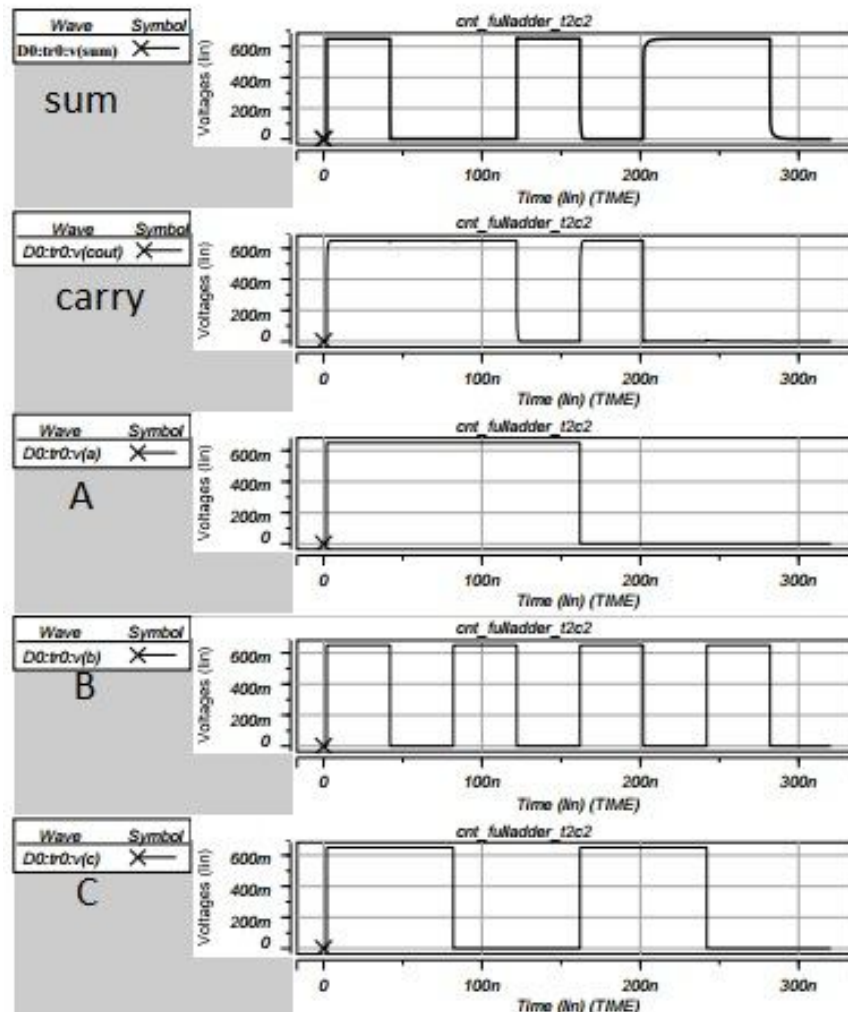


Figure 5: input and output wave form for circuit No. 4

The analysis of Fig 5 shows that the proposed circuit output is close to Full Swing. This may be unbelievable as first, since this circuit bears Pass transistors. But, by referring to equations 3 and 4 it turns out that this is possible, as the carbon Nano-tube transistors would show proper swing by changing the threshold voltage. Since the carbon Nano-tube



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transistors have been used in proposed circuit, output will be close to the Full Swing mode by changing the threshold voltage.

## VII.COMPARINGTHE RESULTSOF HSPICE

In this section, the results of the simulation of the proposed design and previous circuits by the help of the HSPICE software and in conditions cited in section 3-1 are being compared.

Fig. 6 and Table 4 which show the power consumption rate at three different frequencies reveal that power consumption at the frequency of 31.25MHz has reduced 93 % compared to Navi et al [15], 91% compared to NAvi et al [18], and 96% compared to Khatir et al [17]. The power consumption at the frequency of 41.6 MHz has reduced 94% compared to Navi et al [15], 90% compared to NAvi et al [18], and 95% compared to Khatir et al. Finally [17], the power consumption of proposed circuit at frequency of 62.5MHz has reduced 91 % compared to Navi et al [15], 90% compared to NAvi et al [18], and 95% compared to Khatir et al [17].

Table 4: Output Results of circuit power consumption for three different frequency

	62.5MHZ	41.6MHZ	31.25MHZ
Full Adder [15]	25.9E-7 W	25.9E-7 W	25.8E-7 W
Full Adder [18]	24.7E-7 W	24.6E-7 W	24.4E-7 W
Full Adder [17]	53.3E-07W	51.8E-7 W	53.3E-07 W
Full Adder proposed	2.4E-7 W	2.5E-7 W	2.3E-07 W

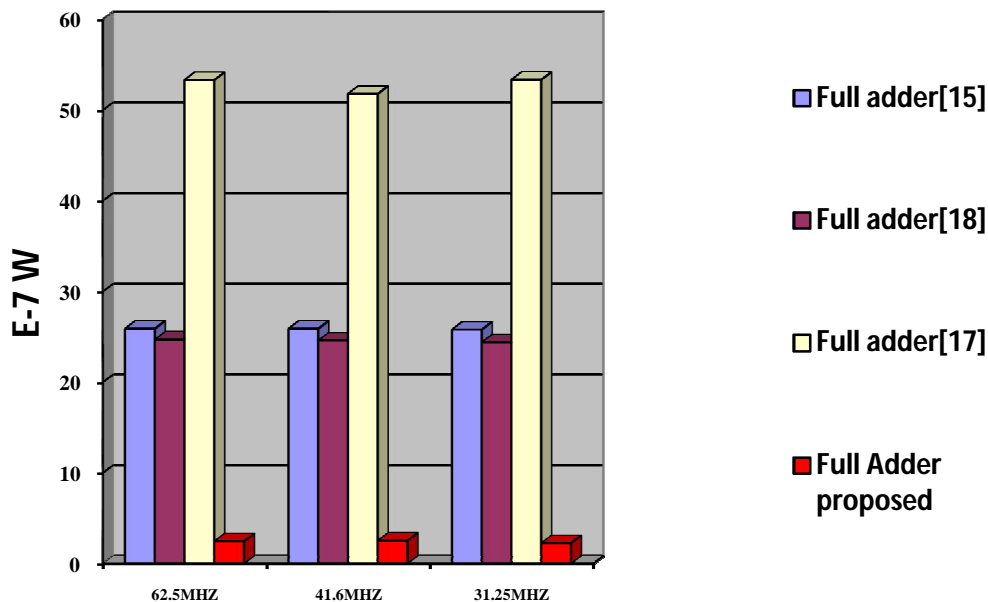


Figure 6: Power Consumption Comparison diagram

The evaluation of Fig. 7 and table (5) shows that the proposed circuit at the load capacitor of 1.4FF reveals 51% less performance delay compared to the circuit of Navi et al [15] and 18% compared to the circuit of Khatir et al[17].

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However, proposed circuit has experienced 49% more performance delay compared the circuit of Navi et al[18]. At the load capacitor value of 2FF, the proposed circuit has showed 41% less performance delay compared to the circuit of Navi et al[15] and 12 % compared to the circuit of Khatir et al[17], and has only experienced 48 % speed fall compared to Navi et al[18]. Finally, At the load capacitor value of 2.4FF, the proposed circuit has showed 37% less performance delay compared to the circuit of Navi et al[15] and 12% compared to the circuit of Khatir et al[17], and has only experienced 48 % speed fall compared to Navi et al[18].

Table 5: Output Results of circuit delay for three different value of load capacitor

	1.4FF	2FF	2.4FF
Full Adder [16]	5.6E-11S	6.2E-11S	6.4E-11S
Full Adder [19]	1.48E-11S	1.88E-11S	2.11E-11S
Full Adder [22]	3.38E-11S	4.13E-11S	4.6E-11S
Full Adder proposed	2.77E-11S	3.64E-11S	4.03E-11S

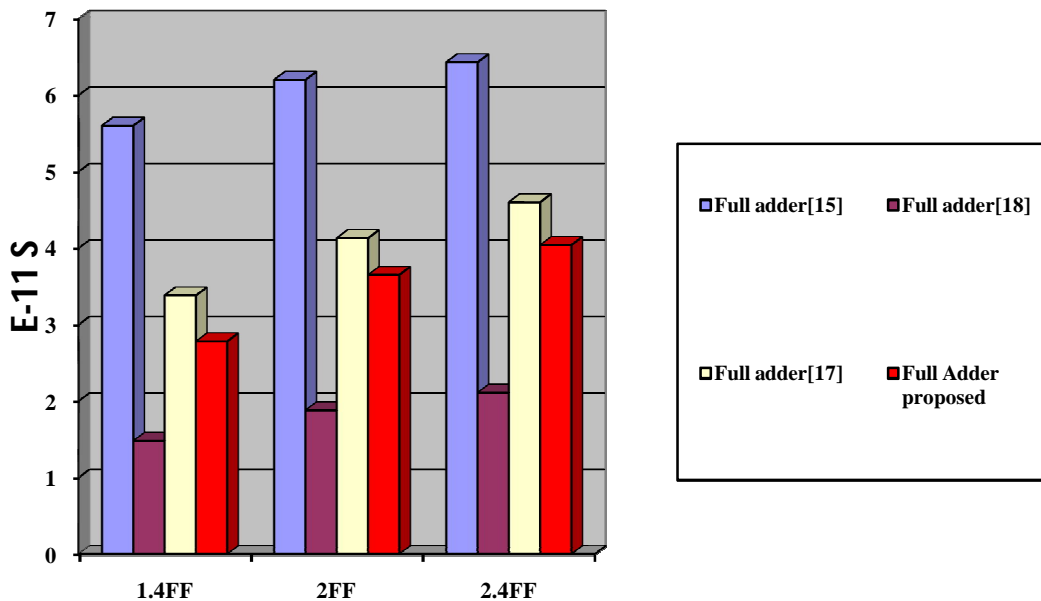


Figure 7: Delay Comparison diagram

PDP is the result of multiplication of power consumption and delay; so, it is one of the best parameters for comparing digital circuits.

According to table 6, the proposed circuit has maintained its superiority over its counterparts by changing the load capacitor value and the frequency.



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Table (7): output results of PDP

	1.4FF	2FF	2.4FF	62.5MHZ	41.6MHZ	31.25MHZ
Full Adder [15]	144.61E-18J	160.34E-18J	166.54E-18J	145.36E-18J	144.92E-18J	144.61E-18J
Full Adder [18]	36.986E-18J	46.380E-18J	51.906E-18J	37.911E-18J	37.794E-18J	36.986E-18J
Full Adder [17]	180.14E-18J	220.67E-18J	245.81E-18J	179.79E-18J	174.89E-18J	180.14E-18J
Full Adder proposed	6.2482E-18J	8.5145E-18J	9.6451E-18J	6.8368E-18J	7.0232E-18J	6.2482E-18J

## VIII. CONCLUSION

A new full adder cell with optimal performance and by Carbon Nano-tube technology was introduced in this study. The main idea of the present paper was to use the Pass Transistors in order to achieve the minimum number of transistors and omit the capacitors in full adder cell design. The results of simulation which was conducted based on Cntfet model and by HSPICE software show that the proposed full adder cell bears remarkable optimization over the existing designs regarding the power consumption rate. Power consumption reduction in proposed circuit results the optimization of PDP compared to other circuit designs. Hence, the proposed design fits suitable for applications that necessitate low power consumption and optimal performance. For future studies, improving the speed of full adder circuits while maintaining their power consumption rate at a low level is a recommended field of research. Avoiding the transistors gates and preceding level outputs from being connected is suggested as a proposed idea.

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