ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

Proceedings of International Conference On Global Innovations In Computing Technology (ICGICT'14)

Organized by

Department of CSE, JayShriram Group of Institutions, Tirupur, Tamilnadu, India on 6th & 7th March 2014

Error Reduction in WiMAX Deinterleaver Address Generator by Using Majority Logic Circuit

A.Nandhini[1], D.Poornima Devi[2]

Assistant Professor, Sri Vidya college of Engineering and Technology, Tamilnadu, India[1]

PG Student, Sri Vidya college of Engineering and Technology, Tamilnadu, India[2]

Abstract: A low-complexity and novel technique is proposed to efficiently implement the address generation circuitry of the 2-D deinterleaver used in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA).The use of an internal multiplier of FPGA and the sharing of resources for quadrature phase-shift keying, 16-quadrature-amplitude modulation (QAM), and 64-QAM modulations along with all possible code rates makes our approach to be novel and highly efficient when compared with conventional look-up table-based approach. We propose majority logic circuit for interleaver structure to reduce hardware complexity and error rate in WiMAX system. We also propose bi-orthogonal decoding to improve the hardware utilization efficiently. The proposed approach exhibits significant improvement in the use of FPGA resources. Exhaustive simulation has been carried out to claim supremacy of our proposed work.

Keywords: WiMAX, FPGA, deinterleaver and simulation

I. INTRODUCTION

BROADBAND wireless access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies [1]. IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX [2]. The channel interleaver employed in the WiMAX transreceiver plays a vital role in minimizing the effect of burst error. In this brief, a novel, low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transreceiver eliminating the requirement of floor function is proposed. Very few works related to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature. The work in [3] demonstrates the grouping of incoming data streams into the block to reduce the frequency of memory access in a deinterleaver using a conventional look-up table (LUT)- based CMOS address generator for WiMAX. Khater *et al*. [4] has described a hardware description language (VHDL)- based implementation of address generator for IEEE 802.16e channel interleaver with only a 1/2 code rate. In [5], the authors have described a finite-state machine (FSM)-based address generator of the same interleaver for all permissible code rates and modulation schemes. Both [4] and [5] are tested on the field-programmable gate array (FPGA) platform. Asghar and Liu in [6] has made 2-D translation of the functions used in WiMAX channel deinterleaver to claim efficient hardware architecture. However, the derivations in [6] do not clearly explain the design issues, particularly for 64-quadrature-amplitude modulation (QAM). Hardware implementation of floor function is very complex and consumes abnormally large amount of resources [6]. Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization, etc. A comparative study with a LUT-based technique confirms the superiority of our proposed design. As compared with the complicated and lengthy expressions, particularly for 16-QAM and 64-QAM, due to the 2-D translation in [6], a compact and user-friendly mathematical representation and subsequent algorithm is proposed. The mathematical expressions have formally been proven using [6]. Our proposed algorithm when realized by digital hardware results in low-complexity architecture for the address generator compared with prevailing technique. A detailed view of the proposed hardware compared with [6] is presented. To make the design compact, the authors adopted optimization by sharing the common hardware between the modules for quadrature phase-shift keying

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

Proceedings of International Conference On Global Innovations In Computing Technology (ICGICT'14)

Organized by

Department of CSE, JayShriram Group of Institutions, Tirupur, Tamilnadu, India on 6th & 7th March 2014

(QPSK), 16-QAM, and 64-QAM. This architecture is modeled in VHDL and implemented on the Xilinx Spartan-3 FPGA. Software simulation using ModelSim is performed to verify the functionality of the proposed algorithm and hardware. FPGA implementation results along with their possible comparison with recent similar work have been made. In this brief, use of FPGA's embedded multiplier provides performance improvement by reducing interconnection delay, efficient resource utilization, and lesser power consumption compared with a configurable logic block-based multiplier. Our work shows betterment over the LUT technique to the tune of approximately 49% in terms of maximum operating frequency.

II. PROPOSED SYSTEM

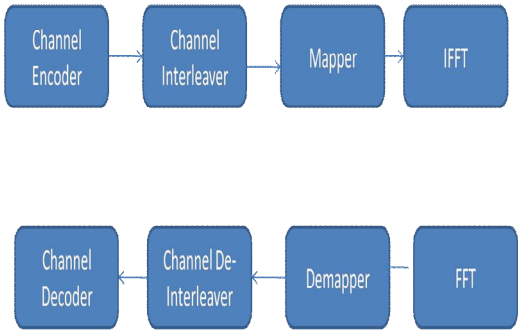


Fig1.Proposed block diagram

The mandatory blocks of a WiMAX transreceiver are shown in Fig. 1. Data stream received from a source is randomized before being encoded by two forward error correction (FEC) coding techniques, namely, Reed–Solomon (RS) and convolutional coding (CC). The channel interleaver permutes the encoded bit stream to reduce the effect of burst error. When convolutional turbo code (CTC) is used for FEC, being optional in WiMAX, the channel interleaver is not required, since CTC itself includes an interleaver within it [7]. Modulation and construction of orthogonal frequency-division multiplexing symbols are performed by the two subsequent blocks, namely, mapper and inverse fast Fourier transform of Fig. 1. In the receiver, the blocks are organized in the reverse order enabling the restoration of the original data sequence at the output [8]. Two-dimensional block interleaver/deinterleaver structure, which is used as a channel interleaver/deinterleaver in the WiMAX system, is described in Fig. 2. It has two memory blocks, namely, M-1/2 and an address generator. In block interleaving, when one memory block is being written, the other one is read, and vice versa. When sel = 1, write-enabled signal *WE* of M-1 is active. During this period, the input data stream is written in M-1 as it receives the write addresses.

Simultaneously, an interleaved data stream is read from M-2 as it is supplied with the read addresses. After the memory blocks are written/read up to the desired location as specified by interleaver depth, the status of sel signal is changed to swap the read/write operation.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

Proceedings of International Conference On Global Innovations In Computing Technology (ICGICT'14)

Organized by

Department of CSE, JayShriram Group of Institutions, Tirupur, Tamilnadu, India on 6th & 7th March 2014

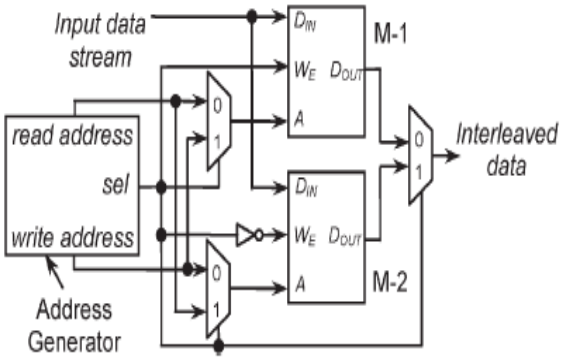


Fig2.Deinterleaver Architecture

Here, the proposed algorithm for address generator of the WiMAX deinterleaver along with its mathematical background has been described. A MATLAB program is developed using (3) and (4) for all modulation schemes and code rates. Due to the presence of a floor function in (3) and (4), their direct implementation on an FPGA chip is not feasible. Table II shows the deinterleaver addresses for the first four rows and five columns of each modulation type. As d = 16 is chosen, the number of rows are fixed (= d) for all Ncbps, whereas the number of columns are given by Ncbps/d.

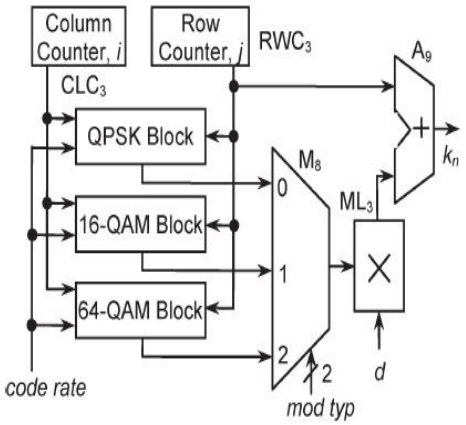


Fig3:Proposed deiniterleaver architecture

III. SIMULATION RESULTS

The verilog HDL program developed for the proposed WiMAX deinterleaver address generator is downloaded on the Xilinx Spartan-3 (Device XC3S400) FPGA [11]. Table IV shows the HDL synthesis report. The two blocks, namely, MO0 and MO1 of Fig. 3(b), are implemented using the mod 2n function of VHDL. The requirement of $i$mod 3 (MO2) and j mod 3 (MO3) functions in 64-QAM circuit are fulfilled by designing two small ROMs of dimension 16 × 3-bit and 64 × 3-bit, respectively, as the MOD 3 function is not supported in VHDL. The use of the rest of the logic circuits is obvious in the design. As the FPGA-based implementation of the WiMAX deinterleaver address generator has not been found in the literature, direct comparison of the results of our proposed work could not be carried out. However, implementation of the conventional LUT-based technique of address generation for the WiMAX 2-D

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

Proceedings of International Conference On Global Innovations In Computing Technology (ICGICT'14)

Organized by

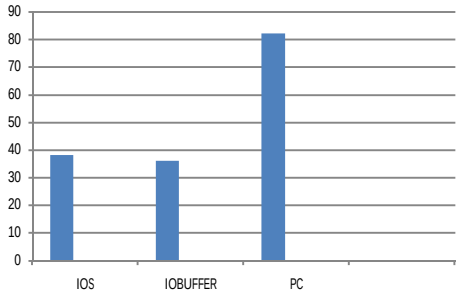
Department of CSE, JayShriram Group of Institutions, Tirupur, Tamilnadu, India on 6th & 7th March 2014

deinterleaver on the same FPGA is made in the similar manner as proposed in [12]. In the latter case, the LUTs are modeled using FPGA's embedded memory, i.e., block RAM [11], to reduce the memory access time. For fairness of comparison, three block RAMs are used, i.e., one for each modulation scheme to house the address LUT of various interleaver depths. Efficient use of block RAMs is made possible by exploring the feature that, within a modulation scheme, the address LUT of a smaller *N*cbps is the subset of the address LUT of the larger *N*cbps.

Performance Analysis:

Performance Evaluation Parameters	Resource Utilization
Adder	1
IOs	38
IO Buffer	36
Latency	4.93ns
Power Consumption	82mW

Performance Analysis Graph:



IV. CONCLUSION

This project has proposed a novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver supporting all possible code rates and modulation patterns as per IEEE 802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using VHDL. Comparison of our proposed work with a conventional LUT-based method and also with a recent work show significant improvement on resource utilization and operating frequency.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014

Proceedings of International Conference On Global Innovations In Computing Technology (ICGICT'14)

Organized by

Department of CSE, JayShriram Group of Institutions, Tirupur, Tamilnadu, India on 6th & 7th March 2014

REFERENCES

[1] W. Konhauser, "Broadband wireless access solutions—Progressive challenges and potential value of next generation," Wireless Pers. Commun., vol. 37, no. 3/4, pp. 243–259, May 2006.
[2] B. Li, Y. Qin, C. P. Low, and C. L. Gwee, "A survey on mobile WiMAX," IEEE Commun. Mag., vol. 45, no. 12, pp. 70–75, Dec. 2007.
[3] Y. N. Chang and Y. C. Ding, "A low-cost dual mode de-interleaver design," in Proc Int. Conf. Consum. Electron., 2007, pp. 1–2.
[4] A. A. Khater, M. M. Khairy, and S. E.-D. Habib, "Efficient FPGA implementation for the IEEE 802.16e interleaver," in Proc. Int. Conf. Microelectron., Marrakech, Morocco, 2009, pp. 181–184.
[5] B. K. Upadhyaya, I. S. Misra, and S. K. Sanyal, "Novel design of address generator for WiMAX multimode interleaver using FPGA based finite state machine," in Proc. 13th Int. Conf. Comput. Inf. Technol., Dhaka, Bangladesh, 2010, pp. 153–158.
[6] R. Asghar and D. Liu, "2D realization of WiMAX channel interleaver for efficient hardware implementation," in Proc. World Acad. Sci. Eng. Technol., Hong Kong, 2009, vol. 51, pp. 25–29.
[7] IEEE Standard for Local and Metropolitan Area Networks—Part 16: Air Interface for Fixed Broadband Wireless Access Systems—Amendment 2, IEEE Std. 802.16e-2005, 2005.
[8] M. N. Khan and S. Ghauri, "TheWiMAX 802.16e physical layer model," in Proc. IET Int. Conf. Wireless, Mobile Multimedia Netw., Mumbai, India, 2008, pp. 117–120.
[9] J. G. Andrews, A. Ghosh, and R. Muhamed, Fundamentals of WiMAX: Understanding Broadband Wireless Networking. Upper Saddle River,NJ, USA: Prentice-Hall, 2007, ch. 8.
[10] Local and Metropolitan Networks—Part 16: Air Interface for Fixed Broadband Wireless Access Systems, IEEE Std. 802.16-2004, 2004.
[11] Xilinx Spartan-3 FPGA Family: Complete Data Sheet, Xilinx, Inc., San Jose, CA, USA, 2012.
[12] B. K. Upadhyaya and S. K. Sanyal, "An improved LUT based reconfigurable multimode interleaver for WLAN application," Int. J. Recent Trends Eng. Tech., ACEEE, vol. 6, no. 2, pp. 183–188, 2011.
[13] I. Kuon and J. Rose, "Measuring the gap between FPGAs and ASICs," in Proc. Int. Symp. Field Programm. Gate Arrays, Monterey, CA, USA, 2006, pp. 21–30.