Fault Diagnosis in H-Bridge Multilevel Inverter Drive Using Wavelet Transforms

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ABSTRACT: Induction motors are normally used in the industrial environments. Industry has begun to use energy efficient high power rating electrical drives. Multilevel inverter drives have become a solution for energy efficient drives in recent years. There may be probability for occurring of many faults in the multi-level inverter fed induction motor drive due to its complex switching patterns. So it is necessary to identify types of fault and its location in order to improve the reliability of the drives. In this paper presents a new fault diagnosis technique based on discrete wavelet transforms for H-bridge multilevel inverter drives. For demonstrating the proposed method one H-Bridge open circuit fault are considered in the H-Bridge multilevel inverter. The 30V prototype system is developed and controlled by Renesas processor. LabVIEW based data acquisition system is used to acquire the real time inverter output voltage and current. The experimental results are shown to illustrate the effectiveness of the proposed method.

Keywords: Multi-level inverter; discrete wavelet transforms, fault diagnosis, LabVIEW

I. INTRODUCTION

Multilevel inverter drives has become the most efficient drives in the industries in recent times. Many types of multilevel inverter topologies is been discussed [1] [2] and for the medium power rating machines the H-Bridge multilevel inverter becomes most efficient drive. The schematic diagram of the H-Bridge multilevel inverter is illustrated in the Fig 1. The industries are relying upon the induction motors for their manufacturing process and the multilevel inverters are used as the drives for the induction motors. If any faults occur in the multilevel inverters the passive protection systems such as the relays and protective circuits will cut the supply and whole system will get shut down. This will affect the production of the industry which incurs loss. So a fault diagnosis method becomes mandatory for the industries when some kind of faults occur in the multilevel inverter drives.

In order to maintain continuous operation for a multilevel inverter system, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary. Faults should be detected as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail. Research on fault diagnosis of the inverters initially focused on the voltage source inverters in which some of the fault modes is been discussed in [3]. A review of the various researches in the fault diagnosis using the wavelet technique is been given in [4]. The wavelet transforms analyze a signal simultaneously in time and frequency domains. The wavelet transforms are very useful in analyzing non-stationary, non-periodic, intermittent, and transient signals.

Therefore, a number of wavelet based techniques are developed and implemented for signal manipulation and interrogation. The wavelet transforms are applied in the investigation of diverse physical phenomena such as climate analysis, financial market analysis, heart monitoring, etc. The diagnostic methods have discussed in [5] which is using the principal component analysis for the feature extraction system. The wavelet based fault diagnosis for the multilevel inverter and concepts of the discrete wavelet transforms is explained in [6] [7]. Discrete wavelet transforms is successfully implemented in leakage current system of insulator to extract the feature of the signal [8]. The hardware details for the multi-level inverter is been given in [9]. The various PWM techniques for the switching of the inverter are discussed in [10]. There are many researches has been made on this topic of fault diagnosis but still to improve the reliability of the drives using multilevel inverter a fault diagnostic method using discrete wavelet transform is been illustrated in the following sections.

II. H-BRIDGE MULTI-LEVEL INVERTER

In the proposed fault diagnostic method a H-Bridge multi-level inverter is been taken for the analysis of the fault. The circuit diagram for the H-Bridge inverter is shown in Fig 1. It consists of 24 switches of which 8 switches per phase in

which each pair of the switch will conduct at the same time. To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$m=2S+1 \qquad (1)$$

where S is the number of dc sources. For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 1 illustrates the schematic diagram of wye-connected -level inverter using three H-bridge cells and three SDCSs per phase, which will be used in the proposed method.
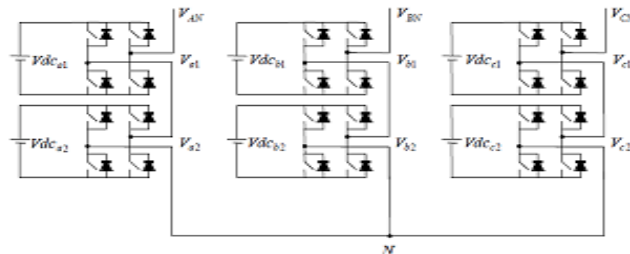

Fig 1. H-Bridge Multi-Level Inverter

V$_{AN}$ is voltage of phase A, which is the sum of V$_{a1}$, V$_{a2}$, and V$_{a3}$. The same idea is applied to phase B and phase C. To synthesize five-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively. According to three-phase theory, line voltage can be expressed in term of two phase voltages. For example, the potential between phase A and B is so-called V$_{AB}$, which can be written as follows:

$$V_{AB} = V_{AN} - V_{BN} \qquad (2)$$

where,
V_{AB} is line voltage V_{AN} is voltage of phase A with respect to point N and V_{BN} is voltage of phase B with respect to point N theoretically, the maximum number of line voltage levels is 2m-1, where m is the number of phase voltage level.

III.   DISCRETE WAVELET TRANSFORMS

In the continuous wavelet transform (CWT), the mother wavelet is dilated and translated continuously over a real continuous number system. Therefore, it can generate substantial redundant information. The mother wavelet can be dilated and translated discretely by replacing a=a$_o$^{m} and b=nb$_o$a$_o$^{m}, where a$_o$ and b$_o$ are the fixed constants with a$_o$>1, b$_o$>0, and m, n belongs to N. Here N is the set of positive integers. Then the discretized mother wavelet function can be defined as

$$\Psi_{m,n}(t) = a_o^{-\frac{m}{2}} \Psi\left(\frac{t - nb_o a_o^m}{a_o^m}\right) \qquad (3)$$

And the corresponding Discrete Wavelet Transform (DWT) can be defined as

$$DWT_\Psi x(m, n) = \int_{-\infty}^{\infty} x(t)\Psi_{m,n}^*(t)dt \qquad (4)$$

DWT decomposes a signal into various scales with different time and frequency resolutions. In the DWT, the procedure starts with passing the discrete signal x[n] of length N through a digital low pass filter with impulse response g[n] and a digital high pass filter with impulse response h[n]. The output of these filters consists of N wavelet coefficients. This constitutes first level of decomposition of the discrete signal and can be mathematically expressed as

$$a^1[n] = \sum_{k=0}^{N-1} g[k]x[n-k] \tag{5}$$

$$d^1[n] = \sum_{k=0}^{N-1} h[k]x[n-k] \tag{6}$$

The approximation coefficients ($a1$) at first level of resolution are used as inputs for another pair of wavelet filters (identical with the first pair) after being down sampled by two. The filters at second level of resolution generate sets of approximations and details coefficients of length N/2. This constitutes second level of decomposition of the discrete signal and can be mathematically expressed as

$$a^2[n] = \sum_{k=0}^{\frac{N}{2}-1} g[k]a^1[2n-k] \tag{7}$$

$$d^2[n] = \sum_{k=0}^{\frac{N}{2}-1} h[k]a^1[2n-k] \tag{8}$$

Fig.2 shows the two-level decomposition of a discrete signal of the discrete wavelet transform. It uses the high pass filters (H) and the low pass filters (G) in the decomposition process. If a wavelet function matches the shape of a signal well at a specific scale and location, then a large transformation value will be generated. On the other hand, if the wavelet function and signals do not correlate well, then a low value of transformation will be generated.
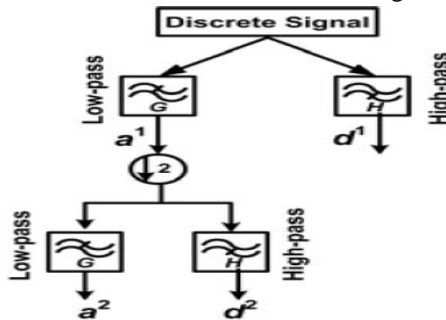

Fig 2. Two-Level Decomposition of a Discrete Signal of the DWT

IV   EXPERIMENTAL SETUP

Fig 3. shows the hardware circuit diagram of the three H-Bridge Multi-level inverter which each phase of the multi-level inverter consists of two H-Bridges with four switches in each H-Bridge. The gate pulse for the switches is given using Renesas processor which is as shown in the Fig 3. Fig4. shows the experimental setup of the proposed system. The gate drive circuit used here is the IR2110 and opto-isolator is used for the protection of the processor from the high voltage side which is the MOSFET switches. Since the switches are working in a high voltage and current the processor and the driving IC's are not able to withstand that much amount of higher voltages so we are connecting it through an opt-isolator.
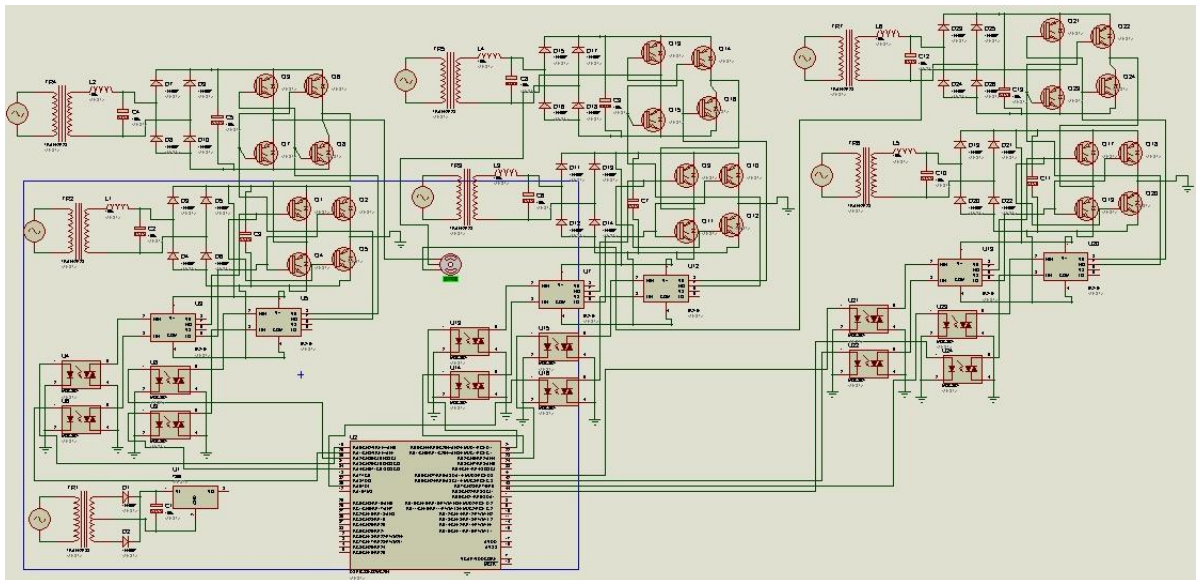
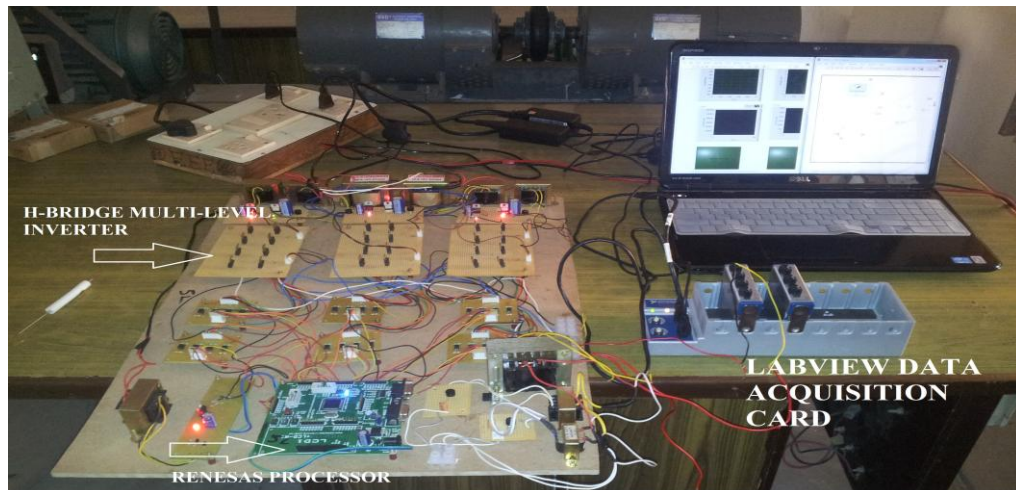Fig 3. Hardware Circuit diagram of Proposed System

Fig 4. Experimental Setup

The gate pulse for the H-Bridge multi-level inverter is generated based on sinusoidal pulse width modulation. The fault in the circuit is created by opening one H-Bridge in any one of the phase in the inverter which is called as H-Bridge open circuit fault. This voltage and current values are measured from the NI DAQ card and it is loaded in excel file. These values are again copied in the matlab file and it is used for the feature extraction using discrete wavelet transforms. A MATLAB program is used to extract the features of the faulted signals in which the signal is divided into 10 levels and the maximum, mean and the standard deviation of the faulted signal is taken. Here the voltage and current signals from the hardware of the H-Bridge multi-level inverter is acquired using the data acquisition card DAQ 9225 for the voltage signal and DAQ 9227 for current signal from the NI LABView data acquiaition. Fig 5 shows the LABView block diagram for the acquisition of the voltage signal and Fig.6 shows the LABView data acquisition of the current signal.
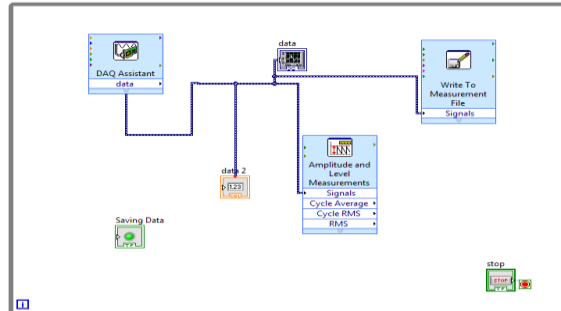
Fig 5. LABView block diagram of voltage acquisition

V. EXPERIMENTAL RESULT AND ANALYSIS

To diagnose the faults in the multi-level inverter system Fig.4 shows the experimental test has been conducted using 30V prototype system. It has an H-Bridge multi-level inverter which is fed by rectifier in the input of the inverter. In which each H-Bridge will have its own separate DC sources. Three phase H-Bridge multilevel inverter is been implemented here in the hardware. The Renesas processor used for producing the gate pulses to the MOSFET switches. These values of the signals are taken and the time period of the fault is extracted and the fault time is measured by using this feature of the signal and it is analyzed. In following sections the output voltage of the multi-level inverter during the healthy condition and the fault conditions has been discussed.

A.   Output voltage of the multi-level inverter during healthy condition

Fig 7. Shows the output single phase to neutral voltage of the H-Bridge multi-level inverter during healthy condition without any faults in the multi-level inverter.
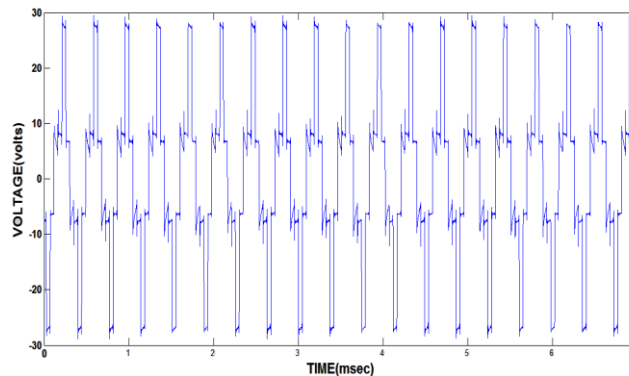

Fig 7. Voltage Output of the Multi Level Inverter during Healthy Condition

B.   *Current output of the multi-level inverter during healthy condition*

Fig 8. Shows the output current of the H-Bridge mu;ti-level inverter during healthy condition. the current was measured through a shunt resistane.
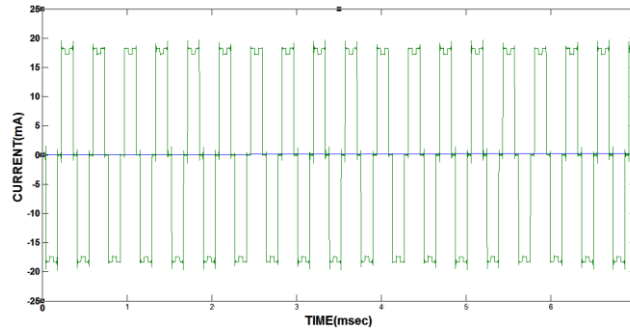

Fig 8. Current output of the multi-level inverter during healthy condition

C.   *Voltage output of the multi-level inverter during one H-Bridge open fault*

The output voltage of one H-Bridge open failure fault is shown in the Fig 9. When there is a failure in the gate pulse of the multi-level inverter the output voltage will have some distortions in their values which are as shown in the waveform below.
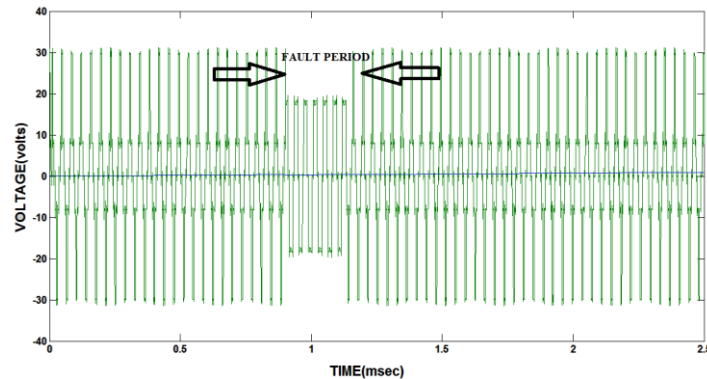

Fig 9. Voltage Output of the Multi Level Inverter during Gate Pulse Failure

The gate pulse failure is made by opening a manual switch across the H-Bridge of any phase. At steady state operation of the inverter the switch is open and there occurs a distortion in the value of the current and voltage which is denoted as fault period in the above Fig 5.The open circuit fault is created at 1msec and cleared at 1.2msec. during this period the output voltage magnitude is reduced to 20vlts and a level in the output voltage is also reduced as shown in the Fig 9.

D.   *Feature extraction system*

The discrete wavelet transforms is used for the feature extraction system. The time and frequency feature of the output current signal of the multi-level inverter during the fault condition is been extracted and the fault values of time and frequency is been known from the extracted feature of the discrete wavelet transforms. The DAQ 9225 voltage acquisition card will read the voltage level upto 300 rms and the current acquisition card DAQ9227 will read upto the level of 5Amps directly from the hardware. The data sent to the computer is loaded in a excel sheet and again it is copied to the matlab file which is used for the feature extraction system. A matlab program is used for the feature extraction system which gives the standard deviation of the signal used for the analyzing the faulted signal.

1. The extracted feature of the output current of the multi level inverter during healthy condition is shown in the Fig 10. The distortion ratio of this normal voltage is 148.58%.
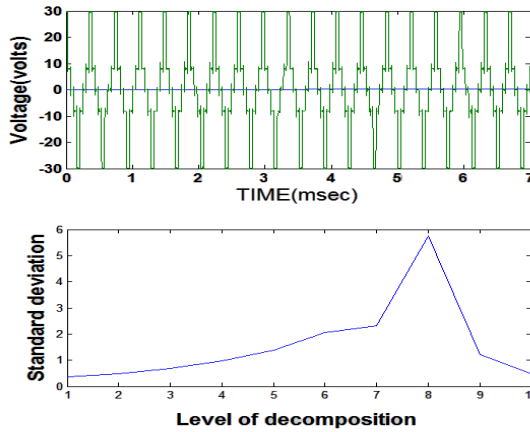
Fig 10. Standard Deviation of the Voltage Signal during Healthy Condition

2. The extracted time and frequency feature using wavelet packet transforms during gate pulse failure is shown in the Fig 8. The level of distortion ratio during the one H-Bridge open circuit fault is about 239.86%. The standard deviation value at fundamental frequency is increased up to 10 as shown below in Fig 11.
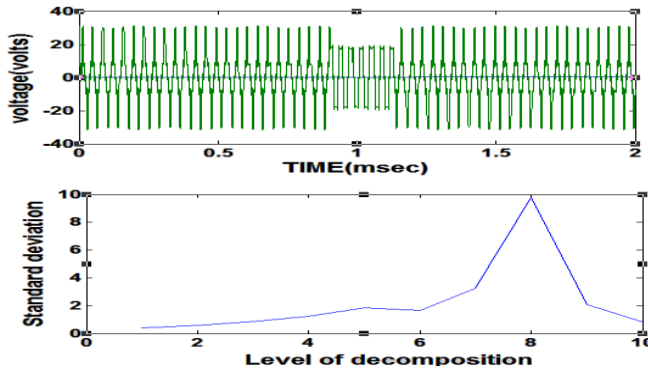

Fig 11.Maximum, Mean, And Standard Deviation of the voltage Signal during one H-Bridge open Failure

The time and frequency features are extracted in the MATLAB using the mat file program in the command window which is used find the fault values of the time and frequency of output current of multi-level inverter. This is used to analyze the fault of the multi-level inverter.

The distortion ratio of the feature is calculated by,

$$\%DR = std(D3) + std(D4)+std(D5) / std(D8) *100 \qquad (9)$$

VI. CONCLUSION

A H-Bridge multi-level inverter can be used for the medium power applications and high voltage system interconnections. A fault diagnosis method is been implemented in the H-Bridge multi level inverter. The considered for the proposed system is the H-Bridge opening fault. A manual connector pin is used to create the faults of the multi-level inverter. For this fault there will be a change in the output voltage and current of the multi-level inverter. The output voltage and current signals of the multi-level inverter is been extracted using the discrete wavelet transforms and the analysis is made in the proposed work. The discrete wavelet transforms separates the signals in to approximations and details by the use of high pass and low pass filters. The mean, maximum, and the standard deviation values of the voltage and current signals have been taken and analyzed. In future work these values will be given to the neural network and it is trained for

the kind of faults and the corresponding gate pulse is changed to balance the output voltage of the multi-level inverter. Thus the faults in the multi-level inverter is been analyzed using the wavelet packet transforms.

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BIOGRAPHY

V.Vinothkumar was born in India, in the year 1989. He received his bachelor degree in electrical and electronics engineering from Anna University, Chennai in 2006. He worked as lecturer at Thiagarajar Polytechinic College for one year. At present he is doing his Master's degree in the Anna University, Chennai.   He published papers in two international conferences and in that one IEEE conference. His current research area is multi-level inverters and wavelet transforms. His areas of interests are power electronics and electrical machines.

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