ISSN (Online) : 2319 - 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

*Volume 3, Special Issue 3, March 2014*

2014 International Conference on Innovations in Engineering and Technology (ICIET'14)
On 21st & 22nd March Organized by

K.L.N. College of Engineering, Madurai, Tamil Nadu, India

# FPGA Based Realization of Multi-Carrier Direct Sequence CDMA for SDR Application

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***Abstract***— this paper presents the physical layer architecture of Software Defined Radio. Here Multi Carrier-Direct Sequence Code Division Multiple-Access (MC-DS-CDMA) system is used as the modulation technique to support multimedia services in mobile/wireless communication. This modulation technique is basically a combination of DS- CDMA and Orthogonal Frequency Division Multiplexing. This is combined with viterbi decoding algorithm has been reported. The challenging factors like peak power and Bit error rate of the transmitted signal is reduced with the proposed system. Two types of modulation are done. According to the Bit error rate we can change the modulation. FFT point is scalable in this Transceiver architecture. The speed of the transmission also increased,

***Keywords***— CDMA, OFDM, MC- CDMA, DS- CDMA, BPSK, QPSK, Viterbi decoder, Software Radio.

## I. INTRODUCTION

The technology Advancement in Wireless communication systems supports various multimedia services such as data processing and video processing. For this we need multi-rate transmission with large bandwidth. The next generation communication system requires fast signal processing with low error probability and low power. The main design challenges for the wireless communication systems are speed, data rate, bit error rate, power etc.

The software Defined Radio (SDR) provides the flexibility of designing all the radio functions in software on a Reconfigurable Hardware. This is collection of Hardware and software [1]. All physical layer functions like data conversion, decoding/encoding, modulation/de-modulation can be implemented on a processor like DSP (Digital Signal processor) or FPGA (Field Programmable gate array) or a GPP (General Purpose processors) so that we can change our application at any time without affecting the Hardware.

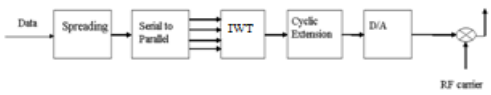
Multi-Carrier Direct-Sequence Code Division Multiple Access (MC-DS-CDMA) scheme in wireless communication system is used to support multi-carrier transmission for different users in same time. In wireless radio communication system, much attention has been taken to the MC-DS-CDMA scheme due to its own capabilities to provide higher capacity, lower bit error rate over the conventional Time Division Multiple Access (TDMA). It mainly reach the good qualities of Direct Sequence Code Division Multiple Access (MC-CDMA) and Orthogonal Frequency Division Multiple Access (OFDM) scheme.

Here, the technique combines the merits of both Multi-Carrier (MC) CDMA modulation technique and Direct-Sequence (DS) CDMA technique. MC-DS-CDMA is mainly used in communication systems (both academia and industry) due to this robustness and flexibility for future wireless network. The main challenges are the Multiple Access Interference (MAI) and select the attainable frequency diversity.

The major technique used for decoder is Viterbi decoding algorithm. Which is an optimum decoding algorithm for the convolution ally encoded digital data sequences on the additive white Gaussian noise (AWGN) channel. When the restrained length of the code is short viterbi algorithm has higher efficiency, faster speed. We have developed an own approach for our design of a MC-DS-CDMA with the viterbi decoding algorithm. By using this technique, we can effectively reduce the bit error rate of the existing system. It performs a maximum likelihood detection of data transmitted over a channel with inter symbol interference (ISI). Any type of modulation can be used here.

## II. SYSTEM ARCHITECTURE

The software radio




architecture is shown in Fig 1. In this architecture all of the physical part can be done on the FPGA. This reconfigurable architecture can reuse for any other

application in future. The reusability of the hardware will reduce the cost. All the applications of the receiver as well as transmitter can work on same hard ware so that there is reduction in area of the hardware. According to our need we can include any type of functions in SDR [2].

Now a day's more developments are done on the FPGA. The run time reconfiguration like application will help us to change the functions at run time itself without affecting the other current programs. This will give more flexibility in design. Since the newer FPGA provides PR modules, it is possible to change of the certain part of FPGA alone and hence we can avoid complete FPGA for reconfiguration.

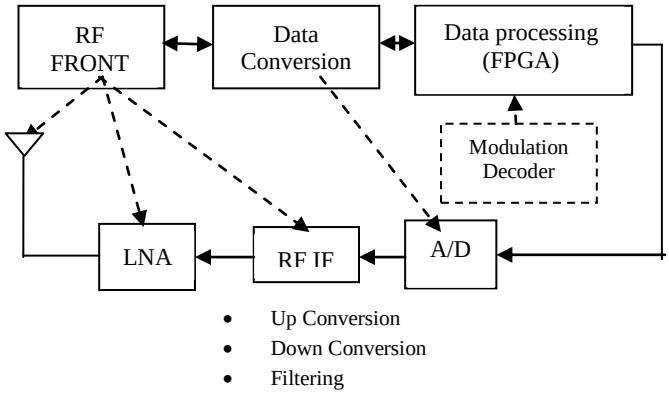



Fig 1 : SDR system Architecture

Here the messages are undergoing data conversion for upper/down conversion. The base station performs the signal processing for this we have to convert it to digital form. Technique a family of Radio products used in communication to be developed in common platform architecture. Then signal process will happening on FPGA. Then convert the processed signal into analog one for transmission. The reverse operation will done at the receiver side [3].

The proposed architecture embeds everything into a single FPGA which in turn reduces the total resource utilization and hence the power and speed. Any type of modifications and adding more features can add easily by changing the software. The partial reconfigurable FPGA can store each functions as separate BIT files [12]. The BIT files can call any time.

The static logic remains functioning and is completely unaffected by the loading of a partial bit file. The reconfigurable logic is replaced by the contents of the partial bit file. There will be a Configuration controller which is part of the static module. This takes care of loading and unloading of dynamic modules. The command to this controller will be given from PowerPC.

## III. CDMA ARCHITECTURE

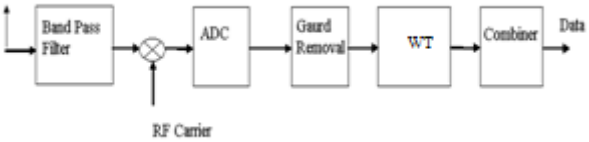
There are two types of multicarrier CDMA system which are Multicarrier Code Sequence Division Multiple Access (MC-DS-CDMA) and MC-CDMA. There is a little difference between these two systems. In former system, the data sequence multiplied by a spreading sequence and modulates with M carriers. In latter system, a spreading sequence is serial to parallel converted, and each bit of spreading sequence is modulating by a carrier frequency. The condition is that the number of carriers must be equal to the number of bits in spreading sequence [6].

Fig 2 : CDMA Transmitter
Fig 3 : CDMA Receiver

The CDMA transceiver system is shown in Fig (3) and (4). Here instead of FFT/IFFT, Walsh Transform is used. The modulation techniques are BPSK and QPSK.

### *A. WALSH TRANSFORM*

Walsh Hadamard Transform is a type of Discrete Fourier




Transform. It performs orthogonal symmetrical functions on real numbers.
This can be represented in matrix form

$$T(n) = \begin{bmatrix} T(n-1) & T(n-1) \\ T(n-1) & -T(n-1) \end{bmatrix} \quad (1)$$

and T(0) = +1

the transform can be calculated with the following equations.

$$(H_m)_{k,n} = \frac{1}{2^{\frac{m}{2}}}(-1)^{\sum_i k_i n_i} \quad (2)$$

### *B. MODULATION*

Modulation can be either BPSK or QPSK. The modulated signal representation given below

#### *1) BPSK*

The modulated BPSK signal has two changes either 1 or 0.

$$\left.\begin{aligned} S_1(t) &= \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t) \\ S_2(t) &= -\sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t) \quad 0 \le t \le T_b \end{aligned}\right\} \quad (3)$$

#### 2.1.1 QPSK

In QPSK modulation basically two sinusoidal signals are used for basic function. In this the information bits are grouped as 4 symbols of 2 bits and each symbol can select any of the values from 00, 01, 10, and 11. In one symbol period four different phase states can be used

| Phase | 0 | π/2 | π | 3π/2 |
|---|---|---|---|---|
| Symbol | 00 | 01 | 11 | 10 |

The signal can be represented as

(4)

*C. SYSTEM OVERVIEW*

Figure.4 (a) shows band limited wide band direct sequence waveform with a single carrier in frequency domain. The bandwidth (BW) of wideband system can be approximately given by

$$BW_{single} = (1+g \square 1/Tc) \quad (5)$$

Where 0<< g<<1 and Tc is the chip duration of single carrier system, we divide bandwidth of single carrier into M sub equal frequency bands and there is no overlap between each band [13].

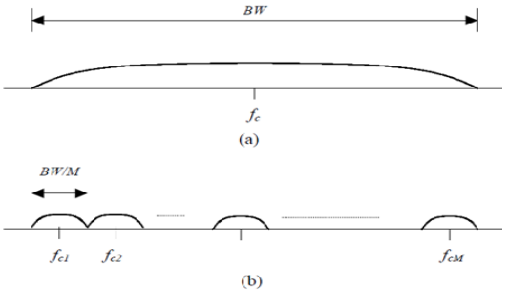



Fig 4 a) PSD of wide band single carrier direct sequence
b) PSD of wide band multi carrier direct sequence

Therefore , the bandwidth of each frequency band can be given by

$$BW_{mc} = (1+\gamma)1/MTc \quad (6)$$

It implies that the chip duration of multicarrier system should be $MT_c$ and M is the number of carriers.

*D. Simulation Model*

*1) Transmitter*

Consider the transmitter shown in Fig 5 where the random binary input sequence of $k^{th}$ user, dε{-1,1}is multiplied by a common pseudo-random spreading sequence cε{-1,1}. We assume that there are Nc chip per symbol and each user has different gold sequence [8].

We assume that all signal are transmitted with the same energy per bit chip Ec Then, the transmitted signal of kth user can be given by

$$\sum_{l=1}^{M} \sqrt{Ec} \sum_{n=-\infty}^{\infty} d_n^{(k)} c_n^{(k)} pTc(t-nTc).\cos(\omega 1t + \theta 1) \quad (7)$$

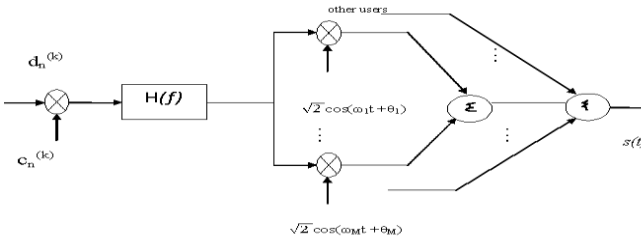



Fig 5 Block Diagram Of Multi Carrier Direct Sequence CDMA

$$S_i(t) = \sqrt{\frac{2E_s}{T}}\cos\left(2\pi f_c t + \frac{\pi}{4}(2i-1)\right) \qquad i = 1,2,3,4$$

*E. Shaping Filter*

In shaping filter, we assume that the there is no partial band interference and the message signal modulated by each carrier is transmitted over band limited channel W, Where $W \leq (f_{i+1}-f_i)/2$ and $f_i$ is the $i^{th}$ carrier frequency. Hence, the chip wave shaping filter is selected so that it satisfies the Nyquist criterion. With H(f) the transfer function of wave shaping filter.

$$H_{RCF}(f) = |H(f)|^2 \quad (8)$$

and

$$\int_{-\infty}^{\infty} |H(f)|^2 \quad df = 1 \quad (9)$$

Let $H_T(f)$ be the frequency response of transmitter filter and $H_R(f)$ be the frequency response of receiver filter. Then, the $H_T(f)$ ,$H_R(f)$ is designed as follows,

$$H_{RCF}(f) = |H_T(f)|\,|H_R(f)| \quad (10)$$

$H_{RCF}(f)$ is raised-cosine frequency characteristics which is defined as:

$$H_{RCF}(f) = \begin{cases} Tc & |f| \leq \frac{1-\propto}{2Tc} \\ \frac{Tc}{2}\left\{1 - cos\frac{\pi Tc}{\propto}(|f| - \frac{1-\propto}{2Tc})\right\} & \frac{1-\propto}{2Tc} \leq |f| \leq \frac{1-\propto}{2Tc} \\ 0 & |f\} > \frac{1\mp\propto}{2Tc} \end{cases} \quad (11)$$

Thus, the impulse response of transmitter and receiver is

$$h_T(n) = \sum_{m=-(N-1)/2}^{(N-)/2} \sqrt{H_{RCF}\left(\frac{mFs}{N}\right)} e^{j2\pi mn/N}$$

n=0,±1,…., ±N-1/2 (12)

*F. Channel Model*

In order to provide performance analysis, the channel is classified as frequency selective if the width of transmitted signal (BW) is large when compared with (Δf),

$$BW > \quad (\Delta f) \quad (13)$$

At the receiver , we would receive several copies for transmitted signal with different delays[6]. With this model, the number of resolved paths of channel, L is given by

$$L = BW/(\Delta f)+1 \quad (14)$$

Where the coherence bandwidth is related to delay spread, Tm, by

$$(\Delta f) = 1/Tm\frac{1}{(Tm)} \quad (15)$$

The channel impulse response can be modeled as in fig 5, where β is zero mean complex Gaussian random variable [7].

For multicarrier system, we are going to choose the number of carriers to achieve the following requirement,

- Each sub frequency band of multicarrier system has no selectivity, in the range i.e, Tm/(MT)<1.
- To satisfy the first condition, we need to choose γ > Tc/Tm
- All the sub frequency are subject to independent fading channel which implies that

$$BWm > (\Delta f) \quad (16)$$

$$C(t) = \lambda\delta(t) \quad (17)$$

Where, λ is the zero mean complex Gaussian random variable [8].
The MC-DS-CDMA signal can be represented as

$$S_{MD}^{j}(t) = \sum_{i=-\infty}^{\infty}\sum_{k=1}^{Nc}\sum_{m=1}^{G_{MD}} b_k^j(i)C_m^j.P_c(t-m-)\,T_c - iTs'.\cos((2\pi f0+k\Delta f')t) \quad (18)$$

*G. Receiver*

For single carrier system, the transmitted signal subjected to frequency selective and multiple transmission paths. Therefore, we employ rake receiver to improve the performance of signal [13]. Here, we have that we have perfect timing and channel estimation [14]. Rake receiver can be implemented as in figure 6

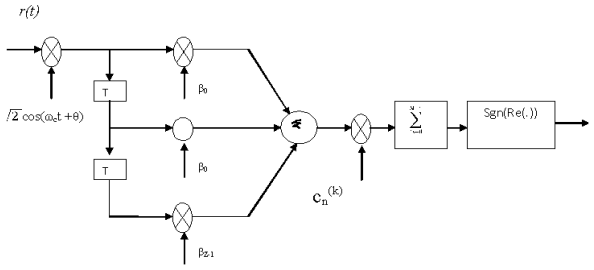



Fig. 7 Receiver System For Single Carrier

## II. VITERBI DECODER

Viterbi decoder is mainly used for encoding the convolutional data to overcome number of errors received at the input data due to channel noise [11].

*A. Convolutional Encoder*

Convolutional encoder shown in fig 7 takes input data bit and gives out two bits. Convolutional encoding is a process of adding redundancy to a signal stream. It allows variable code rates (1/2), constraint lengths (K= 3.9) and generate polynomials. To convolve the encode data, start with 2 memory registers, each holding one input bit. Registers start with a value of 0.

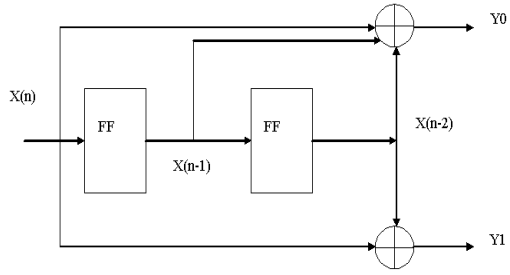



Fig. 6 Convolutional encoder

The encoder has two modulo-2 adders which are implemented with a XOR gate. It generates two bit polynomials, one of each adder.
(Y1Y0)- Encoder output bits,

X(n-1)X(n-2)- previous state of encoder,

X(n)- input bit to encoder.

We present binary (0, 1) input and the binary output sequences of an (n,n-1) convolutional encoder by

$$X(n) = [x_1^0, x_2^0, \dots., x_{n-1}^0, x_1^1, x_2^1, \dots x_{n-1,\dots}^1]$$

$$Y(n) = [c_1^0, c_2^0, \dots., c_n^0, c_1^1, c_2^1, \dots \dots., c_n^1, \dots \dots] = [C^0, C^1, \dots.] \quad (18)$$

Where $X^i$ is the (n-1) tuple of the input digits at time i, $x^i_j$ is the j the digit in the (n-1) tuple and similarly for the output sequence. The transform of the input sequence is written as (n-1) tuple

$$X(D) = [X_1(D), X_2(D), \dots X_{n-1}(D)] \quad [19]$$

Where, $X_j(D)=x_j^0 + x_j^1 D + x_j^2 D^2 + \cdots.,\ 1 \le j \le n-1$

The constraint length of the code is given by

$$H=\sum_{i=1}^{n-1} \max[degree\ g_{ij}\ (D)] \quad [20]$$

The encoder operation can now be described compactly as the vector –matrix product (modulo 2)

C(D)-X(D)G(D)

Or, equivalently,

$$Cj(D)=\sum_{i=1}^{n-1} X_i(D) g_{ij}\ (D) \quad [21]$$

The n-tuple Cj, which is the output of the encoder at time j, is fed into a modulator which produces zj, one of $2^n$ channel signals.

The channel products at the output a noisy discrete –time sequence $\{r_j\}$ where

$$r_j = z_j + n_j$$

and the $\{n_j\}$are statistically independent Gaussian random variable with zero mean and variance N/2. From $\{r_j\}$ a maximum to determine the most likely binary sequence X transmitted.

*B. Viterbi Algorithm*

A Viterbi algorithm finds the most likelihood path transition sequence in a state diagram, given a sequence of symbols. A Viterbi algorithm consists of the following three major parts [16].

*1) Branch metric calculation*: Calculations of a distance between the input pair of bits and the four possible ideal pairs (00.01,10,11) encoder.

*2) Path metric:* For every encoder state, calcilate a metric for the survivor path ending in this state ( a Survivor path is a path with the minimum metric).

*3*) *Trace back unit:*This step is necessary for hardware implementations that do not store full information for the survivor paths, but store only one bit decision every time when one survivor path is selected from the two[15].

The steps involved in the viterbi algorithm are given below,

1. Initialize the parameters
2. Branch Metric Calculation. (using Hamming Distance)
3. Load the Branch metric.
4. ACS (add and compare select)
5. Check whether the states end, if yes then go to step 6 otherwise go to step 3.
6. Check whether the trellis states end, if yes then go to step 7 otherwise go to step 2.
7. Collect the decoded bit
8. End.

### *C. Trellis Diagram*

In the trellis diagram, horizontal direction circles give the stages [13]. Vertical direction circles give ideal states and above which circles represents branch metric. Thick lines indicates encoding path for corresponding input data. T indicates times slots for each clock.

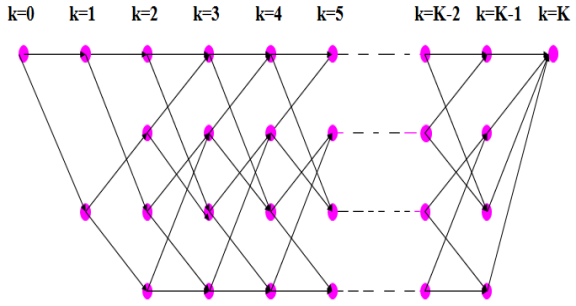



Fig. 8 Trellis Diagram

We will prove the theorem that under certain conditions the same state diagram can be used to compute the error weight distribution of a class of trellis codes. The following definitions are described below.

*Definition* 1: Let $F^p$ be a binary n-tuple given by $(e_1^p, e_2^p, \ldots\ldots, e_n^p)$. Then the squared Euclidean error weight of the encode output $C^p=(C_{1p}, C_{2p}, \ldots\ldots C_{np})$,the channel signal ,is given as

$$d^2(C^p;F^p)=\|M(C^p)-M(C^p \oplus F^p)\|^2 \qquad [22]$$

where $\|(.)\|^2$ is the squared Euclidean norm of (.).

*Definition* 2: Let B be a set of channel signals of cardinality $2^{n-1}$. The weight profile of the set B with respect to a given vector $F^p$, denoted E(B, $F^p$,W), is given as

$$E(B, F^p, W)=\sum a_n w^n \qquad [23]$$

Where, $a_n$ is the number of channel signals in the set.

## RESULTS

The simulation results for CDMA transmitter an d receiver is shown using MATLAB.Figure 10 and 11 shows the original bit sequence transmitted and received with the gold sequence

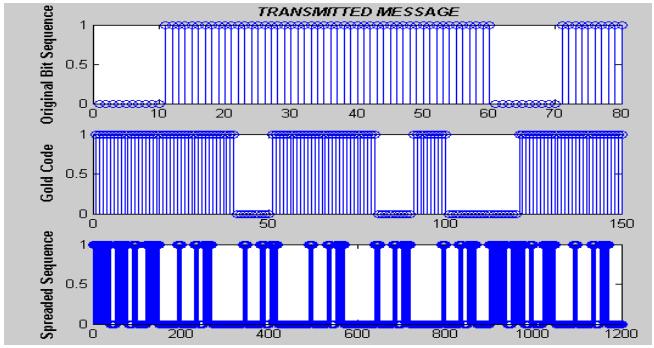



Fig. 9 CDMA Transmitted sequence

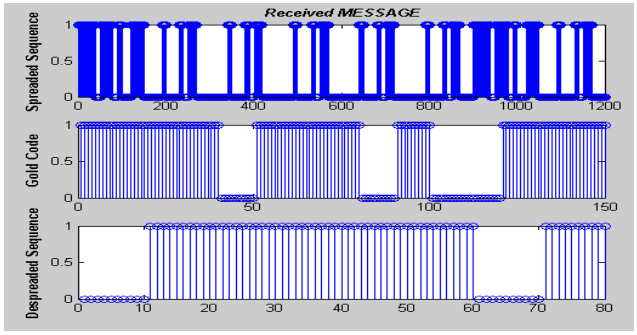



Fig. 10 CDMA Received sequence

Fig 11 and 12 shows the performance of BER over the multiple users. The first figure shows the performance without Viterbi algorithm and the second figure shows the BER with Viterbi algorithm.

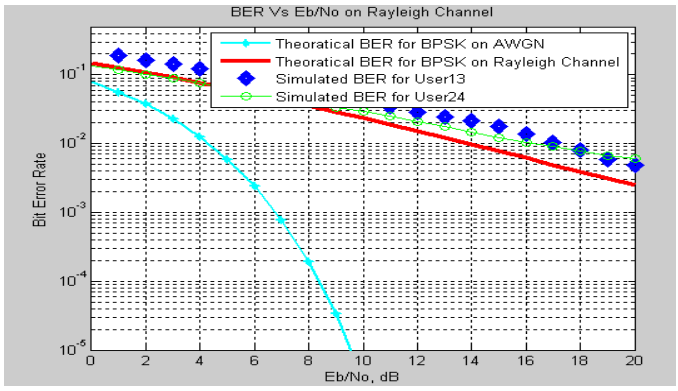



Fig. 11 BER Vs No of users (mc-ds-cdma)

This proposed MC DS CDMA with Viterbi algorithm method reduces the BER effectively.

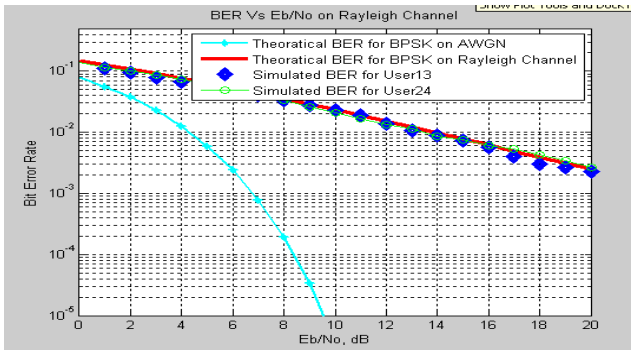



Fig.. 12 BER Vs No of users (Viterbi Decoder)

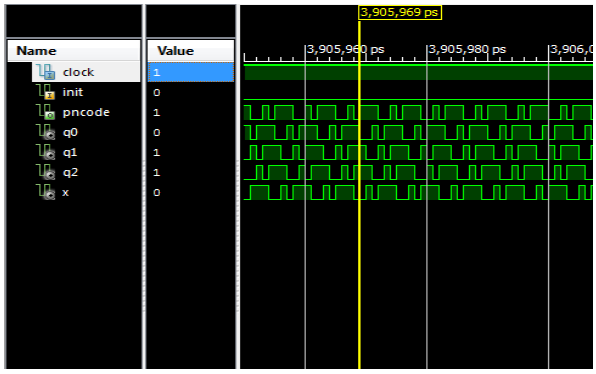



Fig.13 Transmitter

Fig (13) – (16) represents the simulation results of CDMA using Xilinx. The fig (13) and (15) represents the transmitted and received information. The other figures gives the RTL view of the design.

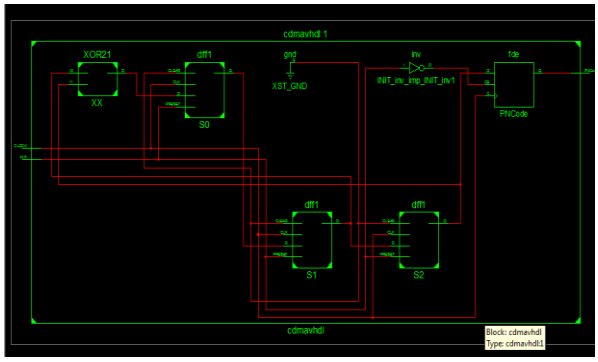



Fig. 14 RTL view of Transmitter

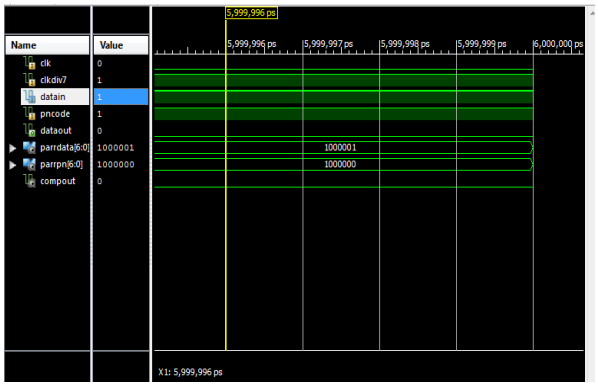



Fig. 15 Reciever

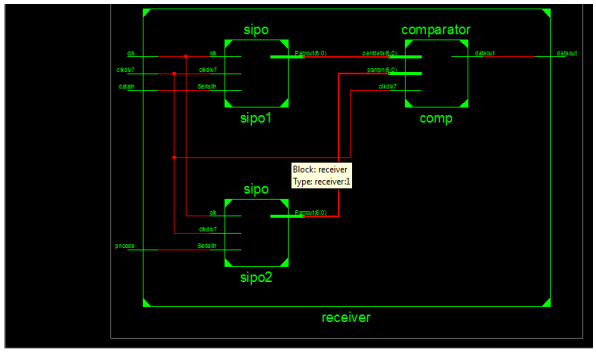



Fig. 16 RTL view

In figure 17 the BER comparison of CDMA with BPSK and QPSK modulation.

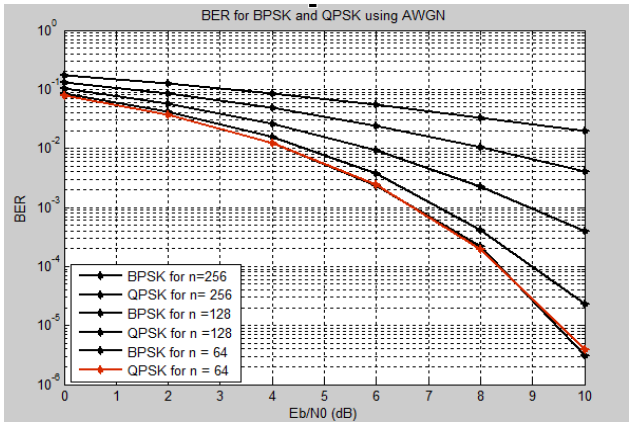



Fig. 17 Comparison of BER for QPSK and BPSK

TABLE I
DEVICE UTILIZATION

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 70 | 960 | 7% |
| Number of Slice Flip Flops | 90 | 1920 | 4% |
| Number of 4 input LUTs | 119 | 1920 | 6% |
| Number of bonded IOBs | 5 | 66 | 7% |
| Number of GCLKs | 1 | 24 | 4% |

## CONCLUSION

From the comparison results with various CDMA, it is clear that both MC-DS-CDMA and viterbi decoder schemes have better performance than the previous one. The BER performance of MC-DS-CDMA system under the viterbi decoder has been analyzed in the presence of AWGN channel and multi-path Rayleigh fading channel. Here the transmission through AWGN channel will give better result than Rayleigh channel. Due to this advantages Multi-carrier Direct sequence CDMA can be

used in 4G wireless communication and next Generation communication systems with SDR.

MC-DS-CDMA should deliver bit rates of 100Mbits/s for slow-moving terminals and 10Mbits/s in a TGV high-speed train travelling at 300kph. The Viterbi decoding algorithm gives better and fast performance comparing with other decoders.

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