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FPGA-Based Bit Error Rate Performance measuring of Wireless Systems

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ABSTRACT: The bit error ratio (also BER) is the number of bit errors divided by the total number of transferred bits during a studied time interval. The proposed BER tester (BERT) integrates fundamental baseband signal processing modules of a typical wireless communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator onto a single FPGA to provide an accelerated and repeatable test environment. Using a developed graphical user interface, the error rate performance of single- and multiple-antenna systems over a wide range of parameters can be rapidly evaluated. The FPGA-based BERT should reduce the need for time-consuming software based simulations, hence increasing the productivity. The BERT modules were developed using device-independent HDL, and no specific features of the FPGAs, such as built-in soft processors, were utilized. Therefore, the system is portable and can easily be synthesized onto larger and faster new FPGAs for the rapid prototyping of increasingly complex emerging wireless communication systems. FPGA solutions offer significant cost reduction compared to commercially available solutions.

KEYWORDS: Bit-error rate tester (BERT), field-programmable gate array (FPGA),fading channel simulation, Gaussian noise generator (GNG), Baseband performance validation

I. INTRODUCTION

World is moving very fast, and every day, there will be new deployments willo ccur no one have idea. What will be the next technology will emerge in the field of wireless communication, if we go back to our passed there was only one way of a medium to people connect to each other is post Letter.Now a days world moving towards on fourth generation of wireless The pace of wireless system development using the latest communication techniques is increasingly limited by the design productivity. It is critical to verify the design characteristics at the earliest possible stage of design (e.g., at the baseband level) to minimize costly design iterations. At the physical (PHY) layer, the bit error rate (BER) performance metric is widely used to measure the reliability of the communication systems. Because BER properties are not in general amenable to analysis, Monte Carlo (MC) simulation techniques have been widely used to generate BER versus a range of expected signal-to-noise ratio (SNR) conditions. However, the execution times of software-based MC simulations of the baseband layer on workstations can be extremely long, especially for increasingly complex communication systems. This is mainly because:

1) Many modern techniques, such as multiple-input– multiple-output (MIMO) systems, rely on computationally intensive signal processing at the receiver. Therefore, bit-true software-based simulation of these algorithms on workstations is becoming prohibitively time consuming. In addition, for a communication system specification with a set of target system requirements such as data throughput, received power, available bandwidth, noise statistics, and a target error performance, there are typically various potential solutions. Each solution can use a different combination of subsystem designs with different sets of input parameters. Exploring the design space to achieve an optimized overall system solution that meets the target specifications can involve a large number of options. To estimate the BER performance of a communication system with the MC simulation method, we have to measure the BER over a large number of independent problem instances . While simulation of digital communication systems under additive white

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Gaussian noise (AWGN) channels is straightforward as the system performance is averaged over a large number of independent instances of noise and data, BER performance measurement of wireless systems over time-varying fading channels requires significantly longer simulation times because of the dependence between the channel instances. To accurately estimate the BER performance of a communication system over a time-varying fading channel, the error performance needs to be averaged not only on independent instances of noise and data, but also on the fading channel samples over a long period. Such a performance evaluation can require several weeks or months of software simulations. Hardware simulators can accelerate the performance evaluation of communication systems compared with software simulators by several orders of magnitude. This makes hardware-accelerated prototyping and validation of the PHY layer as an increasingly attractive alternative. Published hardware-based baseband BER measurement systems use field-programmable gate arrays (FPGAs) and use model-based systems such as Simulink to integrate parameterizable IP blocks (such as conventional cores for forward error correction) onto an FPGA. While using system level tools can eliminate the need for extensive hardware knowledge and will usually shorten the design time, a simulation library may include only a set of basic digital communication components and might not include modules, such as new coding algorithms, for emerging technologies. Thus, designers will still need to implement various communication modules with compatible interfaces with other components. In addition, most of the published BER testers (BERTs) verify the performance under the linear AWGN channel which is a rather inadequate model for wireless mobile communication systems. Fading channel models for mobile communication systems must reproduce the statistical properties of radio propagation environments. Furthermore, although several accurate Gaussian noise generators (GNGs) have been reported over the last few years, published BERTs use a noise generator that has a relatively poor accuracy.

II. RELATED WORK

1) "Hardware-based error rate testing of digital baseband communication systems" by A. Alimohammad, S. F. Fard in the year 2008

They present a flexible architecture for evaluating the bit-error-rate (BER) performance of prototype digital baseband communication systems. The proposed BER tester uses an accurate fading channel model and a Gaussian noise generator to provide a realistic and repeatable test environment in the laboratory. This evaluation environment should reduce the need for time consuming field tests, hence reducing the time-to market and increasing productivity. Using an efficient elastic buffer interface, an arbitrary baseband module can be added to the cascaded architecture of a digital baseband communication system, independent of the module's operating rate, its position in the cascade structure, and its latency.

[2] "OSNR Monitoring for RZ-DQPSK S/m Using Half-Symbol Delay-Tap Sampling Technique" by F. N. Khan, Alan Pak Tao Lau, Zhaohui Li in the year 2010

The proposed and experimentally demonstrated an asynchronous half-symbol delay-tap sampling technique for in-band optical signal-to-noise ratio (OSNR) monitoring in 38- Gb/s return to-zero differential quadrature phaseshift-keying systems. A monitoring range of 11–23 dB has been demonstrated experimentally. Furthermore, the proposed technique also extends the range of calibration-based OSNR monitoring techniques to 5–34 dB. The proposed technique enables simple analytical models for the statistics of a signal pulse which avoids system calibration prior to OSNR monitoring.

[3]"BER Estimation for Performance Monitoring in High-Speed Digital Optical Signals" by Ernesto Ciaramella, Andrea Peracchi, Luca Banchi, Raffaele in the year 2012

Here paper presents a technique that allows easy and accurate estimation of the system bit error rate (BER) by collecting the statistical distribution of the receiver analogsamples, i.e., before decision. The scheme performance is confirmed by both numerical simulations and experimental measurements. In all cases, the estimated BER is found to be very close to the real value, thus providing accurate and robust estimations. It is experimentally verified that in presence of strong inter symbol interference (ISI), or in the highly nonlinear regime, our technique works much better than the well known -factor approach. It could be used to implement effective optical performance monitoring in real systems, with limited hardware complexity.

[4] "FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems" by A. Alimohammad, S. F. Fard in the year 2014

This paper presents the bit error rate (BER) performance validation of digital baseband communication systems on a field-programmable gate array (FPGA). The proposed BER tester (BERT) integrates fundamental baseband signal

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processing modules of a typical wireless communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator onto a single FPGA to provide an accelerated and repeatable test environment in a laboratory setting. Using a developed graphical user interface, the error rate performance of single- and multiple-antenna systems over a wide range of parameters can be rapidly evaluated. The FPGA-based BERT should reduce the need for time-consuming software based simulations, hence increasing the productivity. This FPGA-based solution is significantly more cost effective than conventional performance measurements made using expensive commercially available test equipment and channel simulators.

III . BLOCK DIAGRAM

To demonstrate our methodology, we developed a parameterizable hardware-based baseband BERT for multiple-antenna communication systems. To generate BER versus SNR characteristics using MC simulation, a pseudo-random number generator (PRNG) generates a sequence of uniformly-distributed random bits. The generated bit stream is then passed through various signal processing modules at the transmitter, then faded by the radio channel coefficients and corrupted further by the AWGN. A sequence of baseband signal processing modules at the receiver recovers the transmitted bits from the noisy received symbols. It is important to note that since fading channel coefficients are correlated in time, the BER performance measurements need to be averaged not only over independent instances of AWGN samples and transmitted bits, but also over the fading channel samples. Therefore, to accurately estimate the BER performance of a wireless communication system over a time-varying fading channel, a relatively large number of random bits and noise samples must be generated and the BER for every value of SNR can then be estimated based on a combination of different criteria, including the number of transmitted bits, the number of accumulated errors, and the transmission time. the block diagram of the implemented baseband BER performance measurement system. In the MIMO transmitter block, source bits, generated by a PRNG, are encoded using an extended binary (24, 12) Golay channel code, interleaved with a length–16383 interleaver, and modulated using 4-quadrature amplitude modulated (QAM) symbols.

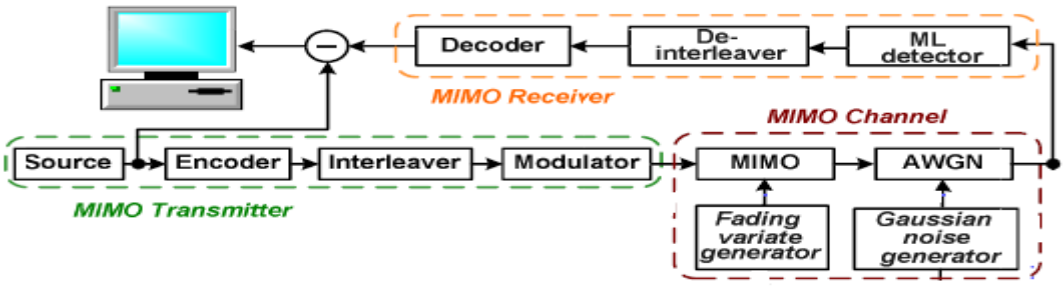

Figure 1. BERT System

Channel coding is applied to the data bits to improve system performance and robustness in the presence of channel impairments. Typically, the fading channel response changes much slower than the data signal. Therefore, the effects of a deep fade can last over a relatively long sequence of data samples, which can result in a burst of errors. Interleaving the data samples before transmission causes bursts of errors arising in the channel to be broken up by the de-interleaver in the receiver. The resulting isolated bit errors can then be more readily detected and corrected by the error correction decoder. The interleaved bits are modulated and passed through the MIMO channel where they are attenuated by the multipath fading and corrupted with AWGN . In the receiver, a maximum likelihood (ML) detector estimates the transmitted bits. After ML detection, the bit stream is de-interleaved, decoded for the extended Golay code, and compared to the transmitted bit stream. At the receiver, we used another instance of the same PRNG employed at the transmitter with the same initial seed values to generate the same sequence of random bits.

IV . HARDWARE IMPLEMENTATION

The parameterizable BERT enables the designers to verify and optimize the transmitter and the receiver algorithms under a wide variety of system parameters such as channel conditions, noise models, modulations, and coding schemes.

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We developed a GUI through which the BERT can be easily configured for different test scenarios. For example, we can vary the SNR and set the spatial correlation parameters of the analytical MIMO fading channel models. The BERT supports different sample rates and modulation schemes. The program can be configured to stop the simulation based on a combination of different criteria including the number of transmitted bits, number of errors, and transmission time. We can also compare different signal processing algorithms to quantify the BER performance versus system resource tradeoffs. The measured BER performance is exported to MATLAB for graphical display.

V. EXPERIMENTAL RESULTS

Device utilization summary:

Selected Device : 3s50atq144-4

Number of Slices:	92	out of	704	13%
Number of Slice Flip Flops:	96	out of	1408	6%
Number of 4 input LUTs:	166	out of	1408	11%
Number used as logic:	158			
Number used as Shift registers:	8			
Number of IOs:	13			
Number of bonded IOBs:	13	out of	108	12%
Number of GCLKs:	2	out of	24	8%

OUTPUT:

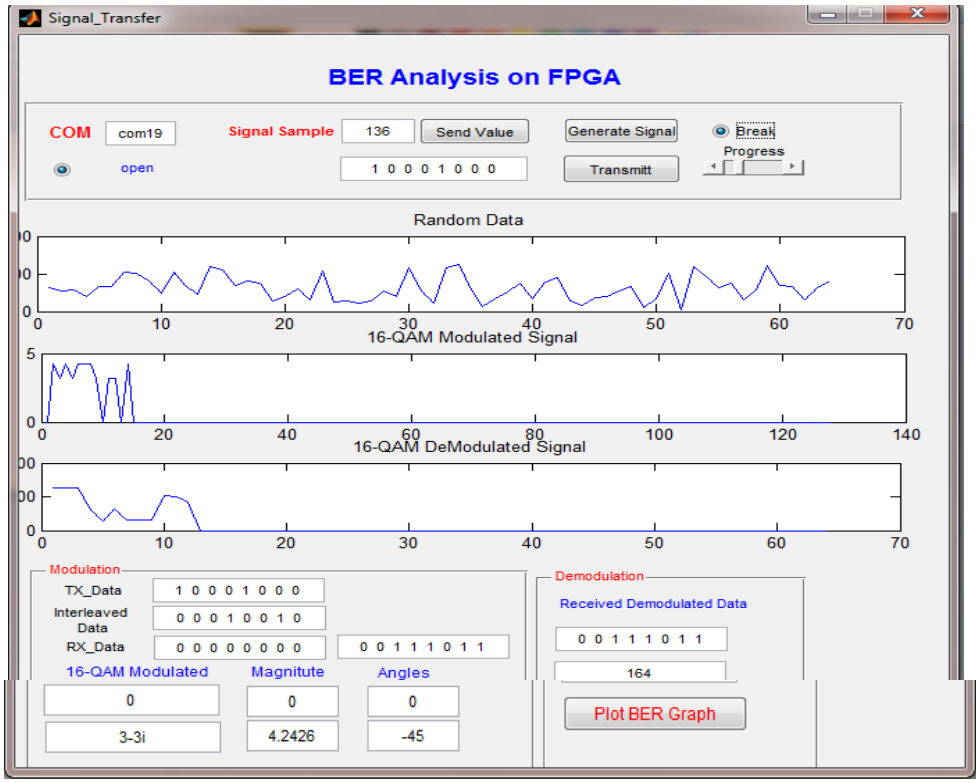

Figure 2: Output of BER

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The output of BERT system is shown in fig.2. The BER analysis on FPGA is done with Spartan 3A.We use the MATLAB software to perform the analysis . Initially we connect to the Com port then give signal sample and send it for processing.. Secondly we transmit the signal value to the interleaver .Then this data get distributed in 4 MSB and 4 LSB. Again 4 MSB bits get modulated into 8 bits. Similarly 4 LSB bits into 8 bits by using 16 QAM method.16 QAM signal get deinterleaved ,demodulate and receive the original data.

BER vs SNR Graph:

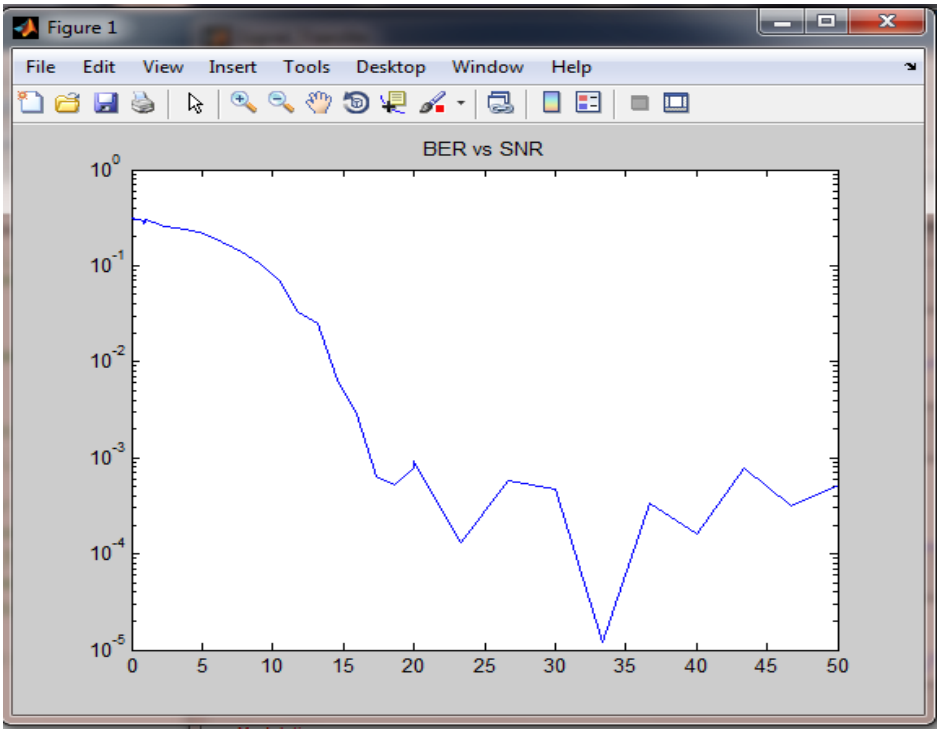

Figure 3..BER performance of a 2×2 coded MIMO system measured using the FPGA-based BERT

To estimate each BER point at each SNR, we measured the performance of signal transmission on the hardware platform. We can verify that the hardware generated BER results accurately match the computer generated BER performance.

VI .CONCLUSION

An FPGA-based BER testing scheme is presented. The scheme can measure the BER performance of a wide range of digital communication systems. Compared with traditional software simulations, the proposed BER testing scheme is a few orders of magnitude faster. Compared with traditional standalone BERT and ATE equipment, the proposed solution is much cheaper. It is also easy to set up for BER testing under different noise conditions as a novel implementation of an AWGN communication channel emulator is included in this scheme. In addition, FPGA-based solution makes it easy to interface. To achieve BER of 0.001 we require 14 to 15 dB SNR

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