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Future Transistor For Hand-Held Devices

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ABSTRACT—This paper highlights the challenges for Semiconductors Professionals and consequently gives the solutions. In this, different technologies have been compared and come up with some solutions. Main responsible parameters for a device performance i.e. drain-induced barrier lowering (DIBL) and short channel effect (SCE) has also been discussed analytically .After focusing on handheld devices it ends up with an answer that UTBB FDSOI technology has become mainstream within industries, with the purpose to serve a wide spectrum of mobile multimedia product.Ultralow-power electronics will expand the technological capability of handheld and wireless devices by dramatically improving battery life and portability

KEYWORDS—Ultra Thin Body and BOX, Hand-held devices, Transistor, Low power.

I. INTRODUCTION

Due to growing intensity of short-channel effects (SCE), the scaling down of transistor dimensions turned out to be less and less productive in driving CMOS performance [1]. Ultralow-power (ULP) transistors are an enabling technology for many proposed applications [2].Therefore manufacturers introduce Strain silicon technology to boost mobility and performance.After the continuous devolvement of technology there comes two facts into picture which drastically reduce device performance.Leakage was one of those, and variability another.If doping concentration is increased then leakage reduces but variability increases. As a solution silicon dioxide is replaced by high-k dielectric and poly-silicon gate is replaced by metal gate. This was the ultimate solution for leakage and variability [3]. Nowadays, going to the 20nm node – and even already at28nm – conventional planar transistors become unable to offer optimal performance without draining your battery or raising the temperature of your smartphone beyond safe limits. The conventional CMOS on Bulk silicon is highly inefficient to meet the demands of Smart Mobile Devices, mainly because of short channel effects that more and more impact the speed increase at each subsequent technology node [4]. Therefore, competition with CMOS in the field of smallness does not seem to be an easy case. In addition, regarding power dissipation and switching frequency, the scaling used to look consistent and successful, and it is used to ensure constancy in power and an impressive progress in frequency. Indeed, if we apply the rules of scaling[5].

Nowadays industrial focus is on fully depleted transistor to continue the technology roadmap. This trend of continuous scaling down leads to two problems and those are variability and leakage. Now we are bound to change the geometrical structure of device. In this way we got two solutions, one is UTBB FDSOI and another is FinFET. We have studied and analyzed both the solutions thoroughly. A true competition is going on between these two and it is really tough to say which is better than other.

II. THE QUEST OF TRANSISTOR FOR HAND HELD DEVICES

First, MOSFET scalability is often monitored with the intensity of drain-induced barrierlowering (DIBL). Both DIBL and short channel effect (SCE) is given by approximately same expression,making it easy to understand why FinFET and UTBB SOI show better scalability [1], as shown in Fig. 1.

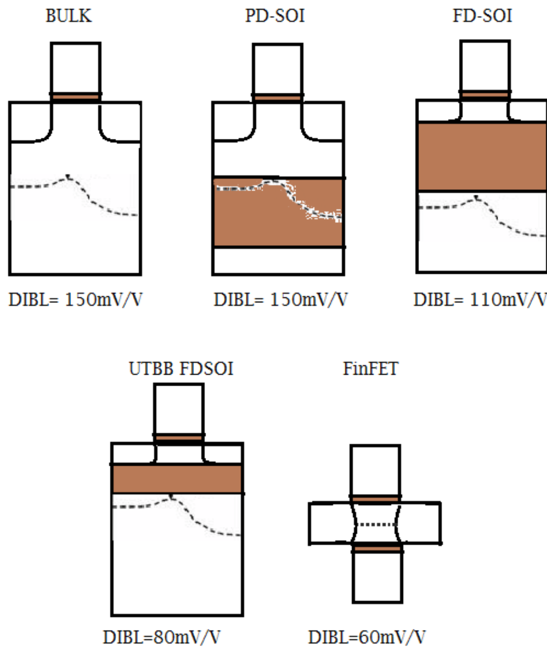

Fig. 1.Electrostatics of different transistor structures

Indeed, the quasi-constancy of oxide thickness (T_{ox}) and supply voltage (V_{dd}) , as well asthe insufficient scaling ofjunction depth(X_j) and depth of depletion layer (T_{dep}, shown by dotted line) , lead all together tonot only a non-scalability but also to a clear augmentationof the SCE and DIBL.

$$DIBL = 0.80 \frac{\varepsilon_s}{\varepsilon_{ox}} EI \times V_{ds} \quad (1)$$

$$SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} EI \times \phi_d \quad (2)$$

In this ε_s is the permittivity of silicon which has a relative permittivity of 11.68 and ε_{ox} is the permittivity of oxide which has a relative permittivity value is equal to 3.9.

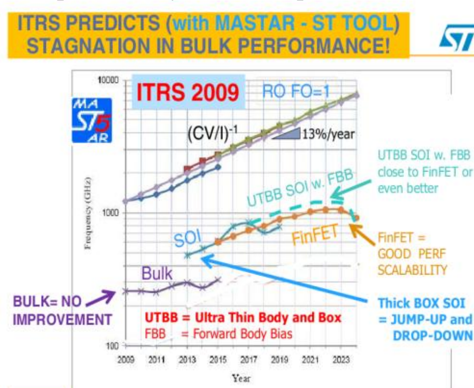

Fig. 2. Frequency versus year curve on the basis of ITRS for UTBB FDSOI. Courtesy-ST Microelectronics.

This curve (Fig. 2) shows the clear frequency compatibility with year and it is clearly observed that UTBB FDSOI is always better in this particular performance as compare to FinFET. Fully depleted transistors can be either planar or tri-dimensional. In the tri-dimensional (FinFET orTriGate), the gate wraps around the sides of a vertical silicon'fin'. In the planar, thin film transistors are fabricated inan ultra-thin layer of silicon over a buried oxide (BOX). Being a natural evolution of the conventional planar Bulktechnology, STMicroelectronics has chosen the 2D planarfully depleted silicon-on-insulator as mainstream CMOS technology [6]. An industrial solution is currently deployed at28nm with the aim to get a boost in speed and powerimprovement before the 20nm bulk technology arrival [2]. Recently this fact came into picture that 28nm FD SOI ARM based chip operated at 3GHz which is fastest, reported yet [7].

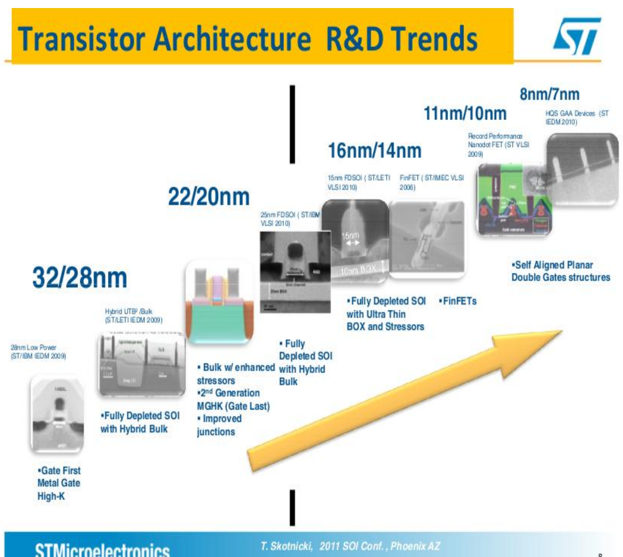

Fig. 3. Prediction of scale down of transistor by ST Microelectronics for UTBB FDSOI transistor.

According to ITRS the technology is scaling down year by year and presently people are working on mainly on 22nm/20nm technology. Year 2013 was full of research on 32nm/28nm technology. Here in fig. 3, it is shown the prediction of ST microelectronics for various technology nodes. It also provides the performance data of the device. Main challenge before us is to achieve 16/14nm technology node. Many electrostatics effects come into picture at this stage [8].

III. Performance for VLSI Design

TABLE I. Device break-down for UTBB FDSOI

Device Type	*SOI part*	*Bulk part*
MOSFET	All transistors	-
SRAM	All bit cells	-
OTP Capacitance	OTP cell	-
Resistors	P+ Poly	N+ diffusion/N well
Diode suite	-	N+/P well & P+/ N well

To be compliant with already existing design developed inbulk technology, a hybrid solution has been introducedenabling the co-integration of bulk and SOI devices on thesame die. 28nm UTBB FDSOI CMOS transistors are fabricated in a7nm thin layer of silicon sitting over a 25nm buried oxide (BOX) [3]. The process is comparatively simple withrespect to FinFET and even conventional bulk technologies. TheUTBB FD-SOI has been plugged on the basis of the 28LPBulk HKMG process from ISDA.

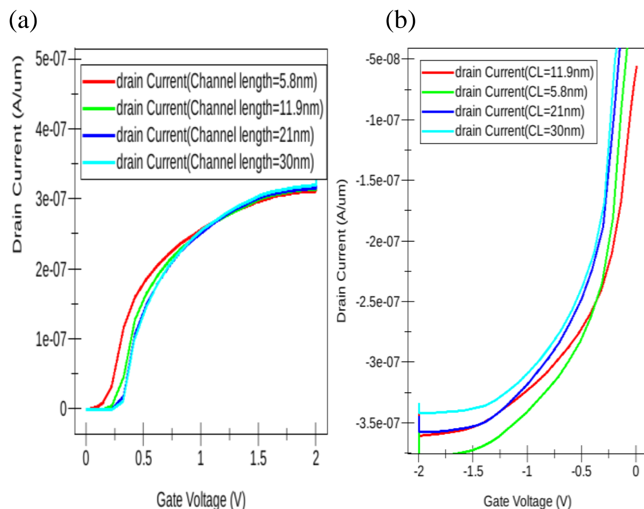

Fig. 4. Drain current versus Gate Voltage characteristics of (a) NMOS and (b) PMOS at Vdd=0.5V and BOX=10nm for various channel lengths.

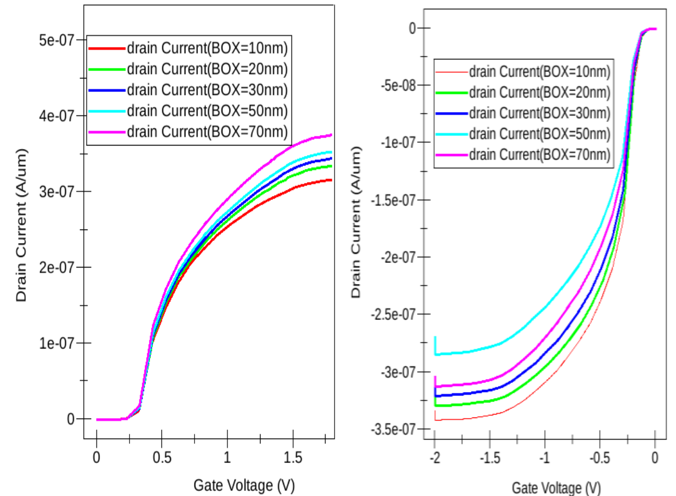

Fig. 5. Drain current versus Gate Voltage characteristics of (a) NMOS and (b) PMOS at Vdd=0.5V and Channel length=30nm for various boxes.

Drain current versus Gate voltage curves are shown in fig. 4. (a) and (b) respectively. These are obtained by the simulation on TCAD. Fig. 6,shows the proposed structure for CMOS in UTBB FDSOI technology. It has metal gate with work-function 4.71 and the thickness of BOX is considered to be 10nm while the silicon film is of 7nm thickness. $HfO_2$is

TABLE II. Multi Threshold voltage stratergy

NMOSFET

Vb	*0V*	*VDD*
n-BP	SVT(i)	LVT
p-BP	HVT	SVT(ii)
w/o BP	STV(iii)	STV(iii)

PMOSFET

VBS	0V	VDD
n-BP	SVT(i)	LVT
p-BP	HVT	SVT(ii)
w/o BP	STV(iii)	STV(iii)

used for isolation instead of silicon dioxide. In this channel is keptundoped for fully depletion technique. Shallow Trench Isolation (STI) is used for isolation between the transistor. In this Source/Drain doping is$1x10^{15}/cm^3$ and well doping is $2x10^{18}/cm^3$ while the substrate is doped with $2x10^{15}/cm^3$. In this technology our main aim is to get multi Vt by the variation in well doping and potential as per the shown in Table II.

Results have been simulated for various BOXs and gate lengths. Fig4 and Fig5 explain the drain current with respect to gate voltage of NMOS as well PMOS at various channel lengths and boxes respectively. As the magnitude of BOX is increasing, simultaneously on-state current will also keep on increasing. Therefore it can be concluded that for bigger BOX more on-state current will be obtained. .

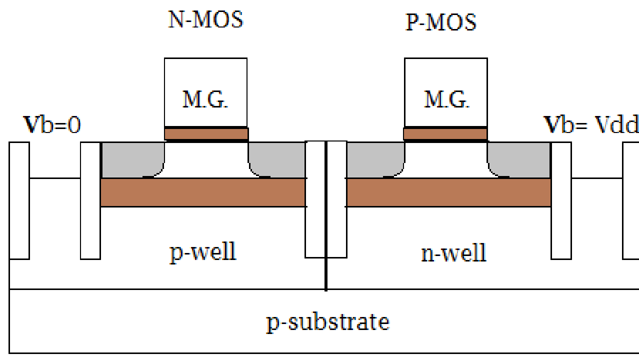

Fig. 6.Schematic for the proposed UTBB FDSOI CMOS with Well arrangement for getting multi threshold voltage.

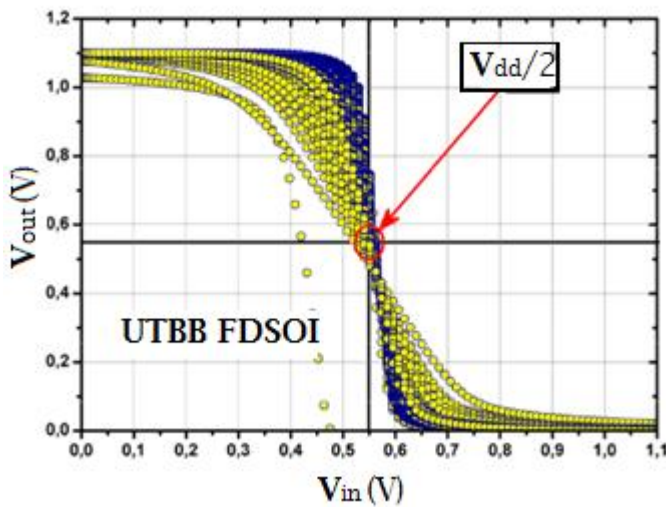

Fig. 7.VTC for UTBB FDSOI CMOS Inverter.

VTC is also simulated for various BOXs and various channel lengths. Blue portion has been obtained for various BOXs and yellow portion is for various channel lengths. It is following the conventional voltage transfer characteristics (VTC) and the obtained slope is steep which is desirable.

IV. CONCLUSION

It has been shown clearly that as per the performance and future prospects UTBB FDSOI technology has more to do for hand held devices. At this time we have challenge to reduce dissipation power of hand-held device so that its battery can go longer and here is the solution in the form of multi threshold voltage in a single transistor. It can be easily obtained by biasing arrangement. Although, initially it was very tough to decide between FinFETs and UTBB FDSOI but in case of low power devices, UTBB FDSOI is always preferred one due to its multi threshold voltage concept.

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