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Gate Capacitance Extraction Two Dimensional T- Shaped Junction less Transistor Using Sentaurus TCAD

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Abstract — The junctionless transistor is one of the device structures which found tremendous potential in terms of reduction of short channel effects, scaling factors, capacitance & fabrication. In this paper we observed an improved gate capacitance (C_{gg}) in depletion and inversion regions of a T-shape double gate junctionless transistor with comparison to the single gate junctionless transistor for oxide thickness (t_{ox}), different doping concentration (N_D) and Gate lengths (Lg).

Keywords — Junctionless transistor, gate capacitance, doping concentration, Gate length.

I . INTRODUCTION

As the semiconductor industry approaches the limits of the traditional silicon CMOS scaling, the implementation windows of certain performance boosters, such as high mobility channel materials and novel structures, have been opened in the near future. In this dissertation, the properties and feasibility of the proposed Junctionless transistor (JNT) have been evaluated for Silicon channels The conventional MOSFET extended its performance margin. The Scaling of gate length to sub 20 nm in MOSFET is unable to control the short channel effect (SCE) .The MOSFET are suppressed by FinFET, Tiple gate and Gate All around (GAA) transistors, but the fabrication is difficult due to the presence of junction between source and drain [1-3]. The junctionless transistor consist of n+(or p+ for a p- channel device) homogeneously doped silicon nanowire, i.e., an n+ source n+ channel and n+ drain(or p+ source p+ channel p+ drain) for the p channel device as gate electrode The junctionless transistor in (Fig.1) shows a uniformly doped source, drain and channel. It turned ON in flat band voltage and turns OFF when fully depleted. The channel region in JLT is to be thin for low leakage currents to be turned off. The current between the source and drain flow through the centre of the bulk channel not at the surface. In depletion region the electric field is high but no current flows due to presence of holes in the region. Now with increasing gate voltage the electrons is increased and the device is neutral [4].The fabrication of JLT is simple then MOSFET [5]. Recently J.P. Colinge *et al* in [6] shown that the capacitance is low in junctionless transistor because the channel is present at the middle and the capacitances is observed in low power junctionless MOSFERT[7]. In this paper gate capacitance (*Cgg*) for different oxide thickness and channel thickness is obtained and is also compared to single gate and double gate JLT for lightly doping and heavily doping body.

II . DEVICE STRUCTURE AND SIMULATION

The simulation of the device is performed on Synopsys Sentaurus TCAD. Both Gate capacitances (Cgg) in single and double gate N - type junctionless MOSFET are simulated. We have obtained the result for single gate, double gate JLT for different gate lengths such as 1nm, 5nm, 10nm and 19nm and oxide thickness such as 1nm. The shape of the gate is T – shaped and for both single & double gate junctionless transistor .The gate length (Lg), doping concentration (N_D), and oxide thickness (t_{OX}) are varied to estimate the effects of subthreshold current and gate capacitance (Cgg) of the device.

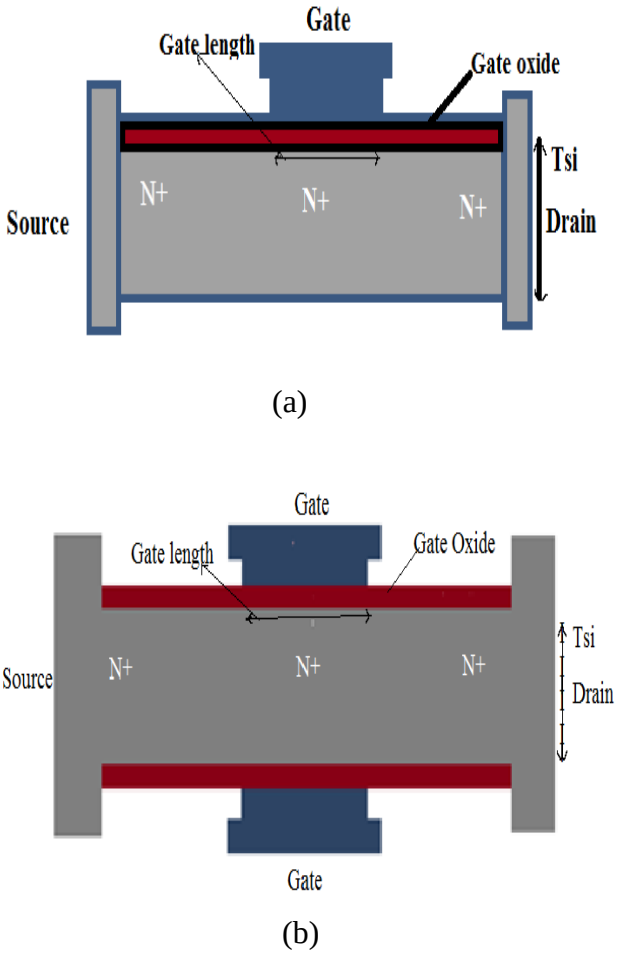

Fig.1. (a): 2D single gate; (b): double gate junctionless transistor.

III . SIMULATION RESULTS

A . Single gate and double gate JLT with different Doping concentration:

The single gate and double gate, as shown in Fig-1, is lightly doped. Fig-2 shows the variation of gate capacitance of single gate (Fig-2 (a)) and double gate (Fig-2(b)) by changing the gate voltages when the thickness of the gate oxide (t_{ox}) is 1nm, silicon thickness (Tsi) is 5nm and gate length(Lg) is10nm at a frequency of 1MHz. The gate capacitance is observed to be low for double gate JLT for different doping concentration changes from $1x10^{14}$ to $1x10^{20}$ cm^{-3}. The gate capacitance, C_{gg}, decreases when doping increases. In JLT, the channel is at the middle and capacitances are minimum with different doping concentration. The capacitance tends to saturate and eventually becomes constant as V_G is sufficiently large. The capacitance is very small at low potential and it is compared with triple gate junctionless transistor as proposed in [8] by Genoromariniello *et al.* The capacitance at negative voltage shows low and it increases linearly and saturate at higher gate voltage.

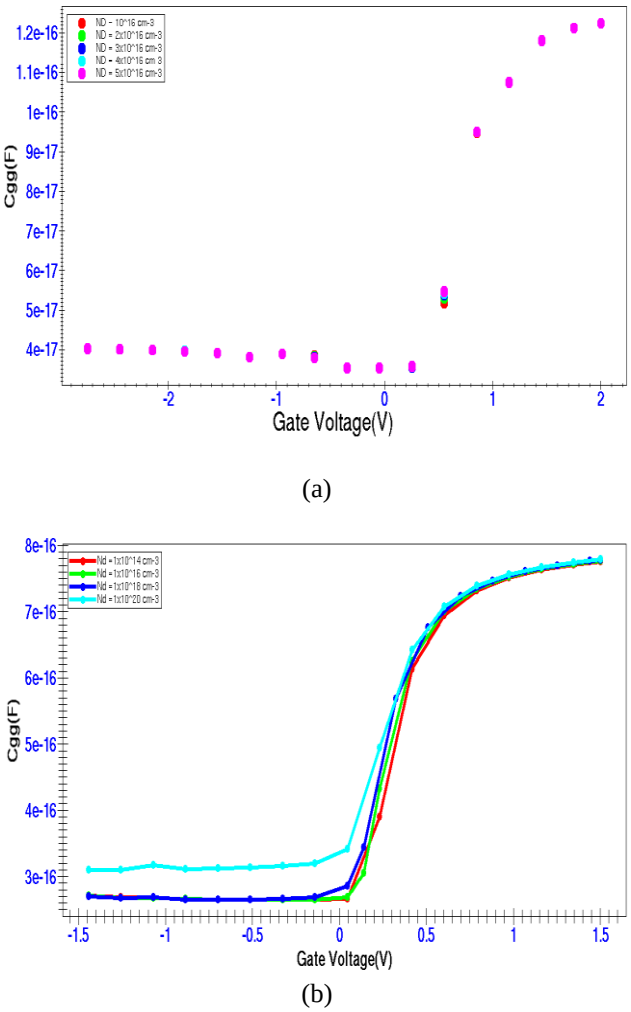

Fig.2. (a). Gate capacitance for lightly doped singe gate JLT.
(b) .Gate capacitance for lightly doped Double gate T shaped JLT.

B .Gate capacitance for different gate lengths

Fig .3 shows a double gate JLT where the gate length is 19nm, gate oxide thickness is 1nm and doped heavily which varies from $1x10^{14}$ to $1x10^{20}$ cm^{-3}.It is observed at low doping shows capacitance high compared to heavily doped device .According to ITRS for 19nm gate length the capacitance is 0.715fF for low power operation[9]. In T- gate JLT with19 nm gate length the gate capacitance is 1.77141fF Table -1 shows the detailed extracted results of C_{gg} at V_G =1v . A large amount of variation is observed when compared to an un-doped or lightly doped device. Increasing the doping its behaviour changes *w.r.t.* Gate voltages for a low drain voltage (V_{DS}). The result of the designed model is compared with the results in [7]. The threshold voltage (V_T) is at -0.5V and subthreshold slope and it observed as 60.8 mv/decade when the thickness of the silicon is at 5nm.

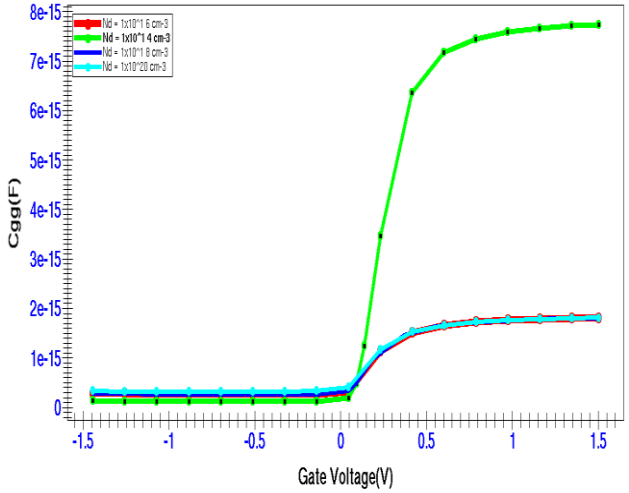

Fig.3. Gate capacitance for19 nm gate length with 1nm oxide thickness

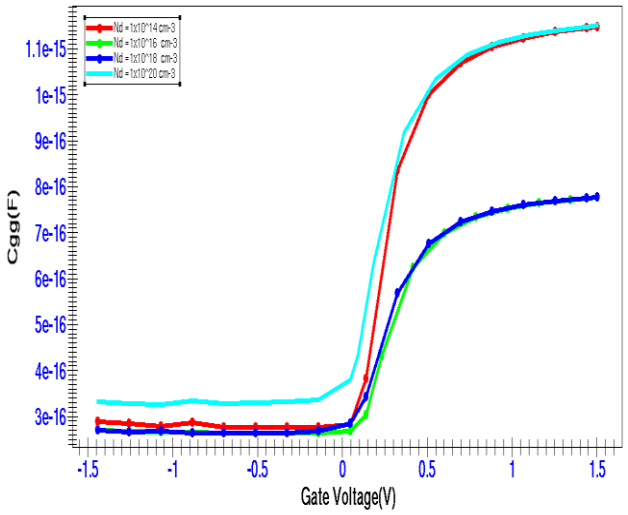

Fig.4. Gate capacitance for Gate length (Lg) of 5-nm with gate oxide thickness of 1-nm double gate T-shaped JLT.

Fig .4 shows the C_{gg} at gate length 5nm, oxide thickness 1nm, silicon thickness of 5nm and doping $1x10^{14}$ to $1x10^{20}$ cm^{-3}. All capacitances are minimum compared to 19 nm gate length. The threshold voltages is at -0.6V when doping concentration is increased and subthreshold slope shown in fig [5] is observed as 59.98 mv/dec which is less than the ideal value. The T- shaped gate is depleting the device fully and oxide is covered all over the silicon body for improved leakage current.

TABLE 1

Gate length (Lg)	Doping concentration(N_D) cm-3	Gate capacitance(Cgg) fF
19nm	1×10^{14}	7.60029
19nm	1×10^{16}	1.77823
19nm	1×10^{18}	1.77181
19nm	1×10^{20}	1.77141

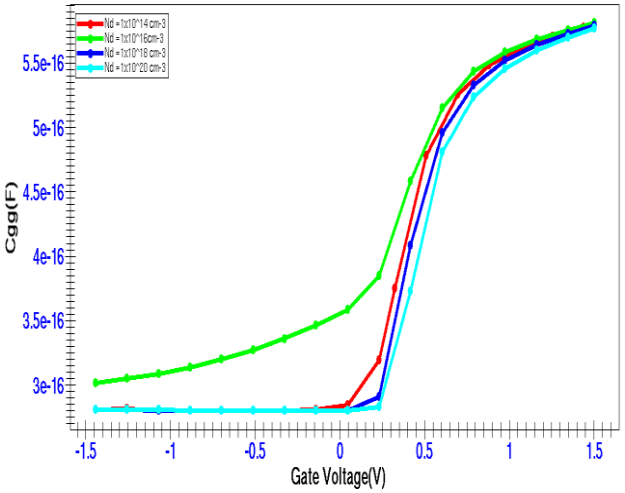

Fig.5. Gate capacitance for 1 nm gate length with 1nm oxide thickness

IV .CONCLUSION

A Symmetrical double gate junctionless transistor capacitance (Cgg) model is developed and is compared to single gate junctionless transistor for heavily doped device with increase in gate oxide thickness and doping concentration . In this paper gate capacitance is observed by changing different parameters and the result shows reduced gate capacitance C_{gg} for double gate w.r.t single gate T-shaped JLT. However the characteristics at higher frequency are not obtained and are kept for future research.

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