



High Performance Efficient Address Generator for WiMAX Deinterleaver

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ABSTRACT: Wireless technology is emerged has the vibrant research areas in the modern communication industry. The IEEE 802.16e has defined a standard commonly known as mobile WiMAX and emerged as the latest wireless technology that has promised to offer Broadband Wireless Access over long distance. This paper proposes an algorithm on address generation circuitry of Deinterleaver using QPSK and 16-QAM modulation for WiMAX transceiver. The floor function associated with the implementation of FPGA is very difficult in IEEE 802.16e standard. The requirement of floor function can be eliminated by using a simple mathematical algorithm. The main aim of the work is to concentrate on performance improvement by reducing interconnection delay, lesser power consumption, and efficient resource utilization by comparing with prevailing technique.

KEYWORDS: Deinterleaver/Interleaver circuit, Wireless systems.

I. INTRODUCTION

Broadband Wireless Access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies. IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX [1].

The channel interleaver employed in the WiMAX transceiver plays a vital role in minimizing the effect of burst error. Memory utilization and frequent memory accesses time are a crucial part of inter leaver design. Basically, the interleaving technique is to reorder the encoded data such that the adjacent bits can now become nonadjacent which can help handling the burst error occurring in those channels with memory. Although the basic concept of interleaving is straight-forward, the way of data reorder can be quite complex. In addition, to reorder a sequence of data requires a large memory buffer and frequent memory access such that the deinterleaver may become a crucial part of the overall decoder circuit in both area and power. Therefore, how to design an efficient deinterleaving circuit is very important [2].

In this paper, a novel, less-complexity, high-speed, and efficient resource address generator for the channel deinterleaver used in the WiMAX transceiver eliminating the requirement of floor function is proposed. Very few works related to hardware implementation of the project is used the interleaver/deinterleaver used in a WiMAX system is available in the literature. The work in [3] demonstrates the grouping of incoming data streams into the block to reduce the frequency of memory access in a deinterleaver using a conventional lookup table (LUT)- based CMOS address generator for WiMAX. A low cost and re-configurable architecture for address computation is always beneficial. IEEE 802.16e [5] called WiMAX is being used in the communication industry with many variants in channel coding, like different block sizes and different modulation schemes (e.g. BPSK, QPSK, 16 QAM and 64-QAM).

The type of interleaver used here is the block interleaver, in which the data is written sequentially in a memory and read in a random order after applying certain permutations.. Some work [2] – [4] has been published for the hardware

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implementation of WiMAX interleaver in different scenarios, but no mathematical formulation has been proposed behind the implementation. This paper emphasizes on reduction in complexity of the address generation by 2-D transformation of the original interleaving functions. Software simulation using ModelSim is performed to verify the functionality of the proposed algorithm and hardware. FPGA implementation results along with their possible comparison with recent similar work have been made.

Use of FPGA's embedded multiplier provides performance improvement by reducing interconnection delay, resource and power consumption compared with a configurable logic block-based multiplier [9].

II. RELATED WORK

2.1 WiMAX CHANNEL INTERLEAVER

The blocks of a WiMAX transceiver are shown in fig.1. The output of source is randomized before being encoded by two Forward Error Correction (FEC) coding techniques, namely, Reed–Solomon (RS) and Convolutional Coding (CC). The channel interleaver permutes the encoded bit stream to reduce the effect of burst error. When Convolutional Turbo Code (CTC) is used for FEC, being used as optional in WiMAX, hence the channel interleaver is not required; CTC itself includes an interleaver within it [7]. Modulation and construction of the orthogonal multiplexing symbols are performed by the two subsequent blocks, namely, mapper and Inverse Fast Fourier Transform (IFFT) of Fig.1. In the receiver end, the blocks are organized in the reverse order to obtain the restoration of the original data sequence at the output [8].

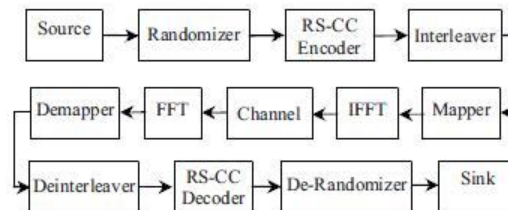


Fig. 1: Overview of WiMAX Transceiver[3]

Two-dimensional block interleaver/deinterleaver structure, is used as a channel interleaver/deinterleaver in the WiMAX system, is described in fig.2. It consists of two memory blocks, namely, M-1/2 and an address generator. In block interleaving, when one memory block is being written, the other is read, and vice versa. When sel =1, write enabled signal WE of M-1 is active. During this time, the input data stream is written in M-1 as it receives the write addresses. Simultaneously, an interleaved data stream is read from M-2 as it is supplied with the read addresses. After the memory blocks are written/read up to the desired location as specified by interleaver depth, the status of sel signal is changed to swap the write/read operation.

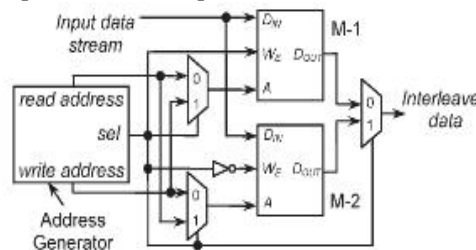


Fig .2 : Interleaver/Deinterleaver Structure

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The block interleaver/deinterleaver exploits different depths ‘ N_{cbps} ’ to incorporate various code rates and modulation schemes for IEEE 802.16e.

The data stream obtained from the RS-CC encoder is permuted by using the two-step processes described by (1) and (2).

$$m_k = \left(\frac{N_{cbps}}{d} \right) (k \% d) + \left\lfloor \frac{k}{d} \right\rfloor \quad (1)$$

$$j_k = s \times \left\lfloor \frac{m_k}{s} \right\rfloor + (m_k + N_{cbps} - \left\lfloor \frac{d \times m_k}{N_{cbps}} \right\rfloor) \% s \quad (2)$$

The number of columns is represented by d ($= 16/12$ for WiMAX); m_k and j_k are the outputs after the first and second steps, respectively; and k varies from 0 to $N_{cbps} - 1$. s is a parameter defined as $s = N_{cbps}/2$, where N_{cbps} is the number of coded bits per the subcarrier, i.e., 2, 4, or 6 for QPSK, 16-QAM, respectively. Modulo and floor functions are represented by percent and $\lfloor \cdot \rfloor$, respectively.

TABLE 1.

Permitted Interleaver/Deinterleaver depth in IEEE 802.16e for all code rates and Modulation type

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)	
	1/2	3/4	1/2	3/4
Interleaver Depth, N_{cbps} in bits	96	144	192	288
	192	288	384	576
	288	432	576	-
	384	576	-	-
	480	-	-	-
	576	-	-	-

2.2 Expressions for Deinterleaver

The deinterleaver performs the inverse operation, is also permuted by two step processes, i.e., (3) and (4). Let m_j and k_j define the first and second level of permutations for the deinterleaver, where j is the received bits index within a block of N_{cbps} bits.

Eqns.(3) and (4) perform inverse operation of (2) and (1), respectively.

$$m_j = s \cdot \left\lfloor \frac{j}{s} \right\rfloor + \left(j + \left\lfloor \frac{d \cdot j}{N_{cbps}} \right\rfloor \right) \% s \quad (3)$$

$$k_j = d \cdot m_j - (N_{cbps} - 1) \cdot \left\lfloor \frac{d \cdot m_j}{N_{cbps}} \right\rfloor \quad (4)$$

Due to the presence of a floor function in (3) and (4), their direct implementation on an FPGA chip is not feasible.

III. QPSK (QUADRATURE PHASE SHIFT KEYING)

Quadrature means the signal shifts among phase states that are separated by 90 degrees. The signal shifts as 90 degrees

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increments from 45° to 135° , -45° (315°), or -135° (225°) data into the modulator and is separated into two channels called I and Q. These two bits are transmitted one per channel simultaneously.

A better way to represent PSK schemes is using diagram. The points are shown in the complex plane where, in this regard, the real and imaginary axis are termed as in-phase and quadrature axes respectively due to their 90° separation. In PSK, the constellation points chosen are positioned with uniform angular spacing to give maximum phase-separation between adjacent points around a circle and thus the best immunity to corruption. They are positioned on a circle to transmit all of them with the same energy.

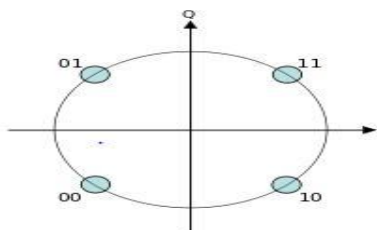


Fig. 3: Constellation diagram for QPSK

3.1 QAM (QUADRATURE AMPLITUDE MODULATION)

Quadrature amplitude modulation is both an analog and a digital modulation scheme. It sends two analog message signals, or two digital bit streams, by modulating the amplitudes of two carrier waves, using the amplitude-shift keying (ASK) digital modulation scheme or amplitude modulation (AM) analog modulation scheme. The two carrier waves, that are sinusoids, are out of phase with each other by 90° and hence are called quadrature components — hence the name of the scheme. The modulated waves are added, and the resulting waveform is a combination of both phase-shift keying (PSK) and amplitude-shift keying (ASK), or (in the analog case) of phase modulation (PM) and amplitude modulation. In the digital QAM, a finite number of at least two phases and at least two amplitudes are used. PSK modulators are usually designed using the QAM principle, but are not considered as QAM since the amplitude of the modulated carrier signal is constant. QAM is used widely as a modulation scheme for digital telecommunication systems. Arbitrarily high spectral efficiencies can be achieved with QAM by setting a finite constellation size, limited only by the noise level and linearity of the communications channel.

3.2 16-QAM: (16-state quadrature amplitude modulation)

Four I values and four Q values are used, yielding four bits per symbol 16 states since $4 \times 4 = 16$. Theoretical bandwidth efficiency is four bits/second/Hz. data is split into two channels, I and Q. As with QPSK, each channel will take on two phases. However, 16-QAM also accommodates two intermediate amplitude values. Two bits are routed to each channel simultaneously. The two bits to each channel are added, then applied to the respective channel's modulator.

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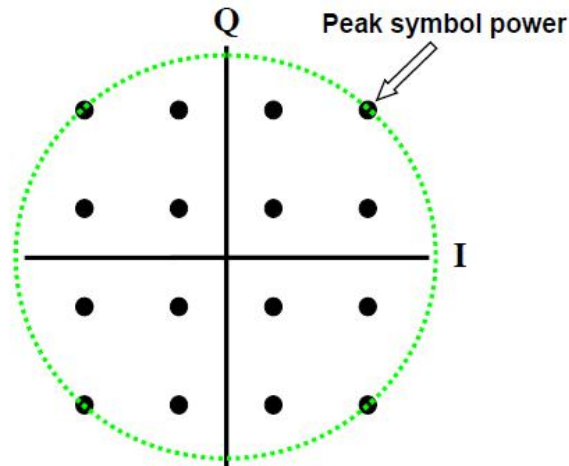


Fig. 3.1: Constellation diagram for 16-QAM

3.3 DESIGN METHODOLOGY OF ADDRESS GENERATOR

The deinterleaver address for the first four rows and five columns of each modulation type

- N_{cbps} =no.of code words=96
- J =row numbers=0,1,.....($d-1$).
- i =column numbers=0,1,.....(N_{cbps}/d)-1.
- K_n =deinterleaver addresses.
- No.of rows= $d=16$ (fixed)
- No.of columns= $N_{cbps}/d=96/16=6$

IV. THE PROPOSED ALGORITHM

The following algorithm for the QPSK and 16-QAM modulation schemes are proposed. These algorithm are also tested on MATLAB. Results obtained are verified with the previous MATLAB program for all code rates and modulation schemes of the WiMAX deinterleaver.

A. QPSK

```

Initialize  $N_{cpbs}$  and  $d$ 
For  $j=0$  to  $d-1$ ,  $j++$ 
  For  $i=0$  to  $(N_{cpbs}/d)-1$ ,  $i++$ 
     $K_n=d*i + j$ 
  end for
end for

```

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B. 16-QAM

```

initialize Ncbps and d
for j = 0 to d - 1, j ++
for i = 0 to (Ncbps/d) - 1, i ++
if (j mod 2 = 0)
kn = d * i + j
else
if (imod 2 = 0)
kn = d * (i + 1) + j
else
kn = d *(i - 1) + j
end if
end if
end for
end for
  
```

V. TRANSFORMATION INTO CIRCUIT

The address generator of the WiMAX deinterleaver with QPSK and 16-QAM hardware is as shown in Fig 5. The QPSK hardware has a row counter RWC_0 to generate row numbers between 0 and $d - 1$. A column counter CLC_0 with multiplexer M_0 and comparator C_0 generate the variable column numbers to implement permissible N_{cbps} . A multiplier M_0 and an adder A_0 perform the desired operations to implement deinterleaver address for QPSK. The address generator for 16-QAM follows as similar structure, such as that of QPSK with few additional modules. These modules are designed with an incrementer, a decremter, two modulo-2 blocks, and two multiplexers, as shown in fig. 5.2.

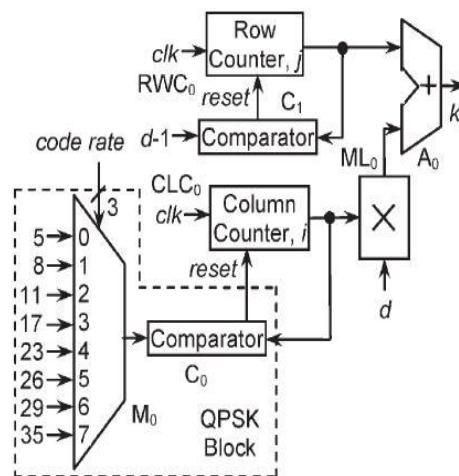


Fig .5.1: Hardware structure of the address generator for QPSK

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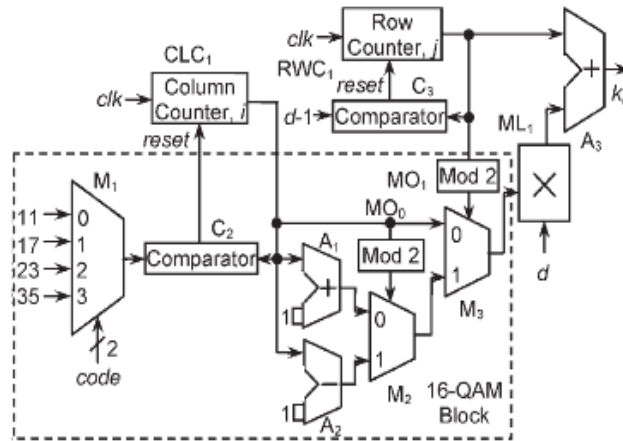


Fig .5.2.: Hardware structure of the address generator for 16-QAM

Implementation of the following blocks is done using verilog hardware description language. The design is optimized in the sense that common logic circuits such as multiplier, adder, rowcounter, and column counter are shared while generating addresses for any modulation type.

Table II
Determination of correlation between address[4]

Row no. (j)	Column no. (i) →	0	1	2	3	4
0	$N_{cbps} = 96$ -bits, $\frac{1}{2}$ code rate, QPSK	$d.0+0=0$	$d.1+0=16$	$d.2+0=32$	$d.3+0=48$	$d.4+0=64$
1		$d.0+1=1$	$d.1+1=17$	$d.2+1=33$	$d.3+1=49$	$d.4+1=65$
2		$d.0+2=2$	$d.1+2=18$	$d.2+2=34$	$d.3+2=50$	$d.4+2=66$
3		$d.0+3=3$	$d.1+3=19$	$d.2+3=35$	$d.3+3=51$	$d.4+3=67$
0	$N_{cbps} = 192$ -bits, $\frac{1}{2}$ code rate, 16-QAM	$d.0+0=0$	$d.1+0=16$	$d.2+0=32$	$d.3+0=48$	$d.4+0=64$
1		$d.1+1=17$	$d.0+1=1$	$d.3+1=49$	$d.2+1=33$	$d.5+1=81$
2		$d.0+2=2$	$d.1+2=18$	$d.2+2=34$	$d.3+2=50$	$d.4+2=66$
3		$d.1+3=19$	$d.0+3=3$	$d.3+3=51$	$d.2+3=35$	$d.5+3=83$

VI. SIMULATION RESULTS

The proposed hardware of the address generator is implemented using HDL Verilog using the Xilinx ISE. Simulation results are obtained for all permissible modulation types and code rates using ModelSimXE-III. The simulation results are verified with the output obtained from the MATLAB program.

