ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol.2, Special Issue 4, September 2014

A High Speed Vedic Multiplier Using Nikhilam Sutra with Barrel Shifter

L Kishore Kumar Reddy, M Venkata Subbaiah

M.Tech, Department of ECE, AITS, Kadapa, India

Assistant Professor, ITS, Kadapa, India

ABSTRACT: Multiplication is one of the most important operation in computer arithmetic. Many integer operations such as multiplication, squaring, division and computing reciprocal require same order of time as multiplication .This paper describes the implementation of an 64-bit Vedic multiplier enhanced in terms of propagation delay when compared with conventional multiplier like array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier. In our design we have utilized a barrel shifter which requires only one clock cycle for 'n' number of shifts. The propagation delay comparison was extracted from the synthesis report and static timing report as well.

KEYWORDS: Barrel shifter, base selection module, Propagation delay, power index determinant.

I.INTRODUCTION

Arithmetic operations such as addition, subtraction and multiplication are deployed in various digital circuits to speed up the process of computation. Arithmetic logic unit is also implemented in various processor architectures like RISC [2], CISC etc., In general, arithmetic operations are performed using the packed-decimal format. This means that the fields are first converted to packed-decimal format prior to performing the arithmetic operation, and then converted back to their specified format (if necessary) prior to placing the result in the result field.Vedic mathematics has proved to be the most robust technique for arithmetic operations. In contrast, conventional techniques for multiplication provide significant amount of delay in hardware implementation of n-bit multiplier. Moreover, the combinational delay of the design degrades the performance of the multiplier. Hardware-based multiplication mainly depends upon architecture selection in FPGA or ASIC.

In this work we have put into effect a high speed Vedic multiplier using barrel shifter. The sutra was implemented by modified design of "Nikhilam Sutra" [1] due to its feature of reducing the number of partial products. The barrel shifter used at different levels of design drastically reduces the delay when compared to conventional multipliers. The hardware implementation of Vedic multiplier using barrel shifter contributes to adequate improvement of the speed in order to achieve high outturn Section II provides an abrupt introduction of Vedic sutras. Section III describes the modified Nikhilam sutra architecture. Section IV simulation results and design analysis of basic Conventional multipliers and proposed design. Section V represents the conclusions

II. VEDIC SUTRAS

Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Application of the Sutras saves a lot of time and effort in solving the problems, compared to the formal methods presently in vogue. Though the solutions appear like magic, the application of the Sutras is perfectly logical and rational. The computation made on the computers follows, in a way, the principles underlying the Sutras. The Sutras provide not only methods of calculation, but also ways of thinking for their application.Application of the Sutras improves the computational skills of the learners in a wide area of problems, ensuring both speed and accuracy, strictly based on rational and logical reasoning. Application of the Sutras to specific problems involves rational thinking, which, in the process, helps improve intuition that is the bottom - line of the mastery of the mathematical geniuses of the past and the present such as Aryabhatta, Bhaskaracharya, Srinivasa Ramanujan, etc.,

Multiplier implementation using FPGA has already been reported using different multiplier architectures but the performance of multiplier was improved in proposed design.By employing Vedic multiplier using modified "Nikhilam

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol.2, Special Issue 4, September 2014

Navatascaramam Dasatah" sutra. The architecture in [1] is modified using barrel shifter by which significant amount of clock cycles are reduced by virtue of which the speed increases. The performance of the proposed multiplier is compared with the previously implemented multipliers on FPGA.What we call "Vedic mathematics" is comprised of sixteen simple mathematical formulae from the Vedas [5].

1. Ekadhikena Purvena
2. Nikhilam navatascaramam Dasatah
3. Urdhva - tiryagbhyam
4. ParavartyaYoayet
5. Anurupye - Sunyamanyat
6. Sankalana - Vyavakalanabhyam
7. Puranapuranabhyam
8. Calana - Kalanabhyam
9. Ekanyunena Purvena
10. Anurupyena
11. Adyamadyenantya - mantyena
12. Yavadunam Tavadunikrtya Varganca Yojayet
13. Antyayor Dasakepi
14. Antyayoreva
15. Gunita Samuccayah.

III. PROPOSED MULTIPLIER ARCHITECTURE DESIGN

Assume that the multiplier is 'X' and multiplicand is 'Y'. Though the designation of the numbers is different but the architecture implemented is same to some extent for evaluating both the numbers. The mathematical expression for modified nikhilam sutra is given below.

$$P=X*Y= (2^{k2})*(X\pm Z2*2^{(k1-k2)})\pm Z1*Z2. - (1)$$

Where k1, k2 are the maximum power index of input numbers X and Y respectively. Z1 and Z2 are the residues in the numbers X and Y respectively. The hardware deployment of the above expression is partitioned into three blocks.

i. Base Selection Module
ii. Power index Determinant Module
iii. Multiplier.

The base selection module (BSM) is used to select the maximum base with respect to the input numbers. The second sub-module power index determinant(PID) is used to extract the power index of k1 and k2. The multiplier comprises of base selection module (BSM), power index determinant (PID), subtractor, barrel shifter, adder/subtractor as sub-modules in the architecture.

A. Base selection module:

The base selection module has power index determinant (PID) as the sub-module along with barrel shifter, adder, average determinant, comparator and multiplexer. An input 8-bit number is fed to power index determinant (PID) to interpret maximum power of number which is fed to barrel shifter and adder. The output of the barrel shifter is 'n' number of shifts with respect to the adder output and the input based to the shifter. Now, the outputs of the barrel shifter are given to the multiplexer with comparator input as a selection line. The outputs of the average determinant and the barrel shifter are fed to the comparator. The required base is obtained in accordance with the multiplexer inputs and its corresponding selection line.

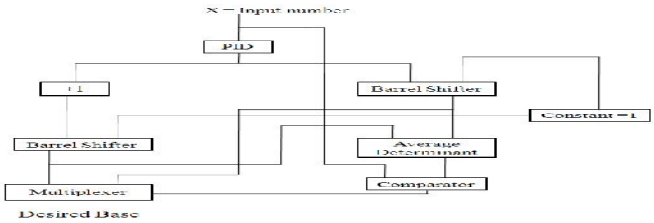

Fig.1 Base Selection Module, BSM

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol.2, Special Issue 4, September 2014

B. Power index determinant:

The input number is fed to the shifter which will shift the input bits by one clock cycle. The shifter pin is assigned to shifter to check whether the number is to be shifted or not. In this power index determinant (PID) the sequential searching has been employed to search for first '1' in the input number starting from MSB. If the search bit is '0' then the counter value will decrement up to the detection of input search bit is '1'. Now the output of the decrementer is the required power index of the input number.

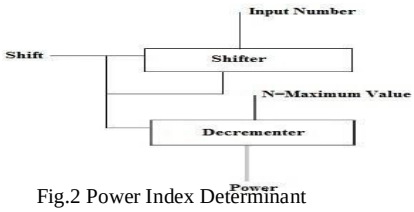

Fig.2 Power Index Determinant

C. Multiplier Architecture:

The base selection module and the power index determinant form integral part of multiplier architecture. The architecture computes the mathematical expression in equation1.Barrel shifter used in this architecture.The two input numbers are fed to the base selection module from which the base is obtained. The outputs of base selection module (BSM) and the input numbers 'X' and 'Y' are fed to the subtractors. The subtractor blocks are required to extract the residual parts z1 and z2. The inputs to the power index determinant are from base selection module of respective input numbers. The sub-section of power index determinant (PID) is used to extract the power of the base and followed by subtractor to calculate the value. The outputs of subtractor are fed to the multiplier that feeds the input to the second adder or subtractor. Likewise the outputs of power index determinant are fed to the third subtractor that feeds the input to the barrel shifter. The input number 'X' and the output of barrel shifter are rendered to first adder/subtractor and the output of it is applied to the second barrel shifter which will provide the intermediate value. The last sub-section of this multiplier architecture is the second adder/subtractor which will provide the required result.

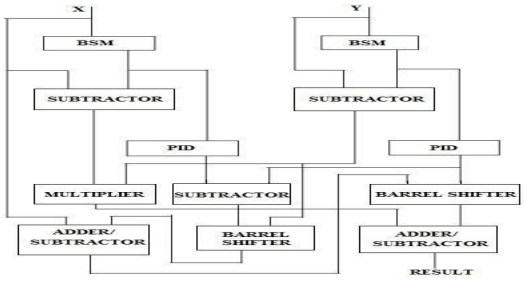

Fig.3 Multiplier Architecture

IV. SIMULATION RESULTS AND DESIGN ANALYSIS

Comparison between conventional multipliers and proposed design is been projected below. Around 95% of reduction in delay can be observed from the proposed design with respect to array multiplier in Table I. The analysis provides much in depth coverage between conventional multipliers and modified Vedic multiplier architecture

Multiplier type	Conventional Multiplier(Array)	Proposed Multiplier
Delay(ns) (64-Bit)	111.748	4.040

TABLE I. DELAY COMPARISON

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol.2, Special Issue 4, September 2014

A. Timing summary

Speed grade: -5

Minimum period: 4.040ns (Maximum frequency: 147.4 MHz) Maximum input arrival time before clock:39.80 ns Maximum output required time after clock: 4.040 ns

B. Timing Details

All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for clock 'clk'

Clock period: 4.040ns (frequency: 147.47 MHz) Total no of paths / destination ports: 22313 / 104 Delay: 4.040ns (levels of logic=7)

Source: rsu2/power_index_determinant/temp_pow_0_1 (FF) Destination: exponent2/ temp_5 (FF)

Source clock: clock rising Destination clock: clock rising.

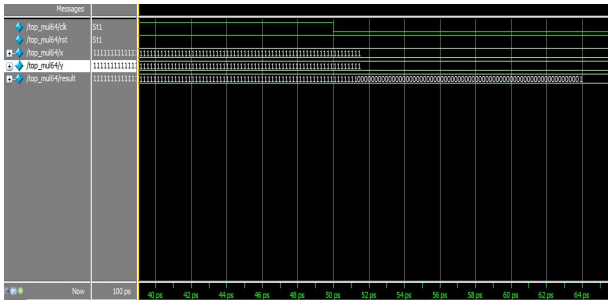

Fig4. Simulation Result

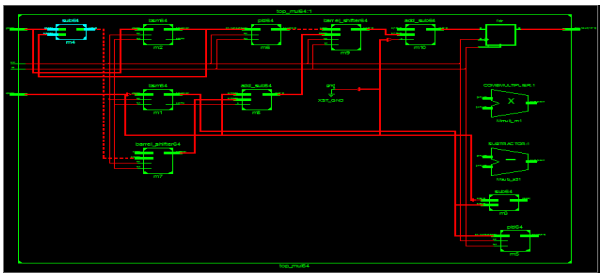

Fig5. RTL Schematic of Multiplier

V. CONCLUSION

In our design, efforts have been made to reduce the propagation delay and achieved an improvement in the reduction of delay when compared to array multiplier, booth multiplier and conventional Vedic multiplier. The high speed implementation of such a multiplier has wide range of applications in image processing, arithmetic logic unit and VLSI signal processing The future scope of this particular work can be extended in design of ALU's in RISC processor.

REFERENCES

1. Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, "High speed ASIC design of complex multiplier using vedic
2. mathematics" , Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, lIT Kharagpur, pp. 237-241.
3. Shamsiah Suhaili and Othman Sidek, "Design and plementation of reconfigurable alu on FPGA", **3**rd International Conference on Electrical & Computer Engineering ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh, pp.56-59.
4. Sumit Vaidya and Deepak Dandekar, "Delay-power performance comparison of multipliers in vlsi circuit design", International Journal
5. Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010, pp.47-56.
6. P. Mehta, and D. Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier," in Proceedings IEEE International Conference on Advances in Computing, Control, and Telecommunication Technologies, Trivandrum, Kerala, Dec. 28-29, 2009, pp. 640-642.

7. J. S. S. B. K. T. Maharaja, Vedic mathematics, Delhi: Motilal Banarsidass Publishers Pvt Ltd,(2010).